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Design And Analysis Of 15:4 Compressor

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ABSTRACT : Compressors play a significant role in high speed systems. Reduction of partial products takes much time and consume more power in the multiplier. But it will create more number of stages to reduce the partial product reduction. To overcome these problems compressors are used. This paper proposes the design and analysis of 15:4 compressor. The 5:3 compressor is the basic module used in 15:4 compressor reduces power dissipation. All design and simulations were done in Mentor graphics tool 130nm Technology.
Keywords – High speed systems, Multiplier, 15:4 compressor, 5:3 compressor, power dissipation.

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I. INTRODUCTION

The popularity and demand of high speed electronic systems are continuously increasing day by day. Hence the development of a fast and efficient system design has been a subject of interest of VLSI design engineers over decades. A processing element called compressor is widely used in high speed system. Compressors can handle large number of inputs than half and full adders. The popularity and demand of compressors are rapidly increasing in many parts of a digital system, particularly in digital signal processors. Multipication is the complex operation which consumes most of the processing time and power. Compressors are utilized to improve better performance of on the optimization of circuit structures for high-speed applications at standard supply voltages.

The rest of the paper is oraganized as follows: Compressor description is given in Section II. Section III, explains about 8:4 Compressor. Section IV, consider about 9:4 Compressor. Section V, cover about 5:3 Compressor. Section VI, study about 15:4 Compressor. Section VII, discussed about results of the designed modules. Finally, in section VIII, concludes the paper.

II. COMPRESSOR

Compressors are the fundamental building blocks used for accumulating the partial products during the multiplication process. Compressors are basic circuits which are made of full adders or half adders to count the number of ``ones'' in the input. Use of compressors not only reduce the vertical critical path but also reduce the stage operations simultaneously. Higher order compressors provide better results in terms of power and speed.

III. 8:4 COMPRESSOR

In 8:4 Compressor three stages of adders are used to compress the input bits into four output bits. It uses three half adders and four full adders to compress the inputs by applying all sum **o**utputs of the first stage to one adder of the second stage and all carry outputs to another adder. The schematic diagram of 8:4 compressor is shown in figure 1.
The logic equations of 8:4 compressor as follows.

$x_1 = a \oplus c \oplus e$ (1)

$x_2 = (ac+ae+ce) \oplus (b \oplus d \oplus f)$ (2)

$x_3 = ((ac+ae+ce).(b \oplus d \oplus f)) \oplus (bd+bf+df)$ (3)

$x_4 = ((ac+ae+ce).(b \oplus d \oplus f)).(bd+bf+df)$ (4)

where

$a = i_0 \oplus i_1$ (5)

$b = i_0.i_1$ (6)

$c = i_2 \oplus i_3 \oplus i_4$ (7)

$d = ((i_2.i_3)+(i_2.i_4)+(i_3.i_4))$ (8)

$e = i_5 \oplus i_6 \oplus i_7$ (9)

$f = ((i_5.i_6)+(i_5.i_7)+(i_6.i_7))$ (10)

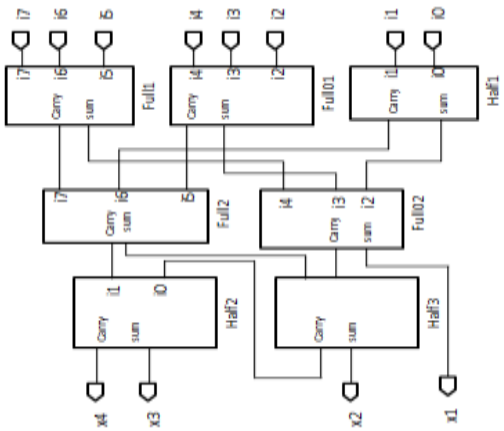


Fig 1: Schematic diagram of 8:4 compressor

IV. 9:4 COMPRESSOR

In 9:4 compressor three stages of adders are used to compress the input bits into output bits. It uses two half adders and five full adders to compress the inputs by applying all sum **o**utputs of the first stage to one adder of the second stage and all carry outputs to another adder. The schematic diagram of 9:4 compressor is shown in Fig. 2

The logic equations of 9:4 compressor as follows.

$x_1=a \oplus c \oplus e$ (11)

$x_2 = (ac+ae+ce) \oplus (b \oplus d \oplus f)$ (12)

$x_3 = ((ac+ae+ce).(b \oplus d \oplus b)) \oplus (bd+bf+df)$ (13)

$x_4 = ((ac+ae+ce).(b \oplus d \oplus b)).(bd+bf+df)$ (14)

where

$a= i_0 \oplus i_1 \oplus i_2$ (15)

$b=(i_0 .i_1)+(i_0.i_2)+(i_1. i_2)$ (16)

$c= i_3 \oplus i_4 \oplus i_5$ (17)

$d=((i_3.i_4)+(i_3.i_5)+(i_4.i_5))$ (18)

$e= i_6 \oplus i_7 \oplus i_8$ (19)

$f=((i_6.i_7)+(i_6.i_8)+(i_7.i_8))$ (20)

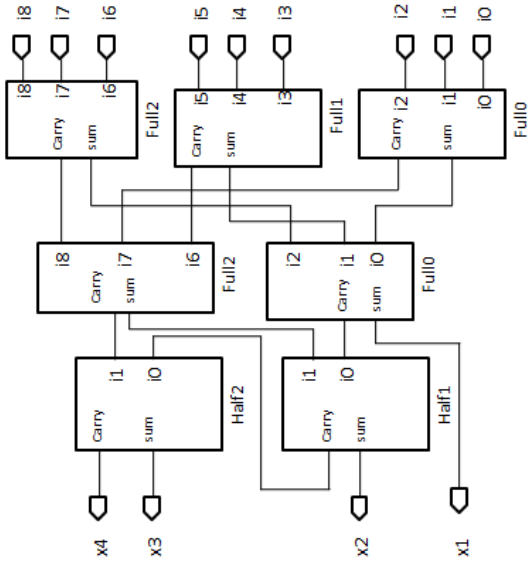


Fig 2: Schematic diagram of 9:4 Compressor

V. 5:3 COMPRESSOR

In 5:3 compressor has 5 input EXOR gate and produce the output as O_0 and other EXOR gates, AND gates, OR gate generate and produce the outputs as O_1, O_2. The schematic diagram of 5:3 compressor is shown in Fig. 3

The logic equations of 5:3 compressor as follows.

$o_1 = x_4 \oplus (x_0.(\sim(x_0 \oplus x_1))+(x_2.(x_0 \oplus x_1)))$ (21)

$o_2 = x_4.(x_0.(\sim(x_0 \oplus x_1))+(x_2.(x_0 \oplus x_1)))$ (22)

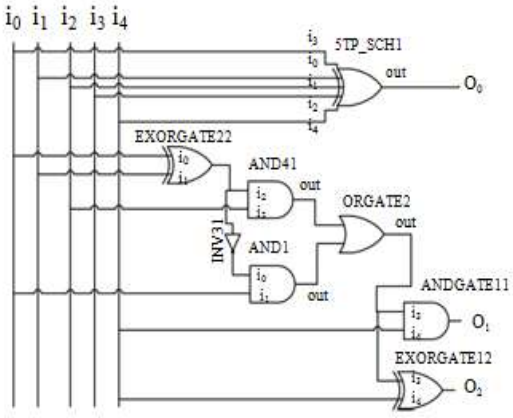


Fig 3: Schematic diagram of 5:3 compressor

VI. 15:4 COMPRESSOR

The design of 15:4 compressor has five full adders at first stage, two 5:3 compressors in second stage and parallel adder at final stage. Design of 5:3 compressor is implemented in 15:4 compressor which will result increased speed and reduced power consumption. The outputs will be checked by using the outputs of full adders in 15:4 compressor, 5:3 compressor and 4 bit parallel adder. The schematic diagram of 15:4 compressor is shown in fig 4.

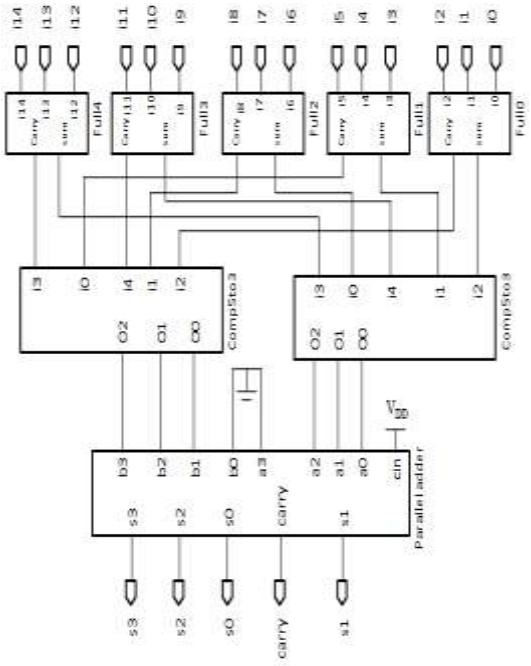


Fig 4: Schematic diagram of 15:4 compressor

VII. SIMULATION RESULTS

Simulation results of 15:4 compressor is shown in Fig. 5

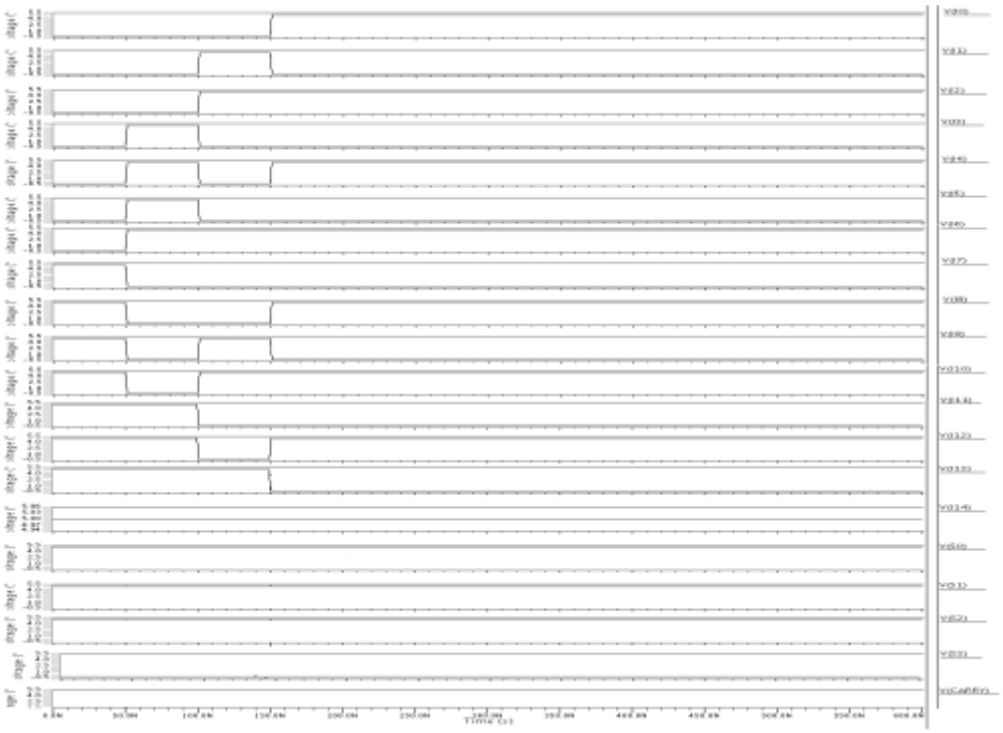
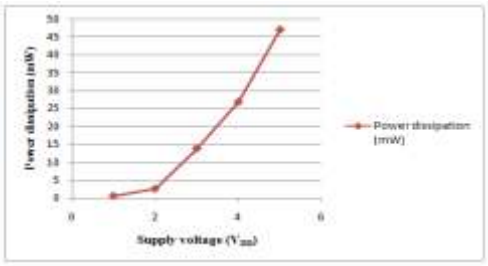


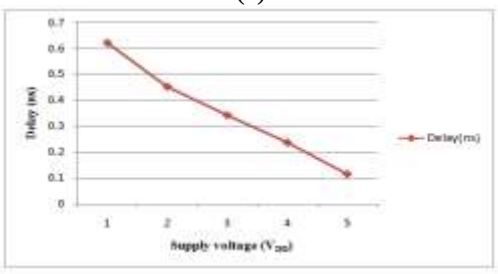
Fig 5: Simulation results of 15:4 Compressor

Table 1: Performance comparison of 8:4 compressor

Supply voltage (V_{DD})	Power dissipation (mW)	Delay(ns)
1	0.53257	0.62180
2	2.5518	0.45308
3	13.800	0.34258
4	26.776	0.23726
5	46.976	0.11505



(a)



(b)

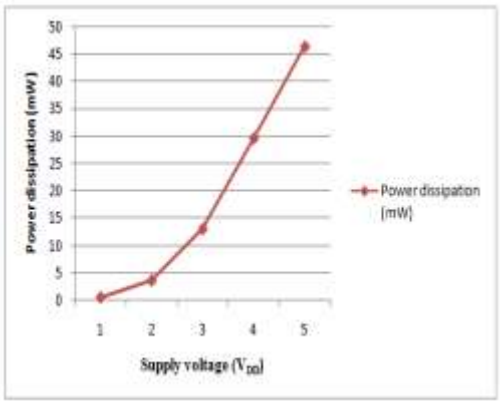
Fig 5: Graphical representations of 8:4 compressor from table1

(a) Power dissipation Graph
(b) Delay Graph

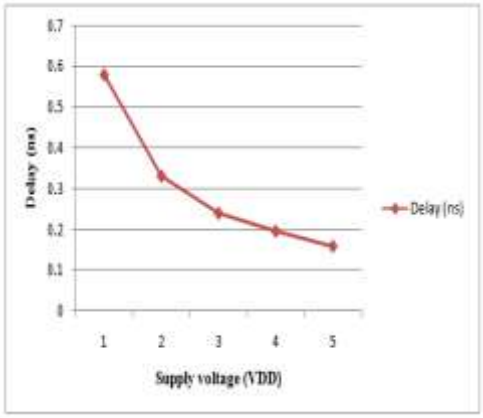
From table 1 and Fig. 5, it is observed that when supply voltage increases, power dissipation increases then delay gets reduced.

Table 2: Performance comparison of 9:4 compressor

Supply voltage (V_{DD})	Power dissipation (mW)	Delay (ns)
1	0.56899	0.581
2	3.6610	0.332
3	13.056	0.241
4	29.606	0.197
5	46.335	0.160



(a)



(b)

Fig 6: Graphical representations of 9:4 compressor from table2

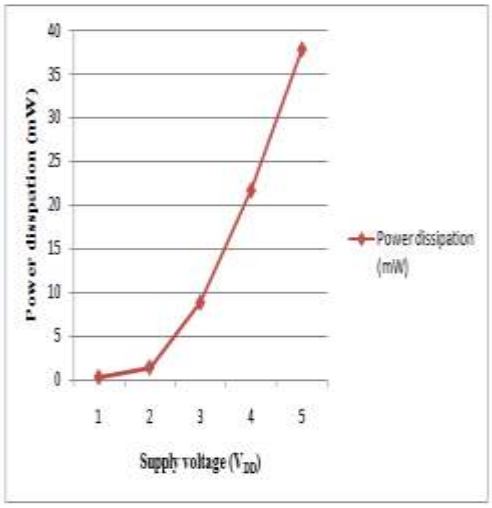
(a) Power dissipation Graph

(b) Delay Graph

From table 2 and Fig. 6, it is found that when supply voltage increases, power dissipation increases then delay gets reduced.

Table 3: Performance comparison of 15:4 compressor

Supply voltage (V_{DD})	Power dissipation (mW)	Delay (ns)
1	0.30639	0.803
2	1.4156	0.499
3	8.8308	0.448
4	21.679	0.398
5	37.808	0.279



(a)

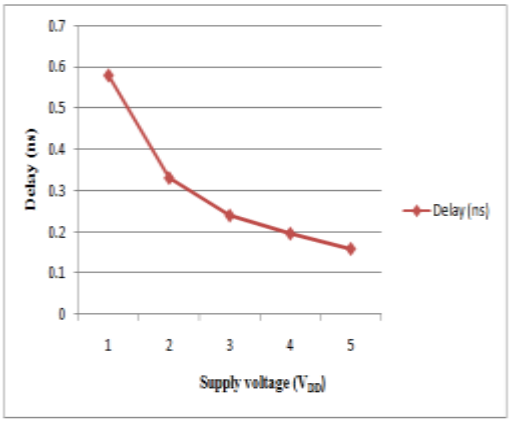


Fig 7: Graphical representations of 15:4 compressor from table3

(a) Power dissipation Graph

(b) Delay Graph

From table 3 and Fig. 7, it is observed that supply voltage increases, power dissipation increases then delay gets reduced.

VIII. CONCLUSION

In this paper different compressors are designed using static CMOS logic. Simulations carried out using Mentor Graphics at 130 nm technology. The advantage of compressors not only reduced partial product reduction but also reduce stage operations simultaneously. The power dissipation is found to be reduced for 15:4 compressor compared to 8:4 and 9:4 compressors at supply voltage of 5V.

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