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Ultralow-Power and Secure IoT for Biomedical Applications

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ABSTRACT
With the advent of Internet of Things (IoT), remote, continuous, and non-invasive monitoring of patients is gaining importance. Energy efficiency and security are the major challenges faced by the researchers for the IoT enabled biomedical devices. Electrocardiogram (ECG) plays a vital role in detecting heart related abnormalities. In this paper, an ECG data acquisition system is implemented using Positive Feedback Adiabatic Logic (PFAL) to reduce power consumption and at the same time provide security. Simulations by Mentor Graphics tool using 130 nm technology indicate reduction of power consumption and power-delay product of about 63% and 60% respectively is achieved with PFAL as compared to conventional CMOS design.
Key words: biomedical, data acquisition, ECG, IoT, PFAL, secure, ultralow-power

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I. INTRODUCTION

Due to food habits, lack of exercise, and increasing work pressure, many people world over are suffering from cardiovascular diseases. This leads to substantial expenditure for treatment and also loss of life. The burden on the middle-income families is prohibitively large and developing countries need to spend huge amount on health sector.

The most important tool for the diagnosis of cardiovascular diseases is Electrocardiogram (ECG). The traditional ECG instruments suffer from bulky in size, lack of freedom to move, wired connection, and requirement for in-hospital examination. With the rapid development of wireless body sensor networks, wearable technology, and Internet of Things (IoT) [1], large number of IoT enabled biomedical and implantable medical devices [2], ranging from ECG processors [3] and cardiac defibrillators [4] to insulin pumps [5] and pacemakers [6] are being deployed. These IoT devices allow continuous acquisition, monitoring, and pre-processing of health data that can be transmitted over the network to hospitals for diagnosis and treatment. Continual monitoring for extended lifetimes and reliance on battery power imposes strict power consumption constraints on implantable medical and wearable devices. The increased use of portable and IoT enabled ECG monitoring devices now-a-days requires design of energy-efficient and secure ECG systems.

Various studies related to hardware, data compression, communication protocol, coding technology have been carried out to reduce the energy consumption. A low-power analog IC for effective wireless ECG data acquisition was fabricated by Tsai, et al. [7]. Yazicioglu et al. [8] reduced the power dissipation of a biopotential sensor node using mixed-signal design approach. A distance-based energy-efficient data strategy to lower the transmission power in both the sensor node level and network level was proposed by Yan et al. [9]. Nemati et al. [10] employed ANT protocol for reducing the power consumption of a wireless capacitive ECG node. These techniques are not suitable for providing security.

In addition to power consumption, recently, security of biomedical devices has gained significant attention. Wireless sensor network devices used in healthcare commonly store secure or personal information and they are vulnerable to many threats in the form of side-channel attacks. A differential power analysis (DPA) attack is considered one of the most powerful side-channel attacks. Several hardware based countermeasures have been developed over the years [11], [12] and implemented at several hierarchical levels including architecture, the block level, the register transfer level (RTL), and the circuit level [13]-[16]. However, these methods are not suitable for applications where the power consumption is the main concern.

Adiabatic logic is one of the circuit design techniques to design energy-efficient and secure hardware. Ultralow-power adiabatic logic and quasi-adiabatic logic were introduced in the 1990s. They were first considered as a countermeasure against DPA attacks in [17]-[20]. In this paper, ECG data acquisition system is implemented using positive feedback adiabatic logic (PFAL) to

achieve ultralow-power consumption as well as security.

The remaining part of the paper is organized as follows. Background of the work is given in section II. Section III gives the details of the implementation of ECG data acquisition system using both static CMOS and PFAL. The simulation results are presented in section IV and finally section V concludes the paper.

II. BACKGROUND

2.1 ECG system

The block diagram of an ECG data acquisition system is shown in Fig.1. The ECG signals that are generated by electrical activity in the heart are acquired using electrodes. These are a small pulse train having amplitude of 0.01–5 mV and bandwidth of 0.05–150 Hz. This small amplitude signal is amplified by an instrumentation amplifier consisting of two opamp stages and then bandpass filtered to remove low and high frequency noise signals. The instrumentation amplifier shall provide adequate gain and high CMRR. The amplified and filtered signal is converted into 8-bit digital signal for further processing using PC.

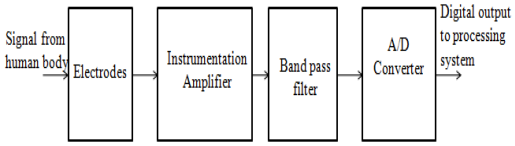


Figure 1. Block diagram of ECG data acquisition system

2.2 Adiabatic logic

The term adiabatic is derived from the Greek word 'adiabatos', means impassable. It also indicates that state change occurs without loss or gain of energy. It makes use of a time-varying voltage instead of DC source to provide a constant current for charging or discharging of the capacitive nodes so that the power dissipation can be minimized. The main idea of adiabatic switching is that transitions occur at a considerably slower rate, so that heat is not emitted. The energy dissipation, E_{diss} in the channel resistance R of an adiabatic network is given by

$$E_{diss} = \xi P \Delta T$$
$$= \xi \bar{I}^2 R \Delta T$$
$$= \xi \left(\frac{CV_{dd}}{\Delta T}\right)^2 R\Delta T \quad (1)$$

where'$\bar{I}$' is the average current flowing into the load capacitance C and ξ is the shape factor which depends on the type of supply clock. From (1), it is clear that when the charging period ΔT is long, then the theoretical energy dissipation is reduced to zero. Fig.2 shows the basic PFAL buffer/inverter. Two cross-coupled inverters formed as latch element, to store the output state, and the functional blocks are connected in parallel to the PMOS transistor.

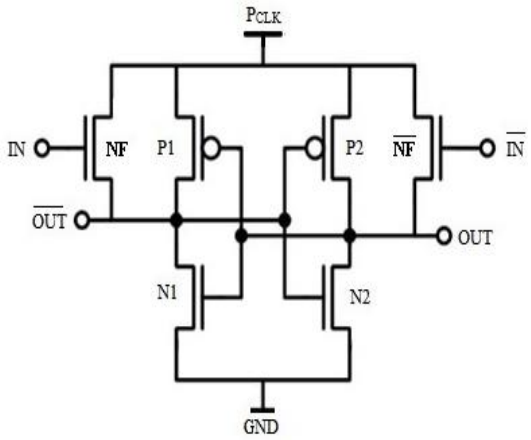


Figure 2. PFAL buffer/inverter

III. IMPLEMENTATION OF ECG DATA ACQUISITION SYSTEM

In order to obtain the electrocardiogram, the small biopotentials developed by human body are acquired using conducting electrodes, amplified by instrumentation amplifier, filtered to remove unwanted noise, converted to digital form for processing by computer and recording of data. To reduce power consumption and to provide security the circuits are implemented using PFAL logic. To find the amount of power saving with PFAL, static CMOS implementation is also carried out.

3.1 Instrumentation amplifier

The amplifier to be used for amplification of ECG signals shall have high input impedance, gain sufficient to display the ECG signal, able to accept low power signals from the sensors, amplify low frequency signals with constant gain, reject the common mode signals, and provide a high signal to noise ratio. To get the required characteristics of high input impedance and high CMRR, a two-stage opamp instrumentation amplifier is used. Fig.3 shows the implementation of instrumentation amplifier using static CMOS and PFAL logic.

Taking an L value of 0.2 μm, the W/L ratios of the transistors are listed in Table 1. A supply voltage V_{dd} of 1V is used for the static CMOS circuit, while the PFAL circuit is given a power clock signal of 1V amplitude and 20Hz frequency. The amplifier is fed with a differential signal of 2.5 mV amplitude and 20 Hz frequency. The corresponding output voltages and CMRR of static CMOS and PFAL circuits are 182.5 mV and 202.5 mV respectively. The CMRR of the circuits are found to be 62 dB and 75 dB respectively.

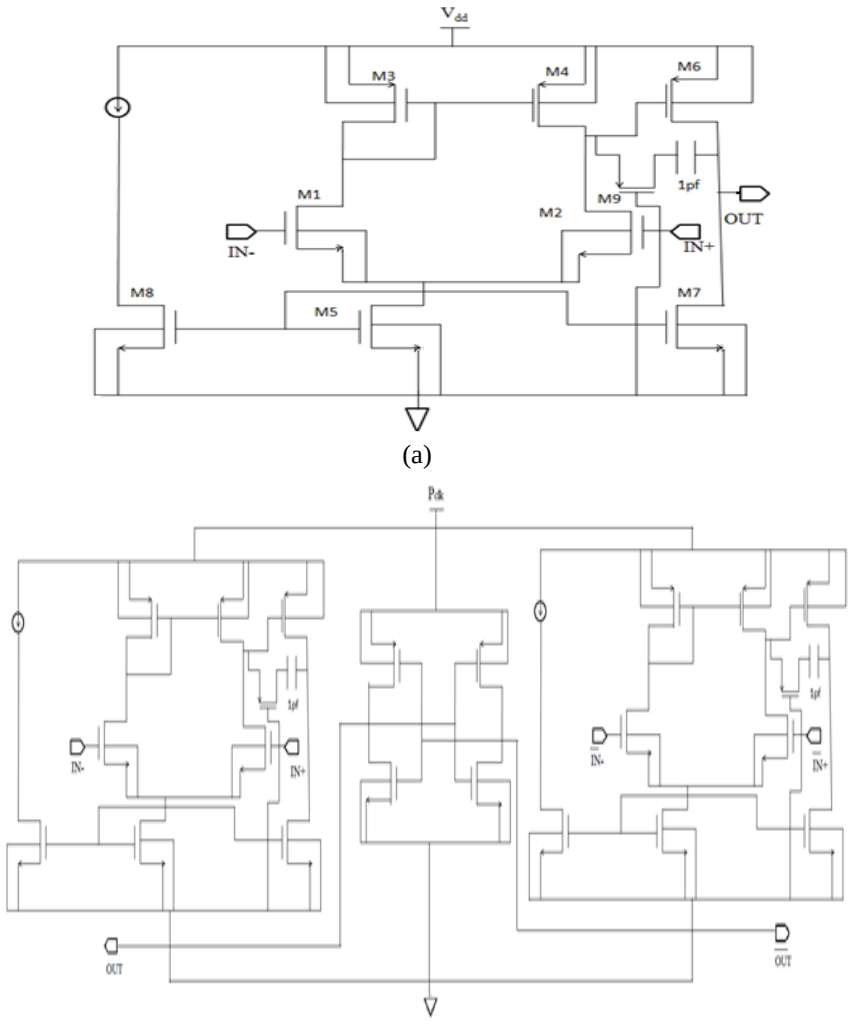


Figure 3. Schematic of instrumentation amplifier using (a) static CMOS and (b) PFAL

Table 1. The W/L ratios of the transistors

Transistors	**W/L ratio**
M1, M2	1
M3, M4	1
M5, M8	1/3
M6	2.5/0.2
M7	3
M9	1/2

3.2 Bandpass filter

The ECG signal is often corrupted by various noises originating from the body. These include the low frequency baseline wander noise due to offset voltages in the electrodes, respiration, and body movement, and high frequency noise due to power line interference and muscle contraction. The amplified signal is bandpass filtered to remove these noise components. The schematic of a bandpass filter is shown in Fig. 4 and its static CMOS implementation in Fig. 5. The amplifier section of the bandpass filter implemented using PFAL is shown in Fig. 6. The corner frequencies of high pass and low pass sections are found to be 0.053 Hz and 159 Hz respectively.

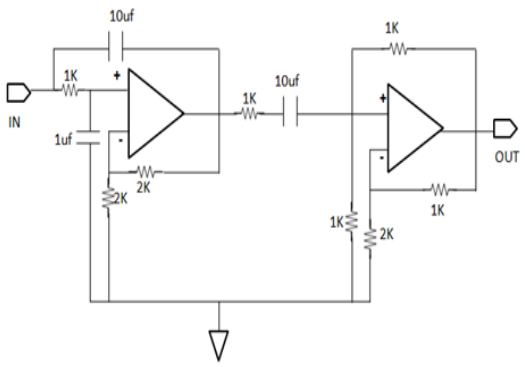


Figure 4. Schematic of band pass filter

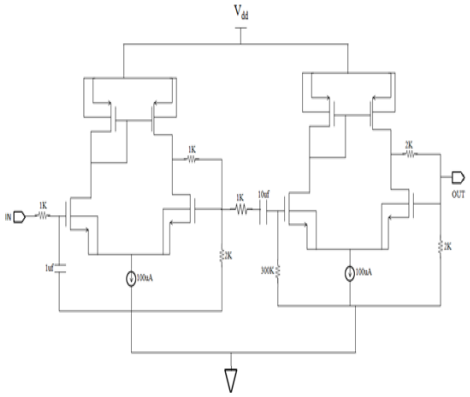


Figure 5. Static CMOS band pass filter

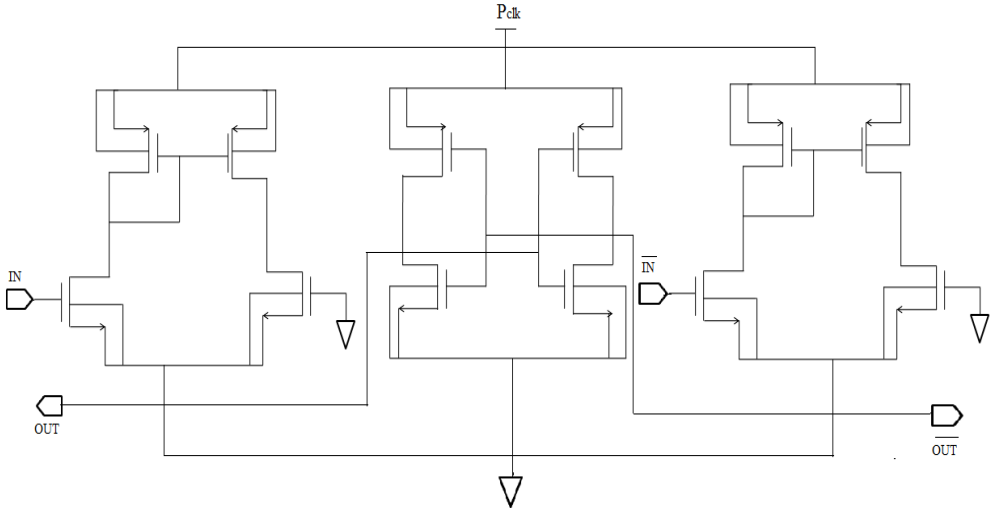


Figure 6. PFAL amplifier of bandpass filter

3.3 Analog to digital converter

For processing the ECG signal using computer and display it as waveform requires analog form of the signal to be converted into digital form. In this work an 8-bit analog to digital converter (ADC) is implemented using both static CMOS and PFAL logic. The 8-bit ADC is obtained by extending the 2-bit ADC. Fig. 7 shows the schematic of a 2-bit flash type ADC. The comparator and other gates required are implemented using static CMOS and PFAL. The PFAL NAND gate, CMOS and PFAL comparator realizations are shown in Fig. 8. The output of ADC is to be fed to computer through USB for processing of ECG signals.

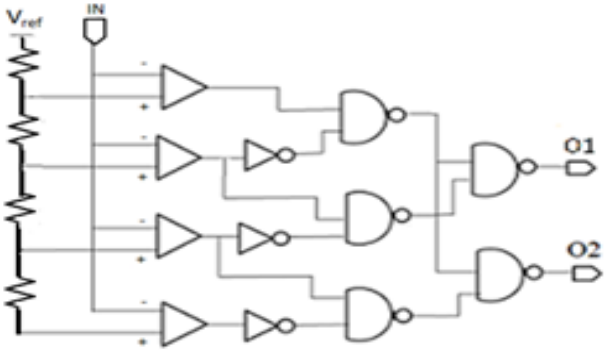
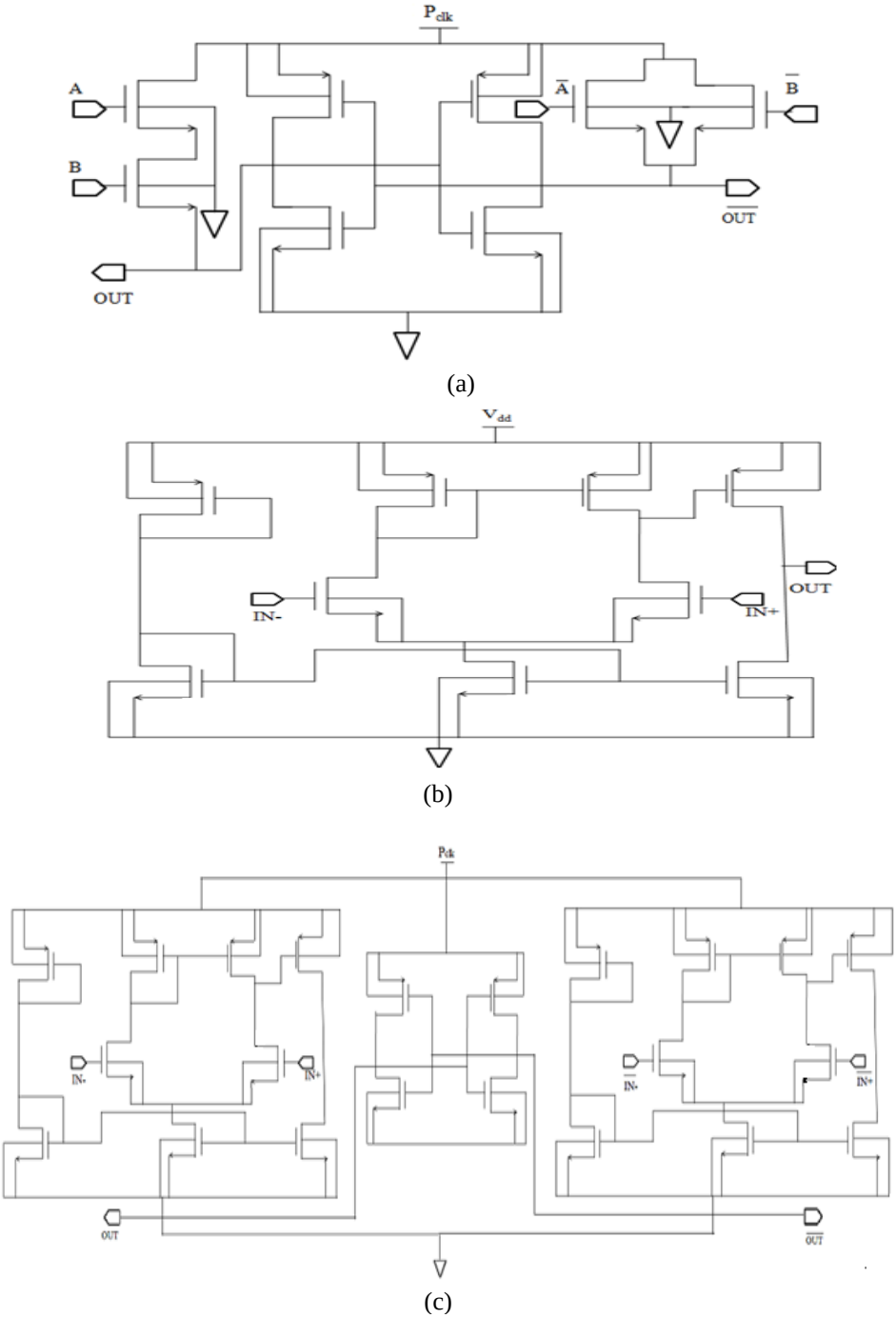


Figure 7. Schematic of 2-bit ADC



(a)

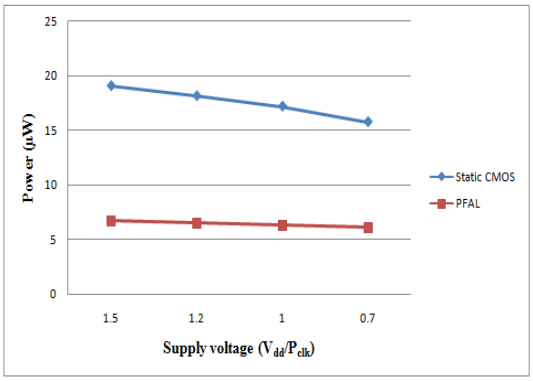
(b)

(c)

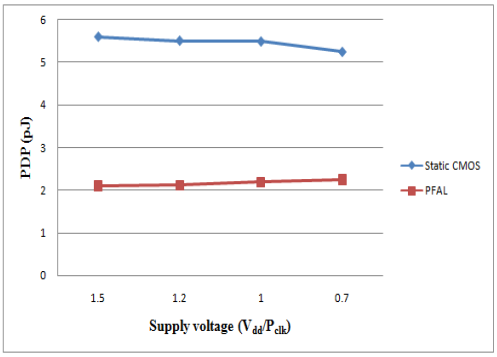
Figure 8. Schematics of (a) PFAL NAND, (b) CMOS comparator, and (c) PFAL comparator

IV. SIMULATION RESULTS

The ECG data acquisition system implemented using static CMOS and PFAL is simulated with Mentor Graphics tool using 130 nm technology node. The power consumption, delay, and power-delay product (PDP) are estimated at various supply voltages. Fig. 9 shows the variation of power and PDP with supply voltage scaling for both the systems. A marginal decrease in power consumption and PDP is observed for static CMOS system when supply voltage is scaled from 1.5 V to 0.7 V, whereas these are almost constant for PFAL system. Table 2 summarizes the values of power consumption and PDP for various supply voltages for an input voltage of 2.5 mV and frequency of 20 Hz. The ECG data acquisition system designed using PFAL offers a reduction of 63.2% in power consumption and 60.08% in PDP as compared to static CMOS implementation at 1 V supply voltage. Thus, the use of PFAL logic greatly reduces the power consumption.



(a)



(b)

Figure 9. Effect of supply voltage scaling on (a) power consumption and (b) PDP of static CMOS and PFAL ECG data acquisition systems

Table 2. Comparison of ECG data acquisition system in static CMOS and PFAL circuits for different supply voltages (input voltage = 2.5 mV and f = 20 Hz)

Supply Voltage V_{dd}/P_{clk} (V)	Static CMOS			PFAL			Percent reduction with PFAL	
	Power (µW)	Delay (ns)	PDP (pJ)	Power (µW)	Delay (ns)	PDP (pJ)	Power	PDP
1.5	19.074	293.81	5.604	6.719	313.54	2.106	64.7	62.41
1.2	18.163	303.42	5.510	6.518	325.60	2.122	64.1	61.48
1.0	17.205	319.16	5.491	6.326	346.57	2.192	63.2	60.08
0.7	15.780	332.42	5.245	6.121	367.71	2.250	61.2	57.10

To verify the effectiveness of PFAL logic in providing security against DPA attacks, current traces are observed for a power clock signal of 1V amplitude and 20 Hz frequency. Fig.10 illustrates the current traces obtained for the PFAL system. The uniform peak current traces indicate increased resistance of the circuit against DPA attacks.

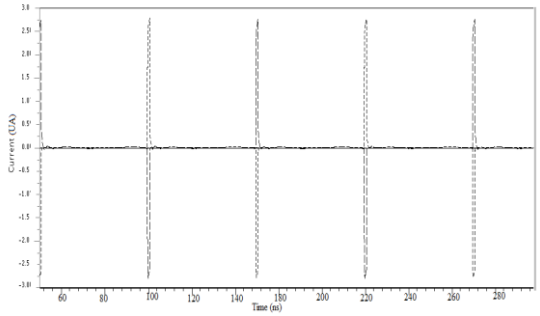


Figure 10. Current traces of PFAL ECG data acquisition system

V. CONCLUSION

ECG data acquisition system was implemented using static CMOS and PFAL logic. Simulations carried out using Mentor Graphics tool at 130 nm indicate a power and PDP reduction of about 63% and 60% respectively with PFAL as compared to static CMOS. The uniform current peaks with PFAL indicate the increased resistance of these circuits against DPA attacks. The PFAL implementation therefore offers ultralow-power and secure communication for IoT based biomedical and other applications.

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