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Design Analysis of Full Adder using Cascade Voltage Switch Logic

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ABSTRACT:
This paper depicts a new design for full adderwith the help of cascade voltage switch logic. Like subtractors we can say adders are also used as basic building block because it is used for all the functional units of microprocessors and digital signal processors. In this modern world of nanotechnology, it is very obvious to designtechniquewhich helps in reduction of area and power consumption. CVSL is a modern technique who meets requirement i.e. high density with minimum delay. The circuit is configurated at 45nm technology and compared with standard cell full adder (45nm technology). Then, circuit comparison on the basis of different parameters is done.

Keywords -Circuit Simulation, CMOSFET Circuits, CVSL, Full Adder.

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I. INTRODUCTION

Adders also known as summers are one of the most used logic components used in the design of VLSI circuits. Summationis commonly used arithmetic logic operation. Adders and subtractor are designed by same methodologies. Summer or Adder in digital electronics, a name represents, circuit in which output depends on addition of two inputs [1]. Apart from its basic function i.e. summation, the adderused for many complex circuits like the multiplexers, encoders, to RAMs, address basic calculations and etc. There are mainlytwo types of adders: Fulladder and Halfadder. The half adder is the simple combinational type of adderwhich used to perform basic addition of two input bits. Itgenerates two outputs, sum and carry. The Full-adder isthe complex combinational type of summation circuit [2]. It involves three input bits, two normal input bits along with carry as third input. It generates two outputs, sum and carry out. The difference between these two types of adders is that the halfadder uses 2 inputs whereas full adder uses 3 inputs. This paper deals in the study of full adder. The logic gates which are required to form full adder are XOR, AND gates and OR gate [3]. Full adder can also be made up of using nine (9) NAND gates. A full adder can also be constructed using two half adders**.** The digital circuits who performs subtraction or addition, full adder remains centre to those circuits. In layman terms, full adder plays very vital role in performing any digital circuitry**.**In the figure shown below, A, B and Cinare input, where A and B are operands to be added, and Cinis the carry bit.Thelogic gate arrangement and truth table for full subtractor is as shown in Figure 1 and Table1 respectively [4].

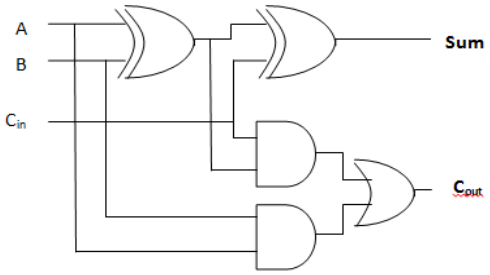

Figure 1:BasicFull Adder

Table1: Truth Table function for Full Adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	0	1	1	1

The sum equation is,

$SUM = A \oplus B \oplus C_{in}$
The carry equation is,

$CARRY\ (C_{out}) = A.B + (C_{in} . (A \oplus B))$

Full adders are mainly used for Arithmetic logic unit (ALU) in computers to perform addition& GPU for the graphics applications to decrease the circuit complexity [5-6].

II. CASCADE VOLTAGE SWITCH LOGIC

The Cascade Voltage Switch Logic an acronym for CVSL. It is a widely used logic in the design of logic circuits wherein we get 2 outputs for a given input [7]. The cascade voltage switch logic is a type of logic circuit in which two types of input is required true and compliment. In its designing 2complimentary NMOS structures are designed and then attached to a pair of cross-coupled pull-up PMOS transistors [8]. There are to type of CVSL circuit fabricated static and clocked. The cascade voltage switch logic has two nodes instead of one for each gate, which results in high tolerance. The basic gate level CVSL design is shown below in figure 2 [9-10].

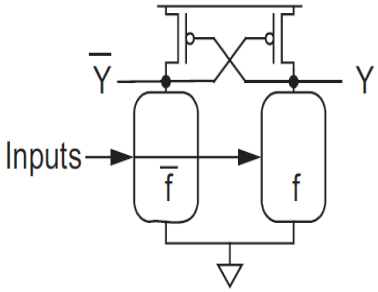

Figure 2: CVSL Circuit

Working of above circuit is shown below:

1. For any input, one of the networks(pull down) will be ON and the other will remain OFF.
2. The network which is ON will generate LOW output. The low output helps to turn ON the PMOS- transistor to generate opposite output high [11].
3. The opposite high output, turns the other PMOS transistor OFF so no static power dissipation occurs [12].

For basic understanding, CVSL implementation with NOR or OR logic is shown below in figure 3 below with a voltage source V_{dd} applied to it. The logic is generated between two inputs A & B and the output is generated for OR and NOR logic at terminal A' and B' [13-14].

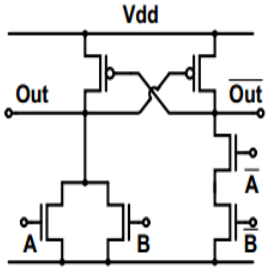

Figure 3 : OR/NOR implementatuion in CVSL

III. CVSL DESIGNS

The configuration and inference of the full adder is done using the CVSL (cascade voltage switch logic) in CADENCE software. The schematic is constructed using 45nm technology. The full adderlogic output is obtained.The schematic for the standard gpdk 45 nm CMOS based Full adder is as shown below in figure 4.

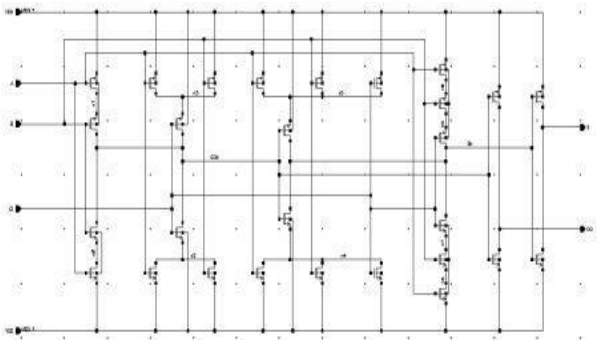

Figure 4: Full Adder with 45nm technology

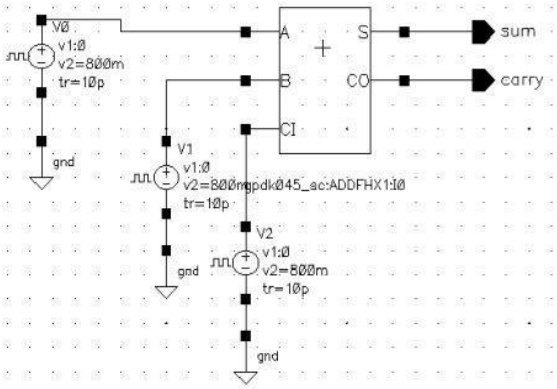

Figure 5: Biased Full Adder

On the basis of CVSL full adder using 45 nm technology is shown below in figure 6.

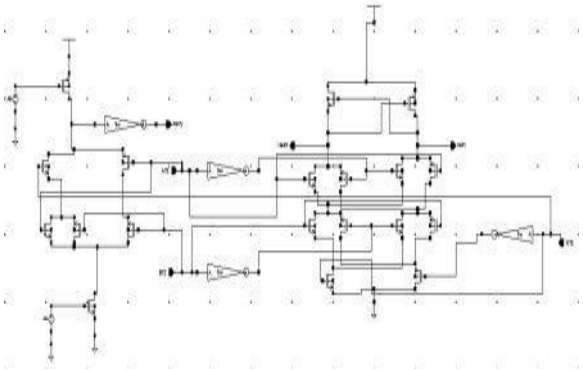

Figure 6: CVSL based Full Adder

IV. RESULT SIMULATION

The output waveforms of the normal adder and CVSL based Full adder design are done using same standard i.e. 45nm to maintain symmetry. The waveforms obtained for normal adder is shown below in figure 5.

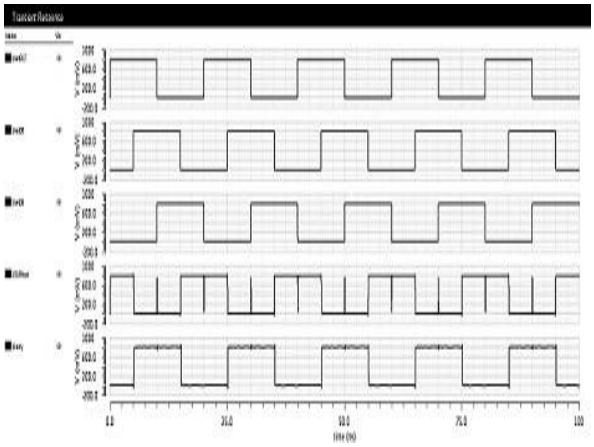

Figure 5: Full adder Output Waveform in 45nm

The CVSL based full adder waveform is shown in figure 6.

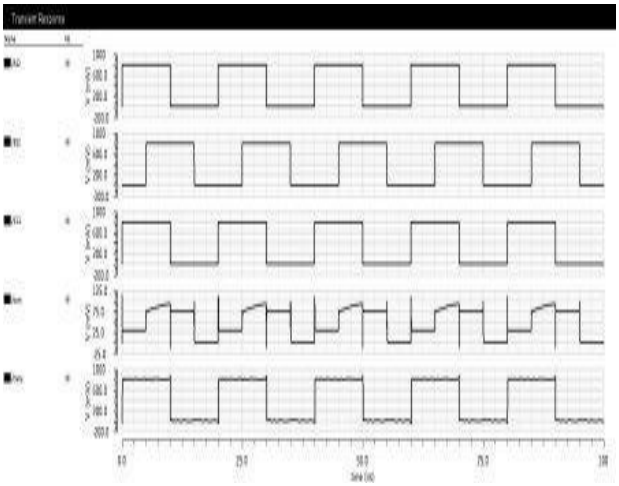

Figure 6: CVSL based Full adder output waveform

Above described, adderwas designed,and analysis was done and both deigned are compared below depending upon two most important parameters. Parameters are power consumption; number of transistors and propagation delay are counted. The comparison is shown below in the Table 2.

Table 2: Parameter Comparison for Full Adder.

Circuit	**Power consumption (nW)**	**Propagation Delay (ns)**	**Transistor Count**
Conventional Full Adder	15.63	110.0 ns	29
CVSL Full Adder	18.942	67.22S	27

V. CONCLUSION

From the design and analysis done for the standard and CVSL based design of Full Adder, it has been studied that the CVSL based design provided much less Power consumption whose value for CVSL design is 18.943nW which is much less than 24.146nW, being the power consumption of conventional design. In addition, the delay time during simulation is only 67.22ns, which is also much better than conventional design delay, whichis 110 ns. Thus, the CVSL design is a better choice for the efficient design of Full Adder for use in complex circuit design.

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