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Verification of HDMI Protocol using SystemVerilog and Universal Verification Methodology (UVM)

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ABSTRACT
High-Définition MultiMedia Interface is an alternate digital video standard over analog video standards. HDMI is mainly used in real time applications for transmitting and receiving audio-video signals. Based on TMDS codec algorithm HDMI transmitter and receiver are designed. This paper proposed a framework for building a enhanceable vérification environnent. The proposed Testplan is based on Universal Verification Methodology (UVM), where testplan is designed according to specifications. The scale of integrated circuit and its complex designs expanding the verification process structure and also time consuming. This work mainly focus on the System Verilog and UVM based verification of HDMI Protocol according to the design verification plan, prepared only after a deep analysis of HDMI functional specifications. The testbench in UVM generates random vectors, the testbench also validates and verifies the characteristic features of HDMI, by running all the test cases and coverage reports progressively at the end of each test. The simulation results are analyzed to estimate and evaluate the effectiveness of the proposed testbench.

Keywords – Coverage**,**HDMI Protocol, Sytemverilog, TMDS,UVM.

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I. INTRODUCTION

Modern development of Technology, now a days electronic display gadgets plays a very important role in our daily life [3]. The audio-video interface is mostly prefered, where HDMI is an audio-video interface is used for professional applications and also send video-audio signals from televisions to computer monitors and home entertainment products to laptop displays. The performance of the HDMI interface is described by the very high data rates and data transferred between these units such as home television and theatre systems. HDMI is not only prefered for the datarates and also the clear and fluent images in display equipments are required by the consumers[2]. In the display high resolution images with high speed of sending and receiving of signals are demanded with quality. Coming to digital display equipments,several digital transmission interface standards have been launched on dailybasis. Among them, HDMI interface protocol is highly accepted choice due to its dense outlook, high transmission speed, and it capability of transmitting the data simultaneously on a single transmission channel, so it gives a better application effect. HDMI and DisplayPort interfaces are most prefered in consumer electronics[4]. However, designing and verifying such HDMI interfaces introduces a challenge. For example, the verification of video protocols requires the capacity to deal with enormous video frames at different stages of protocol layers in multiple streams . The verification target aim is to reduce test run-time and memory consumption of devices, while verifying the DUT design at different levels of blocks, subsystems and at SoC levels. To summarize the verification difficultives of High Definition Television (HDTV) SoCs at each levels. Looking into the verification aspects, System Verilog is the most industry's first unified Hardware Description and Verification Language[1].

System Verilog is used in developing an environment for the HDMI protocol, where System Verilog is most widely used to specify, design and implementing complex digital systems. Traditional verification methods involves writing a testbench in verilog language by driving stimulus to them, but as the design complexity increases the verification methods has insufficient to verify the digital chips. System Verilog has many advanced features which helps in developing flexible potential verification environment, but still a standardized, verification approach can be done by implementing the UVM (Universal Verification Methodology). This verification environment can be reused for many

other IP's also. UVM is a advanced verification methodology that arrange the best practices for the development of verification environments purpose at verifying large gate-count, IP-based SoC's. UVM is mainly used to write a designed test bench for all those designs which are modeled in these languages such as Verilog, VHDL, and C language. It has inbuilt System Verilog class libraries which helps to achieve the reusability.

UVM Methodology supports constrained random coverage for fast driven verification. CDV is a combination of spontaneously generation of all specified test benches, self-observation of test benches,covergroups and coverage metrics. The complexicity of verification process was faced many challenges and dealing with audio and video interfaces, a unified good verification framework choosed for audio and verification environments can be extended. In this paper the related work regarding audio and video interface protocols verification and design was discussed.

II. RELATED WORK

With the available sources and to the tempest of the available knowledge a few attempts have been considered for HDMI Interface Protocol. This paper which is undertaken at present was first brought to mainstream in 2015 and 2016 by Kingston Engineering college open course-ware program in vellore by team of two Assistant professors and they are Mr. C. Srinivasan, Mr. K. ArulOli, and is sponsored by the Department of EEE. The result was estimated regarding the conceptual model of HDMI transmitter by the professors by using high-level object-oriented modeling approach method, they have published article in-depth studies of HDMI and also designed,implemented the HDMI Transmitter and done the transaction level modelling of HDMI Transmitter, based on System Verilog. Completed modeling, and analyzed the principles, algorithms of HDMI Audio and Video data. They have used reusable transaction level model and it supports 32 video formats and 7 audio formats based on types, also works 300% faster than RTL level model. Simulated the design using Model-Sim Software and observed data rates and seperately measured audio and video data. Several developments are taken by individuals at different parts of the world and are being constantly improving the HDMI data rates. At present the Verification of HDMI Transmitter and Receiver which is undertaken as project has several improvements compared to original model, developed by Kingston Instructors [1]. The conventional HDMI interface protocol is verified in both System Verilog and advanced methodology UVM. Improved the datarates, quality of image,video,audio and achieved 100% coverage reports for accurate results was discussed.

III. DESIGN METHODOLOGY

The work here is to achieve the high speed data transmission between source and sink of HDMI Protocol using System Verilog, then verifying the design using UVM method. Developing a reusable and expandable verification framework for HDMI and it is also applicable for different audio and video display interface protocols. The purpose of this paper is mainly on designing the DUT code for HDMI Transmitter and Reciever according to design specifications and also creating Test Bench Environment and apply a advanced UVM Methodology to verify the Functionality of HDMI Protcols and also generating the Coverage,UVM Reports. UVM Phases provides full control over the period of simulation where behavior is in a systematic way and execute in sequential order to avoid jitter conditions.

A. OBJECTIVES

The main aim of this paper is listed below:

- Increase the frame rate(throughput) at the transmission side, that improves the data speed.
- Also Improves the Video and Audio quality of images/Video signals.
- Reduce the short time to market problem.
- Implementation of Test-benches for both the HDMI Transmitter and Receiver.
- To understand, the development of verification environment for HDMI transmitter and receiver using UVM methodology. UVM methodology mainly includes the TestPlan Framework along with the configuration of driver, sequencer and monitor.

B. HDMI (HIGH DEFINITION MULTIMEDIA INTERFACE)

HDMI interface consists of a transmitter, a receiver, and a data output channel, all of three components establishes the signal encoding, transmission and decoding of image,audio and video signals.The three components contains several modules, such as TMDS codec module, HDCP module, DDC unit, CEC and EDID modules. The below Fig. 1 shows the HDMI block diagram with all functional blocks.The HDMI carried a three more signals like Display Data Channel (DDC),Video Electronics Standards Association (VESA) and final one Status and Control Data Channel (SCDC) signals these are the additional features. The DDC

configures and status exchange information between source and sink. The DDC signal is used by source to read the Enhanced Extended Display IdentificationData (E-EDID) signal information of sink to exposed the sink's configuration details and capabilities. The SCDC always supports the sink's read requests from the receiving end.

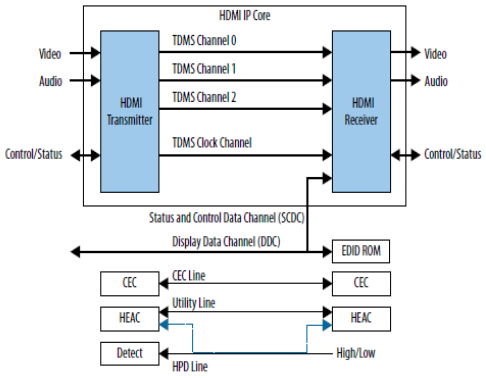

Fig.1. HDMI Block Diagram

The optional signal Consumer Electronics Control (CEC) protocol gives high-level control functions between various audio video gadgets. The optional signal HDMI Ethernet and Audio Return Channel (HEAC) provides the Ethernet suitable data networking between any connected devices and the audio return channel is working in the opposite direction of TMDS channels. The HEAC signal took the help of Hot-Plug Detect (HPD) line for signal transmission to sink. The below Fig. 2 shows the TMDS System with all functional blocks.

An HDMI interface contains three color channels with single clock channel. We can use each colour lines to transfer both auxiliary data and RGB colours individually.The receiver end used the reference frequency of TMDS clock for data recovery and restore on the three TMDS data channels respectively**.** An HDMI interface contains three color channels with single clock channel. We can use each colour lines to transfer both auxiliary data and RGB colours individually.The receiver end used the reference frequency of TMDS clock for data recovery and restore on the three TMDS data channels respectively.

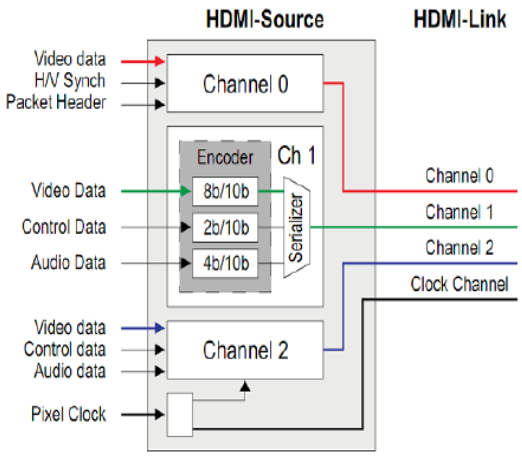

Fig. 2. TMDS system

This clock typically runs at the video pixel rate at high speed. The encoding of TMDS is provided with an 8-bit to 10-bit algorithm depends on modes. This protocol trying to minimize data channel transmission and also maintains the sufficient bandwidth so that a sink device at the receiving end can lock reliably to the stream of data.

HDMI interface contains audio-video data, and control signals, where the auxiliary signal, another name field or line synchronizing signal are encoded according to functional specifications and these signals are transmitted by HDMI transmitter. In data transmission block, data is transmitted to the receiver end by three ways of TMDS(Transition Minimized Differential Signaling) codec scheme and one TMDS clock channel scheme. Each video pixels can be constitutes using 24-bit, 30-bit or 36-bit data. In practical transmission frequency of video data is 165 MHZ and audio data frequency is192 KHz.

The below Fig. 4 shows the two data streams:

- Data stream in green colour-- It transports the color data.
- Data stream in dark blue colour--it transports the auxiliary data.

Auxiliary data transfers the audio data together with a same range of auxiliary data packets. The auxiliary data packets used by sink devices to reconstruct the video and audio data accurately. TMDS Error Reduction Coding–4 (TERC4) bits encoding algorithm is most prefered. Each one of the data stream section is associated with guard bands and pre-ambles. The guard bands and pre-ambles are allowed to receive the data streams with accurate synchronization.

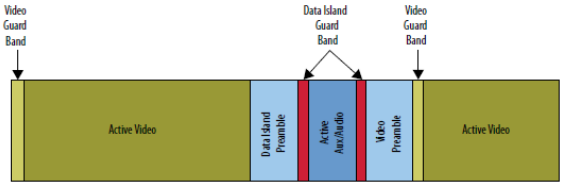

Fig. 3. HDMI Video Stream Data

The below Fig. 4 shows the TMDS Period video frame with all functional modes. HDMI has three types of different TMDS operating modes namely:

a. Video Data Period -- The active pixels of an active video line is transmitted over channel.

b. Data Island Period -- The series of packets containing audio and auxiliary data is transmitted over channel.

c. Control period -- This period is used when no video, audio or auxiliary data information needs to be transferred.

Fig. 4. TMDS periods in 720x480p video frame.

The availability of several regression Test suites applied to HDMI interface and also provide complete solution for the easy integration of IP and SoC environments. HDMI is a very high-speed, multi channel serial data, digital signaling transmission system that is mainly designed to transmit enormous amounts of digital data over a cable. HDMI also incorporates with scrambling and TMDS encoding of digital data to reduce interfernces like electromagnetic interference (EMI) and radio frequency interference (RFI) when it comes to practical implementation. HDMI features such as Framing, TMDS encoding, scrambling, error character detection and correction. The following below Fig. 5 and Fig. 6 shows the order wise arrangement of the video data enable,video data, video H-SYNC signal, and video V-SYNC pulses in the order of 1, 2, and 4 symbols per clock.

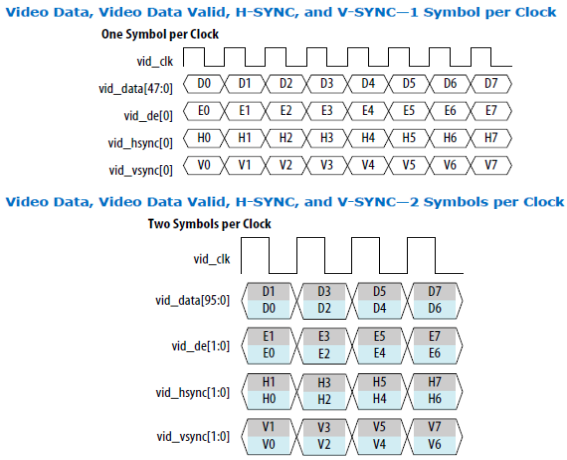

Fig. 5. Video Data, Video Data Valid, H-SYNC, and V-SYNC- 1 and 2 Symbols per Clock

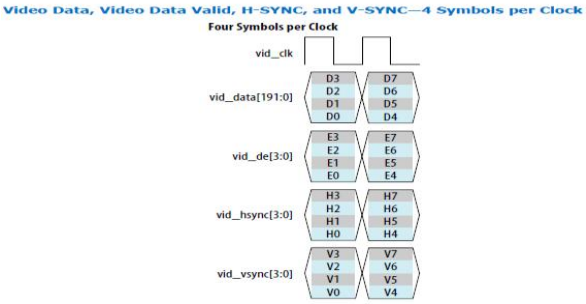

Fig. 6. Video Data, Video Data Valid, H-SYNC, and V-SYNC- 4 Symbols per Clock

The Table. 1 shows the video formats along with various colour depth width. Standard preferd is RGB format.

Table.1. Color Depth Supported for Each Video Format

Video Format	Color Depth			
	8	10	12	16
RGB	Yes	Yes	Yes	Yes
YCbCr 4:4:4	Yes	Yes	Yes	Yes
YCbCr 4:2:2[1]	Not applicable	Not applicable	Yes	Not applicable
YCbCr 4:2:0	Yes	Yes	Yes	Yes

The below Fig. 7 and Fig. 8 shows the RGB color space pixel format for bit-field mappings. The first pixel for any given line of video contains R,G and B components are transferred on the video data period for the first pixel following the Guard Band characters is determined.

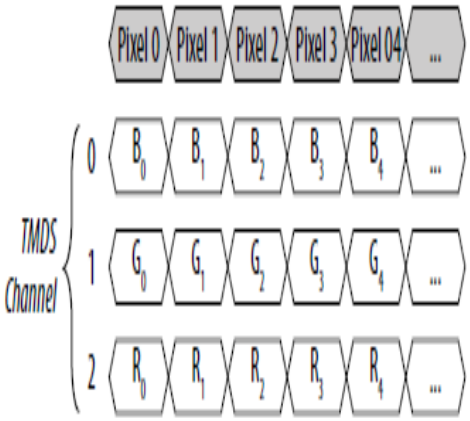

Fig. 7. RGB 4:4:4 Mapped to the Respective TMDS Channels

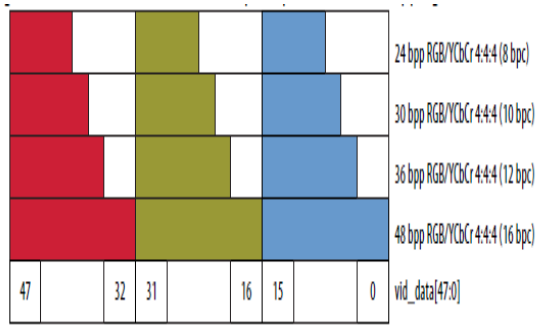

Fig. 8. Source Pixel Data Input Format RGB/YCbCr 4:4:4

The following Table. 2 shows the lists of Source General Control Packet port controllable bit-fields. All other fields of the GCP, where packing of the total pixels is automatically calculated.

Table. 2. General Control Packet Input Fields

Bit Field	Name	Comment				
gcp[3:0]	Color Depth (CD)	CD3	CD2	CD1	CD0	Color depth
		0	0	0	0	Color depth not indicated
		0	0	0	1	Reserved
		0	0	1	0	Reserved
		0	0	1	1	Reserved
		0	1	0	0	8 bpc or 24 bits per pixel (bpp)
		0	1	0	1	10 bpc or 30 bpp
		0	1	1	0	12 bpc or 36 bpp
		0	1	1	1	16 bpc or 48 bpp
		1	1	1	1	Reserved

We must provide the bit-field value in the table. The auxiliary data port of GCP will always be filtered. Table. 3 shows the vendor specific InfoFrame Bit-Fields where HDMI Vendor Specific InfoFrame is once per field.

Table. 3. HDMI Vendor Specific InfoFrame Bit-Fields

Bit-field	Name	Comment
4:0	Length	Length = Nv
12:5	Checksum	Checksum
36:13	IEEE	24-bit IEEE registration identified (0x000C03)
41:37	Reserved	All 0
44:42	HDMI_Video_Format	HDMI video format
52:45	HDMI_VIC	HDMI proprietary video format identification code
57:53	Reserved	All 0
60:58	3D_Ext_Data	3D extended data
61	Control	Disables the core from inserting the InfoFrame packet.

IV. VERIFICATION METHODOLOGY

The Verification plays a most important role in the VLSI technology. Since it is effectively utilized to finding out the bugs in the RTL design, so the overall design should not prove destructive at the initial stages itself. So here we are developing an HDMI protocol design verification environment in System Verilog and UVM methodology. The main aim of developing the verification environment is stimulus generation to the DUT (design under test), and check out the results properly to verify the functionality test according to specifications whether it is correct or not. So that generating the test cases with all possible ways and it can be modified by refering the functional coverage reports. System Verilog is a flexible hardware verification language and this can be used in functional,code verification. It is mainly used to provide the high level data structures available and some features in object-oriented languages. These data structures may enable a higher abstraction level and modeling of complex data types. The System Verilog has inbuilt features like constructs necessary for modeling hardware concepts such as logic,cycles, tri-state values, wires, just like Verilog hardware languages. The below Fig. 9 shows the system verilog verification environment with Stimulus, Driver, Scoreboard, Monitor, Interface and Design under Test Module.

Generator: It is used to generate different input stimulus from the base packet generator , that to be supplied to DUT and at transaction level data transfers takes place, which can be defined by generator.

Driver: It is a component where repeatedly takes place all transactions from the generator and then it drives on to DUT through the interface by transfering the signal to transaction level on to the interconnect.

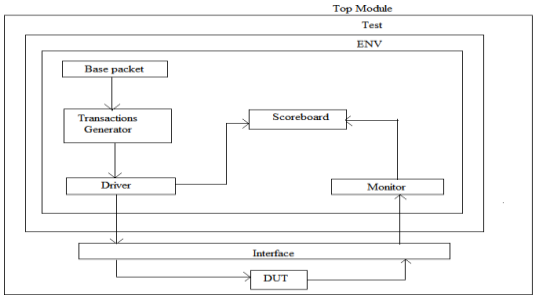

Fig. 9. System Verilog Verification Environment

Interface: It has all the complete design signals that can be completely monitored.
Monitor: It Is mainly used to monitoring input-output ports designs in order to capture activity of complete design.
Scoreboard: It is a test bench component of environment which has to check the accuracy of DUT design. It takes the actual results from DUT and compare with expected results of DUT.
The environment is a body container or house which has class for grouping all higher level components such as the Generator, Driver, Monitor, Interface, Basepacket and scoreboard.
The BasePacket is the actual input and DUT is the actual design and also Test is responsible for test bench configuring also initiate all the test bench components driving stimulus to initiate the construction process of components.
Verification Flow details:
(i)All features listing down.
(ii)All possible scenarios listing down.
(iii)Development of TestPlan.
(iv)Listed the functional coverage points .
(v)Definition of Test-bench architecture.
(vi)Complete Test-bench component coding.
(vii)Complete regression results.
(viii)Coverage results generation.
(ix) Coverage results has to analyze.
(x) Functional Coverage end.

V. SIMULATION RESULTS

This section deals with an insight about the simulation results of the Design Under Test of HDMI Interface protocol for both audio and video transmission. The DUT is also interfaced with all test bench environment modules such as generator module, interface module, driver module and monitor modules in order to obtain the effective verification performance. The HDMI Interface is modeled using System Verilog. After integration with the top module under Design Under Verification, the simulation is carried out and using Mentor Graphics QuestaSim 10.4e simulator tool.

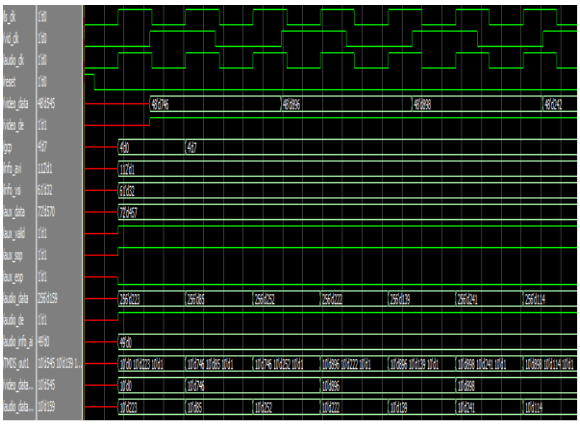
Fig. 10. HDMI audio and video transmission with TMDS

The above Fig. 10 shows the HDMI audio and video transmission of the transmitter and the receiver is as as shown, randomly generating the 256 bits of audio data and 48 bits of video data. The audio and video signals are sending to receiver based on video and audio enable. All signals are controlled by main clock. Audio clk frequency and video clock frequency both are same, but video clock frequency is half of the main clock frequency. GCP data field is configured to 0111 because of 48 bits per pixel for video data. When start of packet is high then transmitter send the packets and when end of packet is high then receiver accepted the last packet after that end of packet is set to low. When valid bit is high then only video and audio is combined at the TMDS channel, where TMDS channel contains audio data,video data and also auxiliary information, the aux data information is needed for frame synchronization and finally the data sent to receiving end without any delay so this achieves speed of data transmission. When it comes to practical implementation the quality of image,video,audio are improved. Error correction module is designed in verification environment to achieve a highly accurate results with minimum delay,frame rate gets increased. The below Fig. 11 shows the simulation results of HDMI Transmitter before encoding, it is just verifying at the transmission side. Based on control signals co and c1 the video and audio data get transferred to channel without encoding and it may contains junk data with delay.

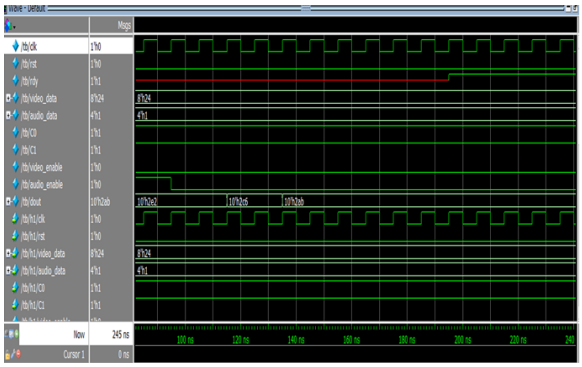

Fig. 11. Simulation Of HDMI Transmitter output before Encoding

The below Fig. 12 shows the simulation results of HDMI receiver with advanced decoding method where, separately compared all intermediate signals of audio and video data along with the auxiliary information and verified the received data according to the functional specifications. TMDS decodec method applied at the sink to enhance the security of the data and synchronization is achieved.

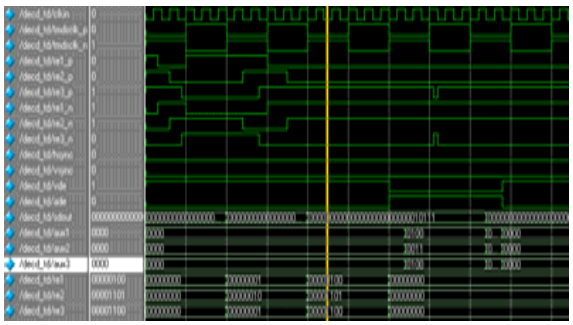

Fig. 12. Simulation of HDMI Receiver with advanced decoding method

The below Fig. 13 and Fig. 14 shows the transcript window outputs for both video data and audio data matched and unmatched conditions. If the audio data input is same as audio data output but the video data input is not same as video data output, then it becomes data unmatched.

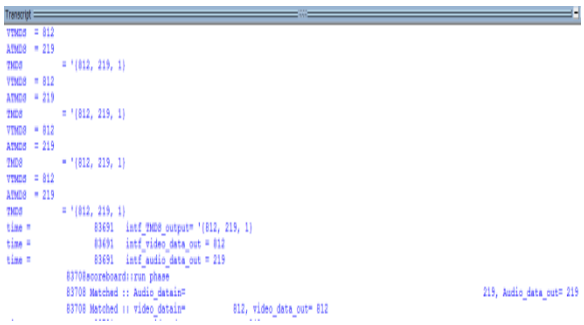

Fig. 13. Transcript window output for data matched

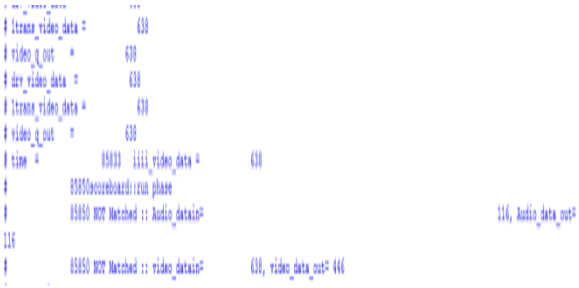

Fig. 14. Transcript window output for data not matched

Audio data depends on video data, video datain is same as video dataout and audio datain is same as audio dataout then it becomes matched. Since highly verified data in scoreboard has stored and same is displayed in transcript window. Covergroup results is as shown in Fig. 15, verification achieves a functional coverage of 94%. Finally coverage is achieved by covergroups and bins.

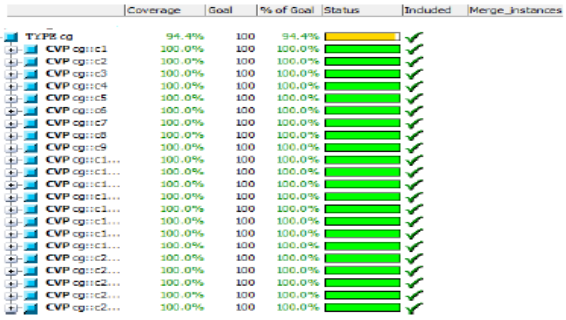

Fig. 15. Covergroup Report

The below Fig. 16 shows the UVM data error summary where errors are reduced to zero and all test cases are checked.

```
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :32484332
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [RNTST]     1
# [TEST_DONE]     1
# [TIMOUTSET]     1
# [UVMTOP]     1
```

Fig. 16. UVM Data Error Summary

VI. CONCLUSION

In this paper, verification of HDMI Interface protocol is done using System Verilog and UVM methodology and also implemented the test bench environment successfully. UVM verification

approach trying to cover all possible bugs, that occur during verification, also the framerates of data is significantly increased. Cross functional coverage using UVM and coverage report . 100% code coverge for functional specifications. Verified the actual results of the audio data and video data with the expected results and also generated the coverage report. Using System Verilog for verification total verification time gets reduced. According to functional specifications all test cases executed and verification plan framework can be reuse for future use. Improved the speed by reusable verification IP,Protocol analyzer and reusable stimulus coverage models and also overall reusable verification IP of HDMI functionality is designed and verified using System Verilog and UVM Methodology.

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