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RESEARCH ARTICLE OPEN ACCESS

Single-Phase Switched-Capacitor Based Multilevel Boost Inverter Topology with Reduced Voltage Stress

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ABSTRACT:
The growth of renewable energy resources in high voltage applications like electric vehicle, HVDC, industrial drive, etc., power electronic converters play an important role in the power conversion suitable for each application. Multilevel inverters have their importance in medium and high voltage applications. A Single-Phase Switched-Capacitor Based Multi- level Boost Inverter Topology with Reduced Voltage Stress is proposed. Apart from the increased voltage gain, self-voltage balancing of the capacitor without any auxiliary method along with reduced voltage stress has been the main advantages of this topology. The comparative study of various Pulse Width Modulation (PWM) techniques used in the inverter and their performance factors were analyzed with MATLAB/SIMULINK. The proposed inverter has an output THD of 7.74% using Fixed Frequency Modulation (FFM) compared to other control strategies and provides an efficiency of 97.8%. The output voltage levels can be varied by varying the switching sequence and also by extending the unit cell.
Index Terms—Multilevel inverter, self balancing , modulation techniques

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I. INTRODUCTION

Renewable energy sources have enormous promises over fossil energy sources. But utilization of these sources is relatively limited due to the sub-optimal power generation capacity, cost, and space requirement. These limitations are highly subjected to the efficiency and structure of the inverter of a renewable energy system. Therefore, a substantial amount of inverter designs are reported. Nowadays, multilevel inverters are getting much attention to operate in renewable energy systems because of their low total harmonic distortion (THD) and low voltage stresses on switches, low dv/dt stress, less requirement for filters, and high modularity.

There are three types of conventional multilevel topologies: neutral-point-clamped (NPC) topology, flying capacitor (FC) topology, and cascaded H-bridge (CHB) topology[6]. How- ever, the electric energy from renewable energy sources, such as photovoltaic (PV) arrays and fuel cells, is largely in the form of low voltage, which needs to be transformed to higher ac voltage. One of the traditional solutions is to cascade a frontend dc-dc boost converter with a backend conventional multilevel inverters. Furthermore, auxiliary balance circuits, current and voltage sensors, or complicated control algorithms are needed for keeping the capacitor's voltage balance of NPC and FC topologies. All of these lead to additional complexity and reduced efficiency.

To mitigate these problems, hybrid cascaded multilevel in- verters (HC-MLI) are proposed. Capacitor voltage balancing techniques in HC-MLI are complex when a higher number of voltage levels are generated. Coupled inductor-based mul- tilevel inverters are also used to boost the output voltage. However, the use of bulky inductors increases the cost and size of multilevel inverters. One category of the multilevel inverters topologies has been based on the multiple isolated dc voltage sources. In this category, the topologies have been classified as symmetrical and asymmetrical configured topologies. In symmetrically configured topologies, the dc voltage sources have the same magnitude. In asymmetrically configured topologies, the dc voltage sources have different magnitude resulting in a higher number of levels with a lower number of switches as well as dc voltage sources. In both types of topologies, the need for a higher number of isolated dc voltage sources limits their applications.

To reduce the number of dc voltage sources, the use of topologies with switched

capacitor units have been recom- mended. The switched capacitor unit has been used with different arrangements resulting in different output voltage levels. Switched capacitor units have a distinctive feature of boosting the output voltage, i.e., the peak of the output voltage is higher than the input supply. In this work, a single phase multilevel inverter based on switch-capacitor technique is proposed. The topology has two dc-link capacitors and a switched capacitor for synthesizing various levels. The unique features of the multilevel inverter are:

1. Usage of a single dc source
2. Voltage balancing of the capacitors
3. voltage gain of 3
4. The maximum voltage stress across each switch is equal to input voltage.

II. PROPOSED SWITCHED CAPACITOR MULTILEVEL INVERTER

In the proposed multilevel inverter, thirteen-level inverter is shown in Fig 1 having two dc-link capacitors C , C ,Level $+3V_{dc}/2$: The dc-link capacitor voltage gets added with the switched capacitor voltage by turning on the switches S_2,S_5,S_6,S_8,S_9, S_{11}, S_{12}, S_{13}, S_{14}.

Level $+2V_{dc}$: Through switches S_2,S_3,S_6,S_8,S_9, S_{11}, S_{12}, a switched-capacitor 1 2 S_{13}, S_{14} the dc input voltage gets added with the voltage of C_3,14 unidirectional switches and one bidirectional switch. The dc-link capacitor splits the input voltage into equal half resulting in a voltage of $V_{dc}/2$. The switching patterns for various voltage levels of the proposed multilevel inverter are provided in Table I.

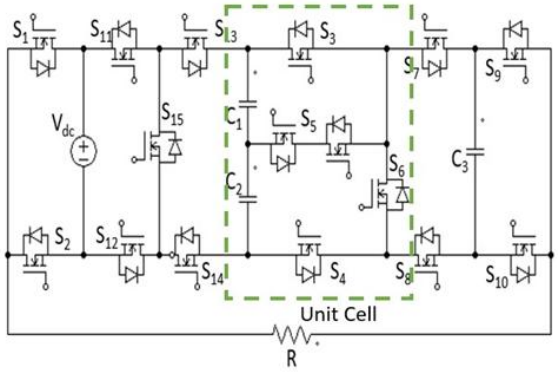

Fig. 1. Proposed multilevel inverter

TABLE I
SWITCHING STATES FOR PROPOSED THIRTEEN LEVEL INVERTER

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}
$+3V_{dc}$	0	1	1	0	0	1	0	1	1	0	1	0	0	1	1
$+2.5V_{dc}$	0	1	0	0	1	1	0	1	1	0	1	0	0	1	1
$+2V_{dc}$	0	1	1	0	0	1	0	1	1	0	1	1	1	1	0
$+1.5V_{dc}$	0	1	0	0	1	1	0	1	1	0	1	1	1	1	0
$+1V_{dc}$	0	1	1	1	0	0	1	1	1	0	1	1	1	1	0
$+0.5V_{dc}$	0	1	0	0	1	0	1	0	1	0	1	1	1	1	0
$0V_{dc}$	0	1	1	1	0	0	1	1	0	1	1	1	1	1	0
$-0.5V_{dc}$	1	0	0	0	1	1	0	1	0	1	1	1	1	1	0
$-1V_{dc}$	1	0	1	1	0	0	1	1	0	1	1	1	1	1	0
$-1.5V_{dc}$	1	0	0	0	1	0	1	0	0	1	1	1	1	1	0
$-2V_{dc}$	1	0	0	1	0	1	1	0	0	1	1	1	1	1	0
$-2.5V_{dc}$	1	0	0	0	1	0	1	0	0	1	0	1	1	0	1
$-3V_{dc}$	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1

A. Analysis of voltage levels

Level zero: In the zero voltage state as in fig 2, switches S_2, S_3, S_4, S_7, S_8, S_{10}, S_{11}, S_{12}, S_{13}, S_{14} are turned on, the capacitors gets connected across the dc voltage source and starts charging.

Level $+V_{dc}/2$: The capacitor link voltage is utilized and the load is connected through switches S_2,S_5,S_7,S_9, S_{11}, S_{12}, S_{13}, S_{14}. The capacitor voltage of C_3 remains unchanged.

Level $+V_{dc}$: In fig 3, the input voltage is applied to the load, also the capacitor is connected in parallel to the dc input voltage through switches S_2,S_3,S_4,,S_7,S_8,S_9, S_{11}, S_{12}, S_{13}, S_{14} to get charged.

the switched capacitor resulting in a voltage level of twice the input voltage as illustrated in fig 4.

Level $+5V_{dc}/2$: The input dc source voltage is connected with a dc-link capacitor voltage and the switched capacitor voltage through switches S_2, S_5, S_6, S_7, S_8, S_{10}, S_{11}, S_{14},
S_{15}.

Level $+3V_{dc}$: In fig 5, The input dc source voltage is connected with a dc link capacitor voltage and the switched capacitor voltage through switches S_2,S_3,S_6, S_8, S_9, S_{11}, S_{14},
S_{15}.

Level $-V_{dc}/2$: In this state, voltage is obtained across the load by utilizing the dc link capacitor voltage through S_1,S_5,S_6,S_8,S_{10}, S_{11}, S_{12}, S_{13}, S_{14}.

Level $-V_{dc}$: For a voltage level of $-1V_{dc}$, the dc voltage source is connected across the load and across the switched capacitor through S_1,S_3,S_4,,S_7,S_8,S_{10}, S_{11}, S_{12}, S_{13}, S_{14} to get charged as shown in fig 6.

Level $-3V_{dc}/2$: Through switches S_1,S_5,,S_7,S_{10}, S_{11}, S_{12}, S_{13}, S_{14} voltage is achieved by adding the dc link capacitor voltage to the switched capacitor voltage.

Level $-2V_{dc}$: Through switches S_1, S_4, S_6, S_7, S_{10}, S_{11}, S_{12}, S_{13}, S_{14} The dc input voltage is added with the voltage of the switched capacitor resulting in a voltage level equal to twice the input voltage depicted in fig 7.

Level -5V_{dc}/2: The input dc source voltage is added with the switched capacitor voltage and a dc link capacitor voltage through S_1, S_3, S_5, S_7, S_{10}, S_{12}, S_{14}, S_{15}. The output results to a voltage equal to twice the applied input voltage.

Level -3V_{dc}: During this voltage state as in fig 8, the input dc source voltage is added with dc link capacitor voltages and switched capacitor voltage through switches S_1,S_4,S_6,S_7,S_{10},S_{12}, S_{13}, S_{15}. The output results to a voltage equal to thrice the applied input voltage.

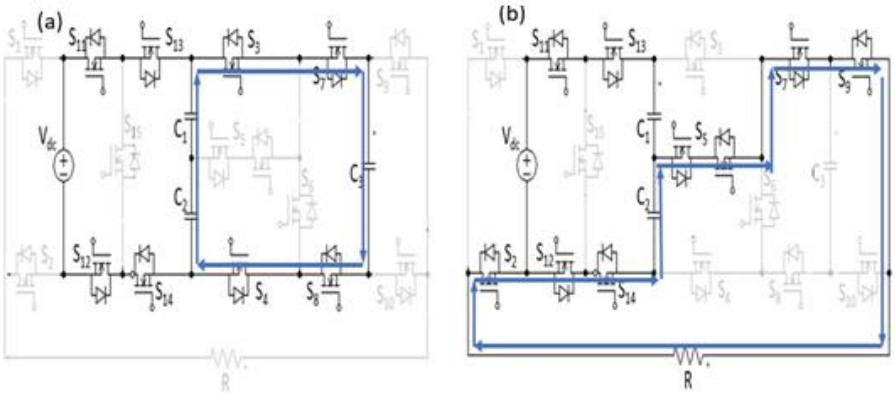

Fig. 2. Mode 1 and Mode 2 Operation

B. Modulation Strategy

For the proposed thirteen-level topology, the Fixed Fre- quency Modulation (FFM) technique has been used. For the FFM fundamental frequency modulation (FFM) methods, the sine wave is compared with the different fixed levels of

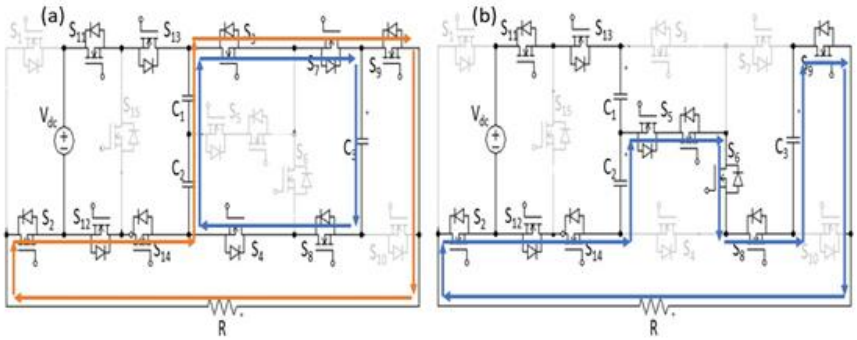

Fig. 3. Mode 3 and Mode 4 Operation

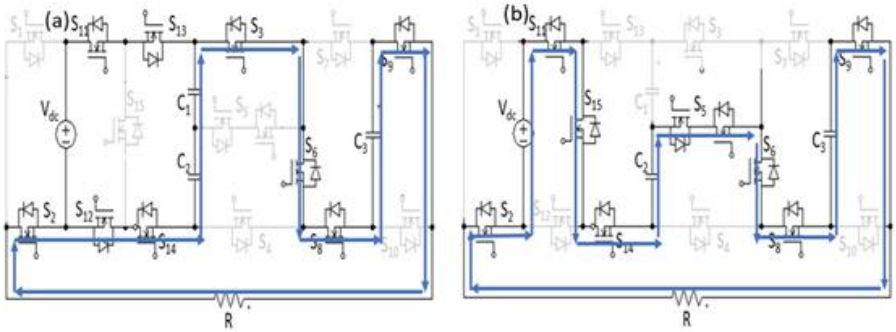

Fig. 4. Mode 5 and Mode 6 Operation

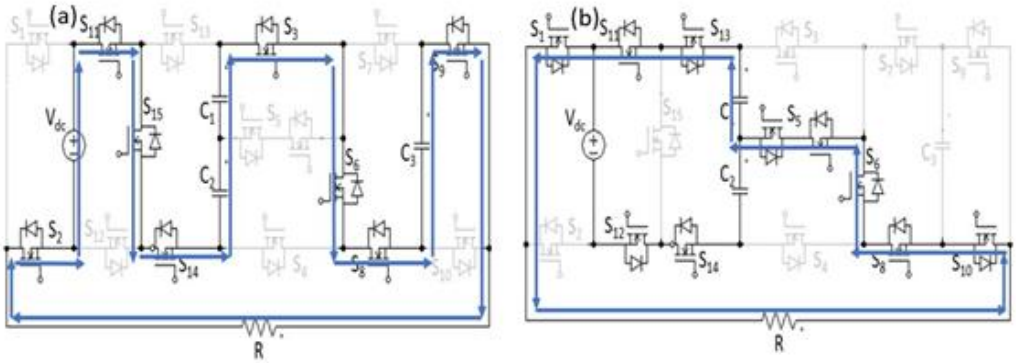

Fig. 5. Mode 7 and Mode 8 Operation

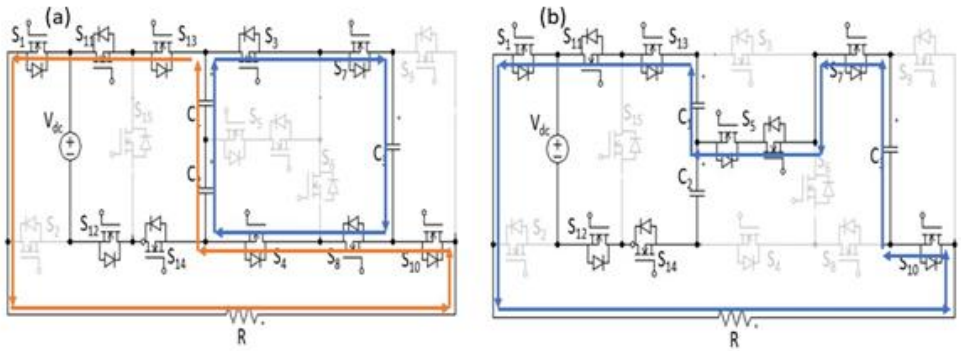

Fig. 6. Mode 9 and Mode 10 Operation

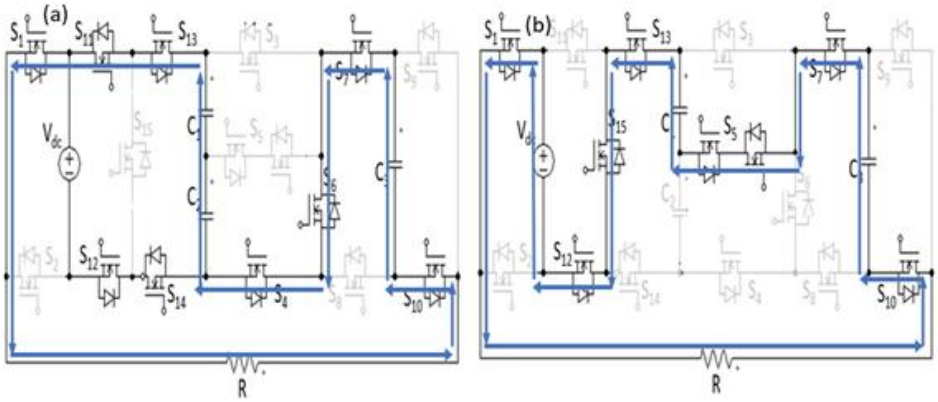

Fig. 7. Mode 11 and Mode 12 Operation

fixed frequency. For N level inverter, (N-1) fixed DC level is required. Hence for the proposed thirteen level inverter, 12

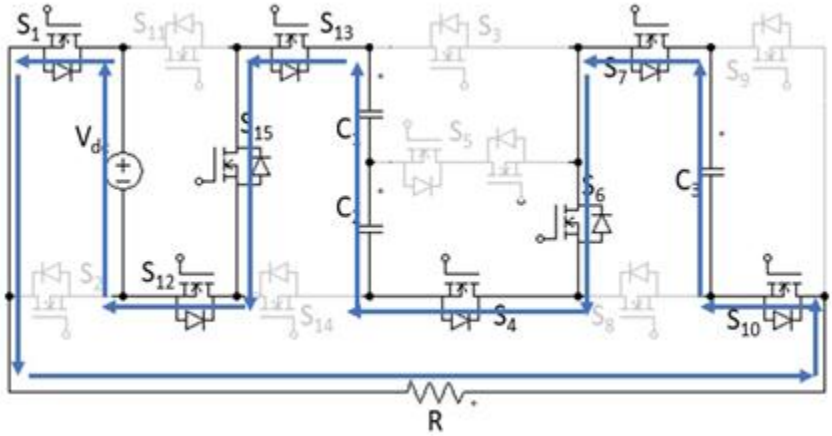

Fig. 8. Mode 13 Operation

fixed DC level is used. It is depicted in Figure 9.

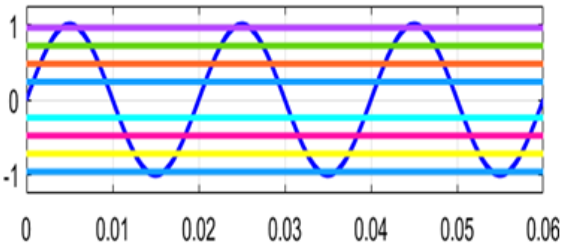

Fig. 9. Fixed Frequency Modulation

III. SIMULATION RESULTS OF PROPOSED INVERTER

The proposed thirteen-level inverter is simulated using MATLAB/SIMULINK with an input of 200V and output is obtained as 600V.

A. Gate Pulse Generation

The gate pulses for the switches are obtained using FFM technique where the modulating signal is compared with twelve constants.

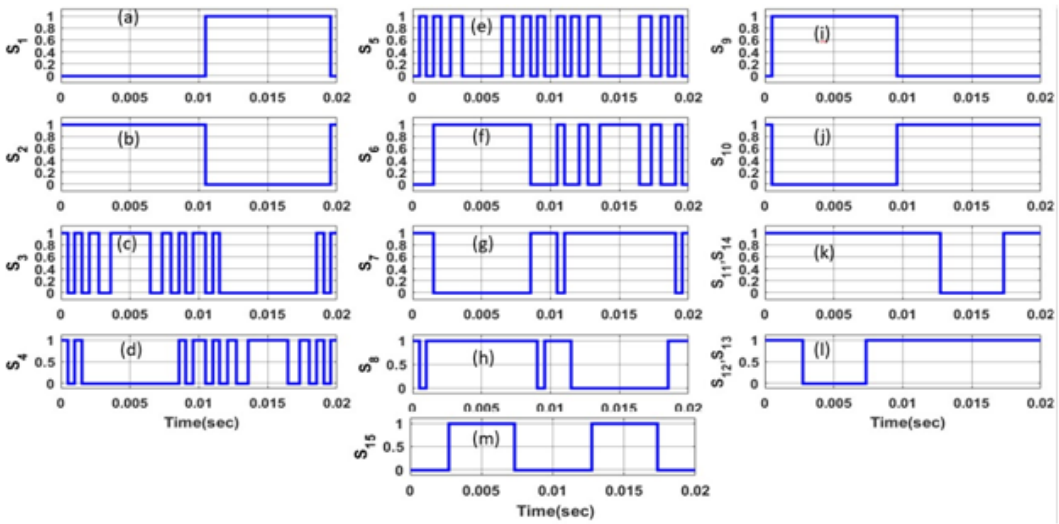

Fig. 10. Gate Pulse Generation of switches (a)S_1, (b)S_2, (c) S_3, (d) S_4,(e) S_5, (f) S_6, (g) S_7, (h) S_8, (i) S_9, (j) S_{10}, (k) S_{11} and S_{14}, (l) S_{12} and S_{13}, (m)S_{15} using FFM

B. Simulation Results

Fig.11 shows the 13 voltage levels and current waveforms for the inverter topology with a resistive load having a Mod- ulation index = 1. This shows a gain of 3.

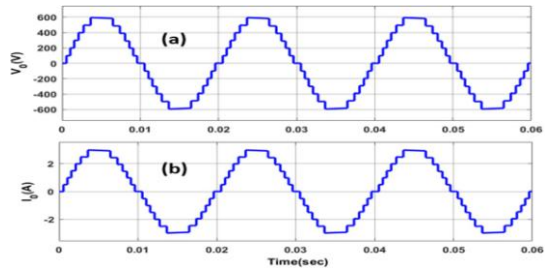

Fig. 11. (a) output voltage and (b) output current for R load

For RL load where R= 200Ω and L = 250mH with M.I = 1, thirteen stepped levels of maximum voltage level of 600V and a current of 2.19A is shown in fig 12.

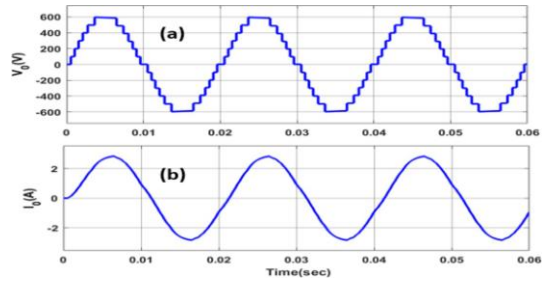

Fig. 12. (a)output voltage and (b) output current for RL load

Capacitor voltage balancing has been one of the important features of the proposed topology. The capacitor C_3 is charged up to V_{dc} during the voltage states of zero and V_{dc}.The dc ink capacitors C_1, C_2 are provided with initial charge of 100V and switched capacitor C_3 to 200V illustrated in fig 13.

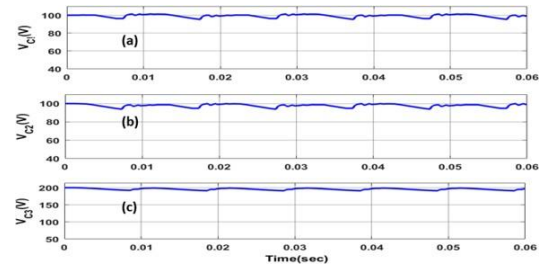

Fig. 13. Capacitor voltages (a) C_1 (b) C_2 (c) C_3

The voltage stress across the switches is shown in fig 14 and 15. Maximum stress across each switch is same as the input voltage

IV. PERFORMANCE ANALYSIS

Analysis from the simulation of the switched capacitor multilevel inverter is done and is obtained as follows:

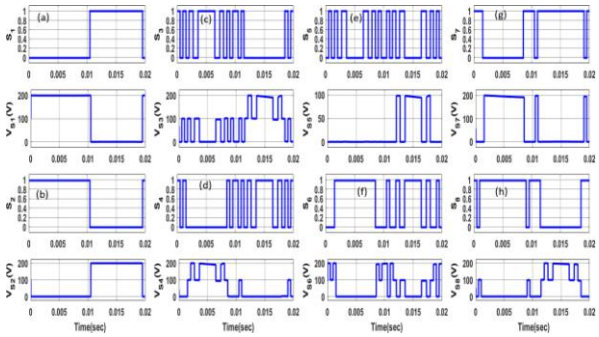

Fig. 14. Gate pulse and voltage stress across switches

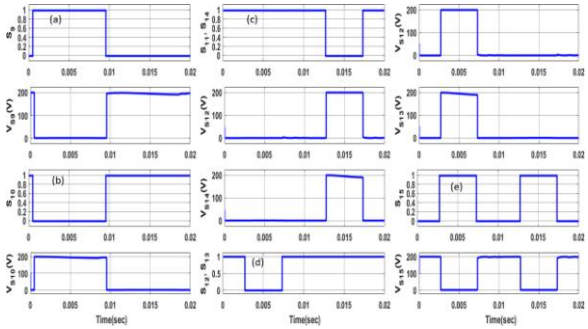

Fig. 15. Gate pulse and voltage stress across switches

A. THD Vs Switching Frequency

Fig 17. shows the THD as a function of switching frequency. Different PWM methods were analyzed for different frequen- cies and at 2 kHz switching frequency it exhibits less THD. For the proposed inverter THD is about 7.74% with the FFM method.

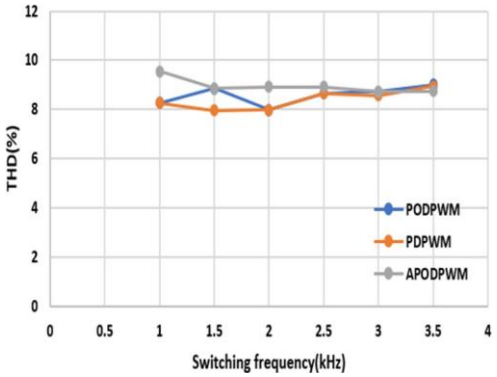

Fig. 16. THD Vs Switching frequency of Proposed Inverter

B. FFT Analysis

The Total Harmonic Distortion (THD) determines the qual- ity of the voltage delivered by an inverter.

FFT analysis is done for various modulation techniques[5].

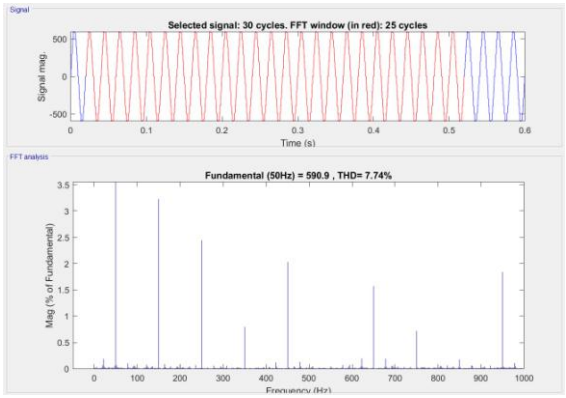

Fig. 17. FFT Analysis of Proposed Inverter wth PDPWM

The control strategy sdopted in the inverter is FFM and THD is about 7.74% as shown in Fig.16. The DC component if the inverter is 0.1462.

C. THD Vs Control Strategies

The % THD for different PWM techniques such as POD- PWM, PDPWM, APODPWM, and FFM proposed inverter respectively is shown in Fig.17.

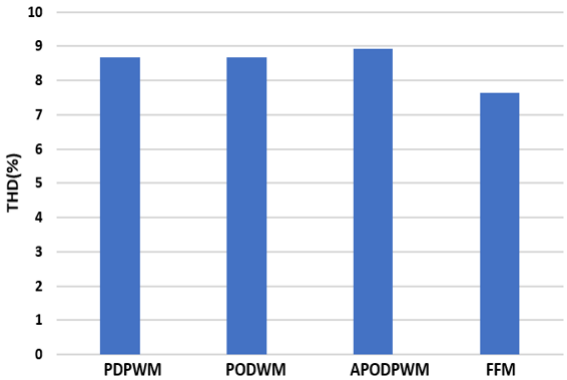

Fig. 18. THD Vs Control Strategy of Proposed Inverter

It can be inferred that FFM technique offers low THD compared to other PWM techniques at 2 kHz. The comparison based on circuit configuration is shown in Table II. N_L, N_{SW} , N_{DC}, N_C, N_D are number of levels, switches, DC voltage sources, capacitors and diodes respectively.

Table III shows the comparative study between the PWM Techniques. From the table it is clear that FFM has less harmonic distortion.

V. CONCLUSION

The proposed multilevel boost inverter topology is based on switched-capacitors. Capacitor voltage balancing is achieved without the need for any additional control strategy or auxil- iary circuit. When the output voltage levels are increased the voltage gain of the inverter also increases and offers reduced switching stress. The main disadvantage related to this circuit is that the number of components is relatively high due to the implementation of multiple levels. The proposed inverter offers an efficiency of 97.6%. Proposed inverter with FFM control strategy offers low THD compared to other control strategies.

TABLE II
COMPARISON OF INVERTER TOPOLOGIES

Topology	N_L	N_{SW}	N_{DC}	N_C	N_D	Gain
Thirteen level inverter [2]	13	7	3	-	3	1
Multilevel inverter[5]	13	14	4	8	-	1
Multilevel inverter[6]	13	12	1	2	2	1.5
Thirteen level inverter [7]	13	14	2	2	-	2
Proposed Inverter	13	17	1	3	-	3

TABLE III
COMPARISON OF PWM TECHNIQUES

Modulation Techniques	THD(%)
PDPWM	8.66
PODPWM	8.66
APODPWM	8.92
FFM	7.74

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