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Variable Gain Switched Capacitor Multilevel Inverter for Drive Applications

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ABSTRACT
Multilevel inverters (MLIs) are suitably used for high power applications because of several advantages such as low voltage stress with better harmonic spectrum and reduced filter requirements. The conventional cascaded topologies and other MLIs comprises of more number of power switches, passive elements as well as sources which makes the circuit bulkier in size, weight and less cost effective. A single phase seven level inverter with reduced component count is studied in this paper which can be used in grid and motor drive applications. Switched Capacitor (SC) technique is used in this topology and the number of output voltage levels is calculated by the number of SC cells. This work also presents the analysis of certain performance factors such as % THD, voltage stress, gain etc. with MATLAB/ SIMULINK 2017a. Output voltage level varies on varying the modulation index (M.I) and thus the gain can also be varied.

Keywords - Carrier modulation, Seven-level inverter, THD

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I. INTRODUCTION

Electricity demand is keep on increasing in modern world which has introduced new challenges for the existing power systems that have to be solved by utilizing renewable sources of energy. Conventional sources such as fossil fuel consumption lead to global warming and other environmental effects which lead to a rapid progress in finding an alternative non-conventional energy.

Power converters are becoming absolute in supplying high-quality electrical energy to different electric loads, and they are used to provide renewable energies to the consumers. The significant features of multilevel inverters are their ability to handle high voltages across individual devices, low switching and conduction losses, reduced stress, transformer-less operation and enhanced power quality with lower harmonic distortion have made them a competent solution for many applications [2].

MLI topologies can be classified into three: cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) inverters. Increasing the number of voltage levels planning to reduce total harmonic distortion (THD) with higher waveform quality results in the size and cost of the circuit but it may have a voltage balancing issue [7][8]. The major advantages such as low THD, low dv/dt switching, and reduced size of output filter make the circuit unique and give wide acceptance.

Cascading three H-bridge circuits will result in a seven-level inverter topology. However, the number of power switches and DC power supplies are more in such a case, which restricts its broad applications. Consequently, reducing the number of power components used, especially the number of DC supplies and power switches, inorder to reduce the design and execution cost as well as the size became a challenging task[1]. Capacitor voltage unbalancing problem and voltage boosting inabilities are the other crucial restraints of the existing MLIs. To implement a circuit with a single dc source can be achieved by the series connection of three capacitors, thus a series of seven-level inverters can be developed. But capacitor voltage imbalance exist as a biggest challenge.

A circuit topology that can effectively increase the number of output voltage levels with reduced component count is presented in [5] with voltage-balance control strategy for capacitor voltage imbalance. However, it creates a high output voltage harmonic distortion ratio, which cannot be allowed in real applications.

In this work, a single phase seven level inverter topology is studied. The circuit is developed based on SC technique, employing one DC voltage

source, nine power semiconductor switches, single diode and two capacitors for generating seven voltage levels and its performance analysis is done based on different control strategies.

II. CIRCUIT TOPOLOGY OF SEVEN LEVEL INVERTER

A Seven level inverter circuit [1] presented is based on switched-capacitor method as shown in Fig.1. It consists of a single DC source V_{dc} capacitors C_1 and C_2, nine power semiconductor switches and one diode. In this topology, the active switches (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8) are complement to each other.

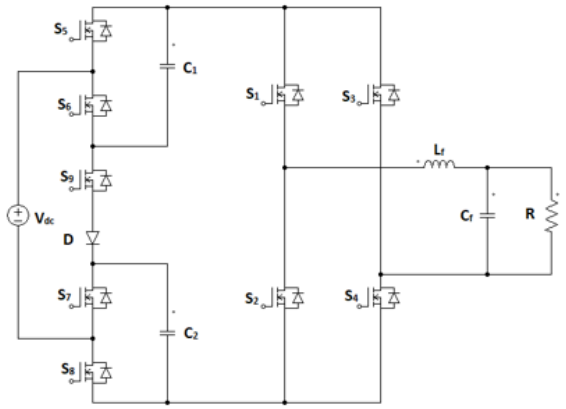

Fig.1: Single Phase Seven level Inverter

By the use of switched-capacitor technique, self balancing of capacitor voltage and a three-time boosting ability are both attained. Capacitors C_1 and C_2 are naturally maintained at V_{dc} due to the self balancing function.

Modes of Operation: The seven level inverter outputs a multilevel AC voltage which is higher than the input DC voltage by seven modes of operation for different voltage levels.

Mode 1 (+0) and Mode 2(+V_{dc}) Operation: During this mode, zero voltage is obtained at the load via S_1 and S_3 as shown in Fig.2(a). By turning on S_1, S_4, S_5 and S_8, the output voltage level V_{dc} can be achieved in Fig.2(b).

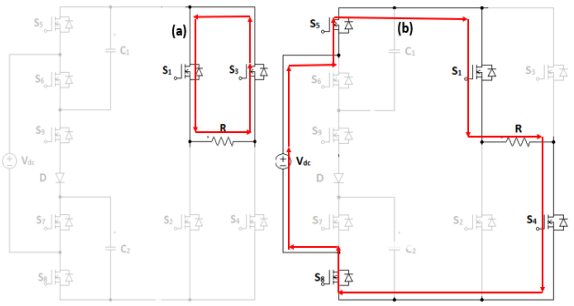

Fig.2: (a)Mode 1(+0) and (b)Mode 2**(+V_{dc})**

Mode 3 (+2V_{dc}) and Mode 4(+3V_{dc}) Operation: The voltage +2V_{dc} is applied to the load through S_5, S_1, S_4 and S_7 and the input voltage V_{dc} charges the capacitor C_1 through S_5, S_7, S_9 and D as shown in Fig.3(a). Similarly, for the output voltage of +3V_{dc}, both the capacitors C_1 and C_2 discharges along with the input source V_{dc} through S_6, S_1, S_4 and S_7 which is depicted in Fig.3(b).

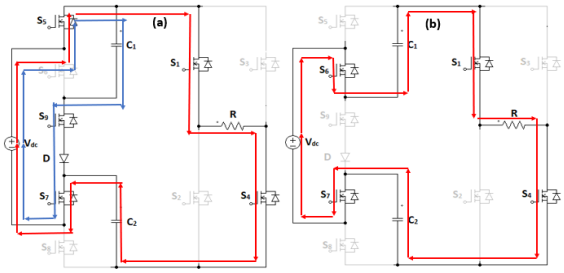

Fig.3: (a)Mode 3(+2V_{dc}) and (b)Mode 4(+3V_{dc})

Mode 5(-V_{dc}) and Mode 6(-2V_{dc}) Operation: -V_{dc} is applied to the load through S_5, S_3, S_2 and S_8 as shown in Fig.4(a). For the output voltage of -2V_{dc} capacitor C_1 discharges through S_6, S_3, S_2 and $S_8$and the capacitor C_2 charges through S_6, S_9, S_8 and diode D which is depicted in Fig.4(b).

Mode 7(-3V_{dc}) Operation: For the output voltage -3V_{dc}, the two capacitors C_1 and C_2 discharges through S_6, S_3, S_2 and S_7 as shown in Fig.5. The advantages of the seven level inverter are seven level output voltage is produced with each level of V_{dc} and a gain of three.

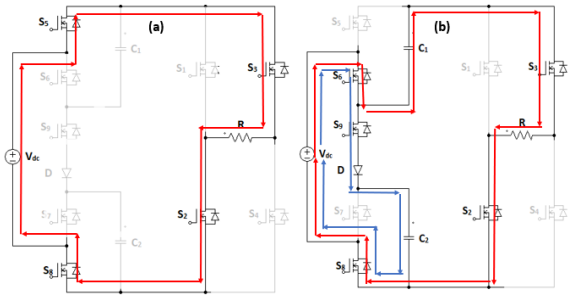

Fig.4: (a)Mode 5(-V_{dc}) and (b)Mode 6(-2V_{dc})

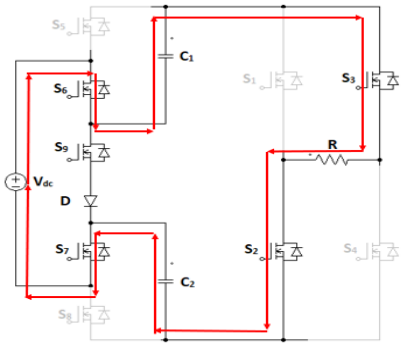

Fig.5: Mode 7(-3V_{dc})

III. CONTROL STRATEGY

Various multicarrier PWM techniques are analyzed on the inverter like Sinusoidal Phase Disposition (PDPWM), Sinusoidal Phase Opposition Disposition (PODPWM), Alternative Phase Opposition Disposition (APODPWM) etc.

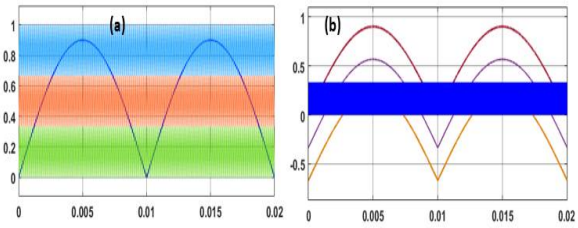

Fig.6: (a) LSCM (b)LSSM technique

Two modulation schemes are depicted in Fig.6, i.e., Level-Shifted Carrier Modulation Scheme (LSCM) and Level Shifted Sine Modulation Scheme (LSSM). These two modulation schemes provide low THD compared to other control strategies.

IV. SIMULATION AND RESULTS

The proposed MLI is simulated in MATLAB/ SIMULINK R2017a with an input of 30 V and the output obtained is 60 V RMS shown in Table I.

TABLE I
SIMULATION PARAMETERS

Parameters	Specification
Input Voltage (V_{dc})	30 V
Output Voltage (V_o)	60 V RMS
Modulating Frequency (f_o)	50 Hz
Carrier frequency (f_s)	10 kHz
Rated Output Power (P_o)	150 W
Output Load Resistance (R_o)	24 Ω
Capacitors (C_1, C_2)	4700 µF
Filter Inductance (L_f)	400 µH
Filter Capacitance (C_f)	5 µF

Gate Pulse Generation: Gate signals for 9 switches are obtained by LSCM and LSSM methods as shown in Fig.7.

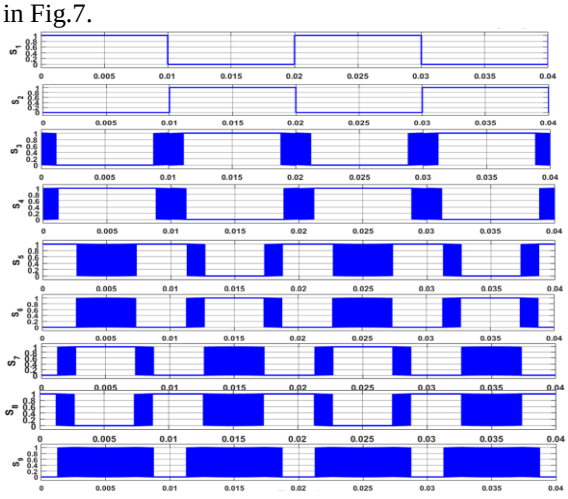

Fig.7: Gate Pulses of Seven level Inverter

Simulation Results

An input of 30 V is boosted to an output of 58.1 V RMS and output current of 2.42 A is obtained for R

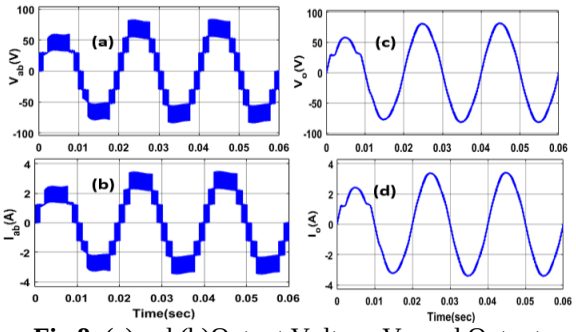

Fig.8: (a)and (b)Output Voltage V_{ab} and Output Current I_{ab} without filter (c)and (d)Output Voltage V_o and Output Current I_o with filter [LSCM]

load with Modulation index=1 which gives a voltage gain 3, obtained with LSCM scheme as shown in Fig.8. Fig.9 shows the seven stepped output voltage and current for the Seven level Inverter with each step of V_{dc} with LSSM scheme. Similar output results are generated using both the modulation schemes.

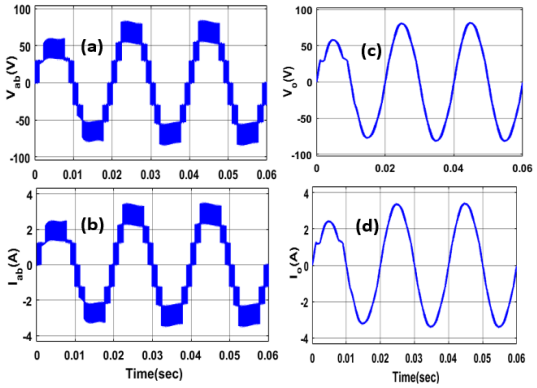

Fig.9:(a)and (b)Output Voltage V_{ab} and Output Current I_{ab} without filter (c)and (d)Output Voltage V_o and Output Current I_o with filter [LSSM]

A seven stepped output voltage with a maximum of 80 V and a current of 2.1 A is obtained for RL load where R=24 Ω and L=100mH with M.I=1, as depicted in Fig.10.

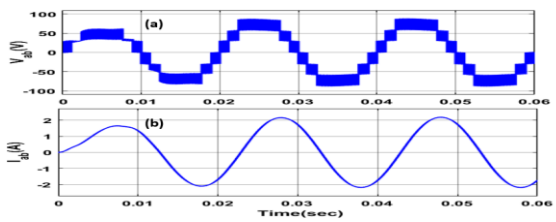

Fig.10:(a) Output Voltage V_{ab} and (b)Output Current I_{ab} for RL load

Following Fig.11 shows capacitor voltages of the two capacitors.

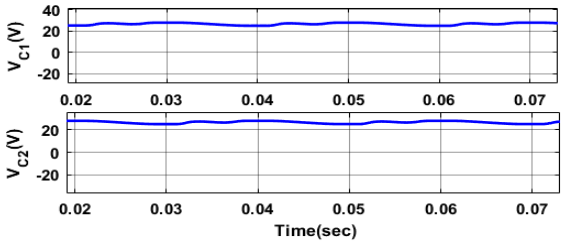

Fig.11: Capacitor voltages

Whenever the modulation index is reduced, the output voltage level also decreases which is depicted in Table II. When the modulation index is varied to 0.6 and 0.3, the output voltage levels get reduced to 5 level and 3 level with maximum voltage of 60 V and 30 V, respectively as in Fig.12. Thus output voltage levels and gain varies on varying modulation index.

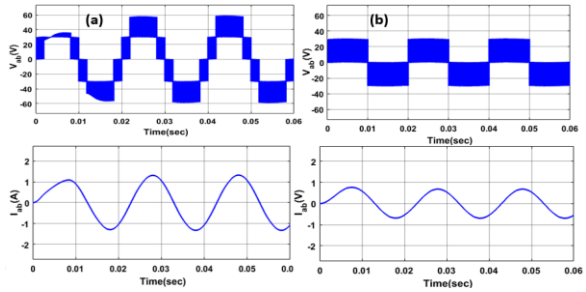

Fig.12: Output Voltage V_{ab} and Output Current I_{ab} for M.I (a)0.6 and (b)0.3

Table II
GAIN WITH MI VARIATION

MI Variation	Number of levels	Gain
0.7<MI≤1	7	3
0.4<MI≤0.6	5	2
0<MI≤0.3	3	1

Fig.13 shows the gate pulse and voltage stress across all the switches..

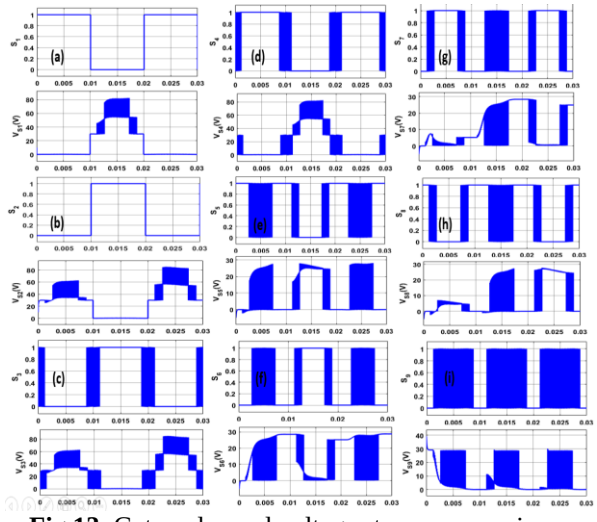

Fig.13: Gate pulse and voltage stress across nine switches (S_1-S_9)

The stress across switches S_1–S_4 has a four level voltage shape and the dv/dt of switching is very small. The major disadvantage of the circuit is the high capacitor inrush current of 500 A and input current of 200 A which is shown in Fig.14. High input current as well as high capacitor inrush current is reduced by applying an initial charge of 27.5 V to both the capacitors. An initial charge of 27.5 V is fixed based on the analysis done. The output voltage and current with initial charge given is shown in Fig.15.

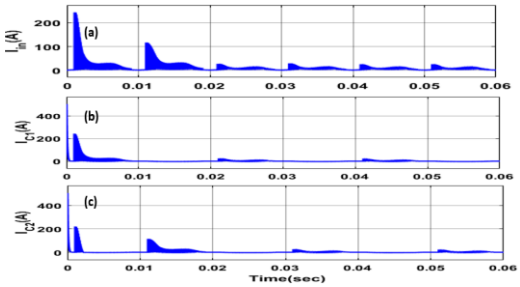

Fig.14:(a) Input Current (b)Capacitor Current

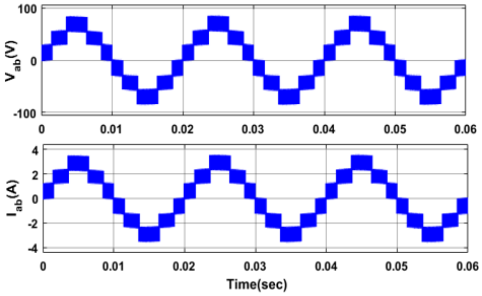

Fig.15: Output results with initial charge

V. PERFORMANCE ANALYSIS

Efficiency Vs Output Power: The inverter efficiency is around 96.5 % for 150 W output power for a R load of 24 Ω which is depicted from Fig.16. An initial charge of 27.5 V is given to both the capacitors and analysis is done. The inverter provides a good efficiency of 80-97% for an output of 60 W - 450 W with initial charge which is depicted from Fig.16.

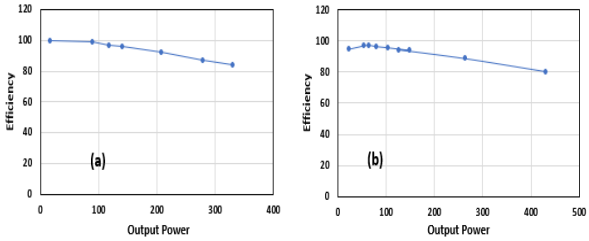

Fig.16: Efficiency Vs Output Power

THD Vs Control strategies: Fig.17(a) depicts the %THD for different PWM methods such as PDPWM, PODPWM, APODPWM and FFM for the

seven level inverter. It can be inferred that LSCM and LSSM offers low THD of 18.3% compared to other PWM techniques at 10kHz for seven level inverter. Fig.17(b) shows that THD is less at 10kHz for both LSCM and LSSM.

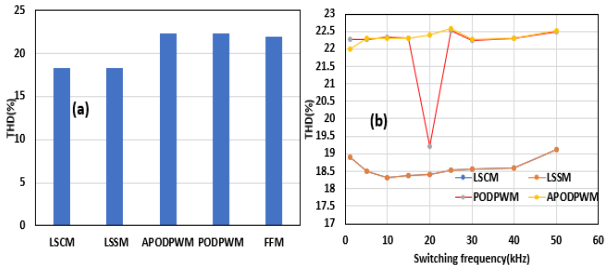

Fig.17:(a) THD Vs Control strategies (b)THD Vs switching frequency

Input Current Vs Initial Charge: An initial charge of 27.5 V is applied to the two capacitors based on the result shown in Fig.18. Initial charge is varied from 18 V-30 V, and a charge of 27.5 V offers the lowest capacitor voltage ripple of 1.5 V.

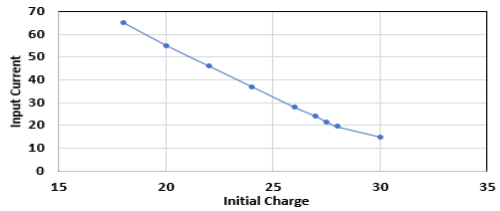

Fig.18: Input Current Vs Initial Charge

FFT Analysis: Fig.19 shows the FFT analysis of output voltage using LSCM and LSSM technique, which is about 18.3% using both LSCM and LSSM schemes and dc component is 0.00939.

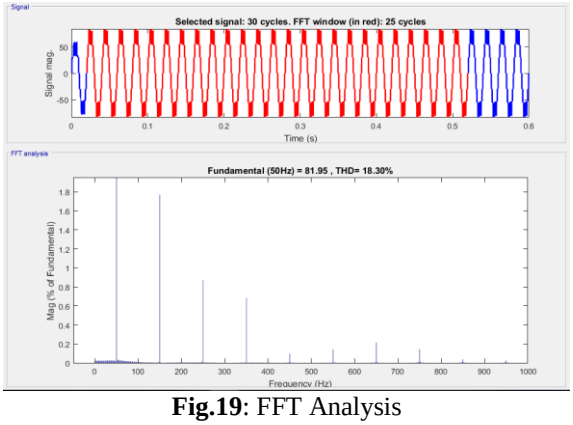

Fig.19: FFT Analysis

APPLICATION: Seven level inverter can be used in renewable energy integrated grid application as well as an AC motor drive application. Here the inverter is used to operate a Single-phase induction motor with a fixed M.I=1 instead of a R/RL load and Fig.20 depicts the speed and torque characteristics of motor with speed of 1500 rpm and torque of 10 Nm.

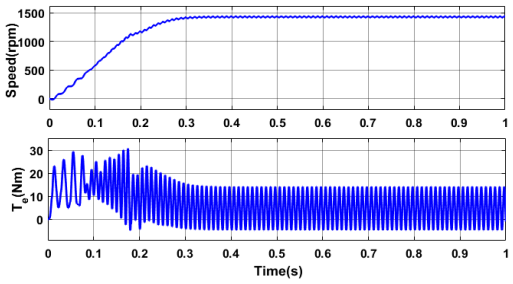

Fig.20: Speed and Torque Characteristics

Comparison

Table III shows the comparison of different seven level inverter topologies and among them, the Seven level inverter studied has least number of components.

TABLE III
COMPARISON OF SEVEN LEVEL INVERTER TOPOLOGIES

Topology	N_{sw}	N_C	N_d	N_{Cbal}
Diode-clamped [2]	12	6	30	0
Capacitor-clamped [2]	12	6	0	15
Cascaded H-bridge [3]	12	3	0	0
Switched capacitor topology [4]	10	0	0	3
Switched capacitor topology [6]	8	2	0	1
Switched capacitor topology [7]	7	3	2	0
Seven level Inverter	9	0	1	2

Table IV shows the comparative study between different PWM Techniques. and it is clear that LSCM and LSSM has less harmonic distortion.

TABLE IV
COMPARISON OF PWM TECHNIQUES

Modulation Techniques	THD (%)
LSCM	18.3
LSSM	18.3
POPWM	22.33
APODPWM	22.3
FFM	21.93

Among the different seven level inverter configurations, the presented circuit [1] gives better results in terms of device count. From the simulation results, the output voltage levels vary according to variable M.I and thus variable gain can be obtained. Gain can also be improved by adding SC cells, but it make the circuit more bulkier and less efficient compared to existing topologies. So it can be rearranged with the existing number of capacitors based on the circuit proposed in [8].

VI. CONCLUSION

In this paper, a switched capacitor seven-level inverter is studied, which uses less components compared to conventional inverters and existing switched capacitor MLIs and no inductor is employed, so that the circuit structure is small and simple. LSCM and LSSM produces less THD among all the multicarrier PWM techniques. Operation and performance analysis of proposed inverter are studied and verified. Inrush current is reduced by providing initial charge. By varying M.I, output voltage can be varied with different levels and thus variable gain is obtained.

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