

Hybrid Approach to solve Capacitor Allocation problem in Distribution System Using Political Optimizer Algorithm

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Abstract

Decreasing of power loss and boosting of voltage profile (VP) in the distribution network (DN) is an important issue in recent times in this paper a systematic approach is introduced to tackle the capacitor placement problem in DN to boost voltage profile (VP) as well as power loss reduction. further consolidated methodology of voltage stability index and the political algorithm is introduced to take care of capacitor position issue in DN. further, the goal of the carried-out technique is to decrease the power loss of DN. Further created approach is tried on 69 and 33 bus system and different cases are considered for examination. Further the results of created technique are compared.

Keywords: distribution system, political algorithm, consolidated, voltage profile, power loss.

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I. INTRODUCTION:

The losses in the distribution network (DN) are predominately overwhelming when contrasted with the transmission system. Also, the greater part of the DNs is radial and voltage profiles at end clients in these types of networks are extremely less. So, along these lines it is needed to improve voltage profile [VP] and decrease the losses to the maximum extent in DN is a very significant issue. Further, the load associated with DN are increasing in recent times and this decreases the consumer voltage profile (VP) further. thus, reasonable compensating devices are needed to control these voltage levels in recommended limit for accomplishing this. It is needed to put appropriate capacitors with proper sizes in DN. The Inappropriate placement of the capacitor will reduce the advantages of the system and even damage the whole system.

Various researchers solved the capacitor placement problem (CPP) in DN and achieved good results in reducing power losses and increasing VP in DN. In [1] CPP is solved by using Adaptive whale optimization algorithm (AWOA). In [2] CPP is solved by Honey Bee Mating Optimization Algorithm (HBMO) in primary distribution network and the results were compared with other algorithms.in [3] authors solved CPP in DN by Diffusion and update techniques-based algorithm (DUTA). Further, this method is implemented on 15 and 33 bus system and results are compared with other methods.in [4] CPP in DN is solved by the new metaheuristic algorithm is proposed and it is

called as political optimization. Further, this algorithm is compared with other algorithms .in [5] CPP in DN is solved by using Polar bear optimization algorithm is proposed to place shunt capacitor in DN at various loads. Further, the results are implemented for 15,30,33,85 bus system. In [6] Optimal placement of capacitor banks in distribution system by using Hybrid Flower pollination algorithm (FPA)-Exhaustive search approach. Further, it is implemented on 10,34 and 85 bus system and compared with other algorithms. In [7] author presented a multi-stage procedure based on two LSI (Loss sensitivity indices) and ACO algorithm to find the optimal allocation and size of the capacitor for power loss reduction and increase in voltage profile in DN. In [8] to overcome the disadvantages of classical gradient-based algorithms. New flexible meta-heuristic algorithm is presented, such as particle swarm optimization (PSO) algorithm. Further, it is a stochastic algorithm and it does not depend on the gradient information about the objective function. In [9] CPP problem is solved by using firefly algorithm. Further, this method is tested on Taiwan 83 bus system for DN. In [10] CPP is solved by using Dragonfly algorithm. Further, it is tested on 119 bus system. In [11] CPP is solved by using TLBO algorithm. Further, it is compared with PSO, GA. In literature survey various authors used different optimization methods to solve the CPP in DN. In this paper, combined approach of PO and VSI is presented to solve the capacitor placement problem in DN. Further, the implemented method is tested on 33 and 69 bus system.

The article is mainly divided into the following sections. In section 2 problem formulation and objective function are explained. In section 3 VSI for CPP is explained. In section 4 algorithm steps to solve the capacitor allocation problem are explained. In section 5 results and discussions are explained. In the last section conclusion of the article is presented.

II. PROBLEM FORMULATION:

2.1 Load flow analysis

Generally, analysis of load flow is significant to evaluate the exhibition of the power system, especially how much current is passing throughout the circuit, voltage level, and power flow calculations. Further, the most regularly utilized LF methods are the gauss seidel technique, NR, and decoupled method however these methods are not given proper data because DN calculation thus distribution load flow is utilized for computing power flows in a circuit.

2.2 objective

The principal focus of this paper is to place capacitors suitably and minimize the power loss and enhance the voltage profile of DN to a considerable extent.

2.2.1 Power loss minimization

$$Powerloss = \sum_{x=1}^{ya} |I_x|^2 R_x \quad (1)$$

2.2.2 Constraints:

Voltage limits

$$|V_{min}| \leq |V_m| \leq |V_{max}| \quad (2)$$

Power balance:

$$P_{ss} = \sum_{x=2}^y P_x + \sum_{y=1}^{nz} P_{loss}(x, x+1) - \sum_{y=1}^{nzc} P_{cap,x} \quad (3)$$

Reactive power:

$$\sum_{u=1}^{N_c} Q_{C,u} \leq 1.0 \sum_{u=1}^n Q_L \quad (4)$$

III. VOLTAGE STABILITY INDEX (VSI) FOR OPTIMAL CAPACITOR PLACEMENT PROBLEM (CPP)

Voltage breakdown is a huge issue in RDN. Further, the buses with the insignificant opinion of the VSI are a proper decision for placing capacitors. So, utilizing this index estimate weak buses and place capacitors at these buses. Further, the formulae for VSI are determined by

$$VSI_l = |V_m|^4 - 4[P_l r_{lm} + Q_l x_{lm}] |V_m|^2 - 4[P_l x_{lm} - Q_l r_{lm}]^2 \quad (5)$$

The VSI for 33 bus systems in the base case is represented in Fig.1.1 and the buses with the least values of VSI are considered as the best for placement of the capacitors.

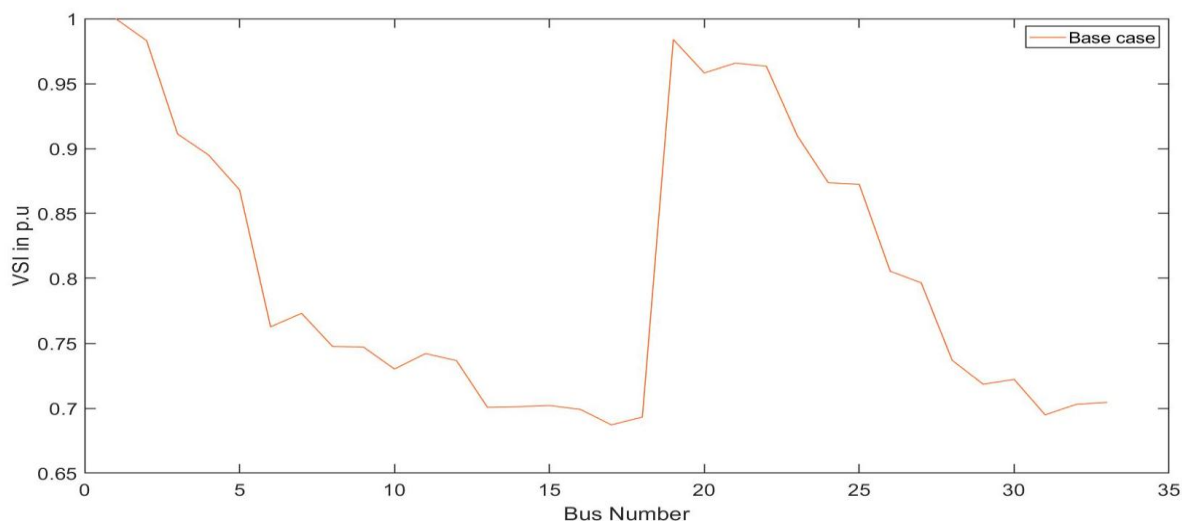


Fig.1.1 Base case VSI values for 33 bus system.

The VSI for 69 bus system in the base case is represented in Fig.1.2 and the buses with the least

values of VSI are considered as best for placement of capacitors.

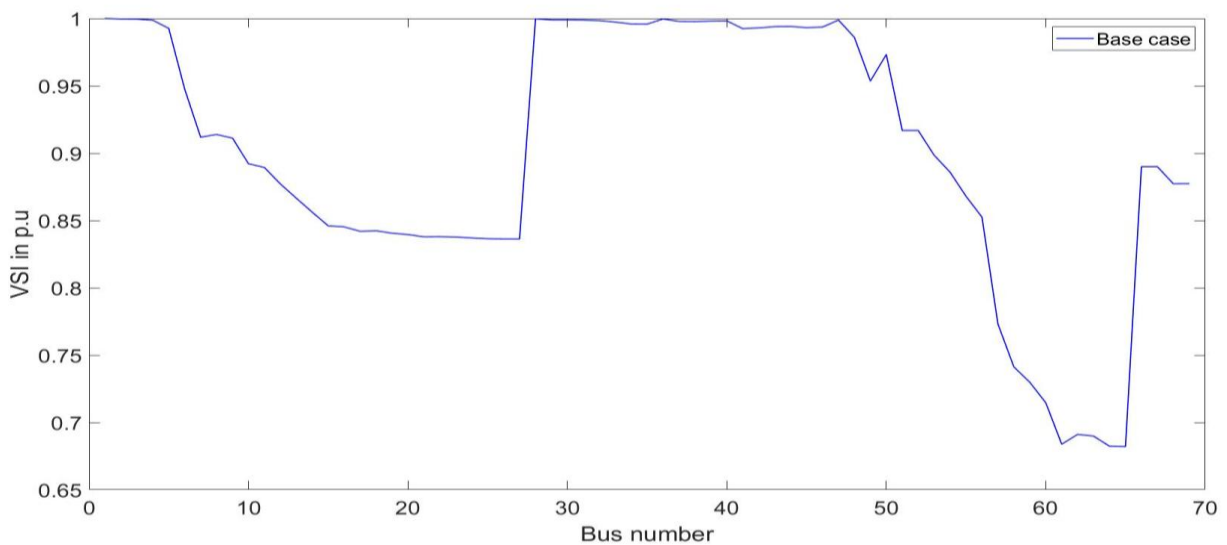


Fig.1.2 Base case VSI values for 69 bus system.

IV. POLITICAL OPTIMIZER ALGORITHM (POA)

Political optimizer (PO) is created by Qamar askarithe. Political optimizer is a mathematical mapping of all major phases of politics and they are given in [4]. In this article, it is used to find the best sizes of capacitors. Before these locations are find out by the VSI.

4.1 Algorithmic steps to solve capacitor allocation problem.

- S1: Collect the test system data.
- S2: Read bus and line data.
- S3: Develop DLF.
- S4: Run DLF.
- S5: Calculate the base case values of power loss and VSI.
- S6: Identify the weak buses by VSI.
- S7: Given as input to PO.
- S8: Rank the Sizes of capacitors.
- S9: Calculate the power loss for given capacitor sizes.
- S10: Repeat the same process for up to maximum iterations.
- S11: Print the results.
- S12: Stop the procedure.

V. RESULTS AND DISCUSSION:

The developed strategy is executed in MATLAB. The test system considered for implementation is 33 and 69 bus. Further, the active power loss without placement of capacitor for 33 and 69 buses are 202.66kw and 225.95kw. VP for 33 and 69 bus without placement of capacitor are

0.9131 p. u and 0.9090 p. u. Next identified the weak buses using VSI. The best buses for placement of capacitors for 33 bus systems are 16,17,30 and 69 buses are 26,60,63. Three cases are considered for the analysis and the same is tabulated in Table 1 and Table 2.

- Base case
- Case 1: 1 Capacitor
- Case 2: 2 Capacitors
- Case 3: 3 Capacitor

5.1 IEEE 33 Bus system

In case 1 when the capacitor is connected at 16 bus the power loss is minimized to 181.62 kW and the minimum voltage profile (VP) is improved to 0.9419 p.u.

Further, in case 2 two capacitors are placed at 16 bus and 17 bus, and the power loss is reduced to 181.25 kW and the voltage profile VP is enhanced to 0.9426 p.u. So, the percentage loss reduction is improved to 10.56 as compared with the base case. Next in case 3 three capacitors are considered and placed at bus numbers 16,17 and 30. The power loss, in this case, is reduced to 141.048 kW and voltage profile VP is enhanced to 0.9445 p.u. Finally, in overall comparison point of view, the percentage loss reduction in case 3 is 30.40 as compared to base case so power loss is decreased if the number of capacitors placed at best locations is increased but a greater number of capacitors is placed at suitable locations again increases the power loss so optimal number of capacitors at desired locations minimizes the losses to a considerable extent. Finally, voltage profile VP comparison for the base case and cases 1,2, and 3 are illustrated in Fig 1.1 and fig 1.2. It is observed that voltage profile VP at all buses is

improved after placing of capacitor in suitable positions.

Table 1: Simulation results of 33 bus system for different cases

Particulars	Base case	Case 1	Case 2	Case 3
Best location (size in kvar)	NA	16(519.9030)	16 (480.522) 17(38.630)	16 (210.137) 17 (116.679) 31 (968.183)
Power loss (kW)	202.66	181.628	181.259	141.048
% Loss reduction	NA	10.37	10.56	30.40
V _{min} (p.u)	0.9131	0.9419	0.9426	0.9445

5.2 IEEE 69 Bus system

In case 1 when the capacitor is placed at 26 bus the power loss is minimized to 215.007 kW and the minimum voltage profile VP is improved to 0.9104 p. u further, in case 2 two capacitors are connected at 26 bus and 60 bus and the power loss is reduced to 147.57 kW and the voltage profile VP is enhanced to 0.9306 p.u. So, percentage loss reduction is improved to 34.12 as compared to base case. Next in case 3 three capacitors are considered and placed at bus numbers 26,60 and 63 the power loss, in this case, is reduced to 147.237kw and voltage profile VP is enhanced to 0.9314 p.u. Finally, in overall comparison point of view, the percentage loss reduction in case 3 is 34.57 as

compared to base case so power loss is decreased if the number of capacitors placed at best locations is increased but a greater number of capacitors is placed at suitable locations again increases the power loss so optimal number of capacitors at desired locations minimizes the losses to a considerable extent. Finally, voltage profile VP comparison for the base case and cases 1,2, and 3 are illustrated in Fig 2.1 and Fig 2.2. It is observed that voltage profile VP at all buses is improved after placing capacitors in suitable positions.

Table 1: Simulation results of 33 bus system for different cases

Particulars	Base case	Case 1	Case 2	Case 3
Best location (size in kvar)	NA	26(397.610)	26 (268.504) 60(1.2886e ⁰³)	26 (271.690) 60 (1.079e ⁰³) 63 (209.463)
Power loss (kW)	225.001	215.007	147.573	147.237
% Loss reduction	NA	4.442	34.412	34.57
V _{min} (p.u)	0.9090	0.9104	0.9306	0.9314

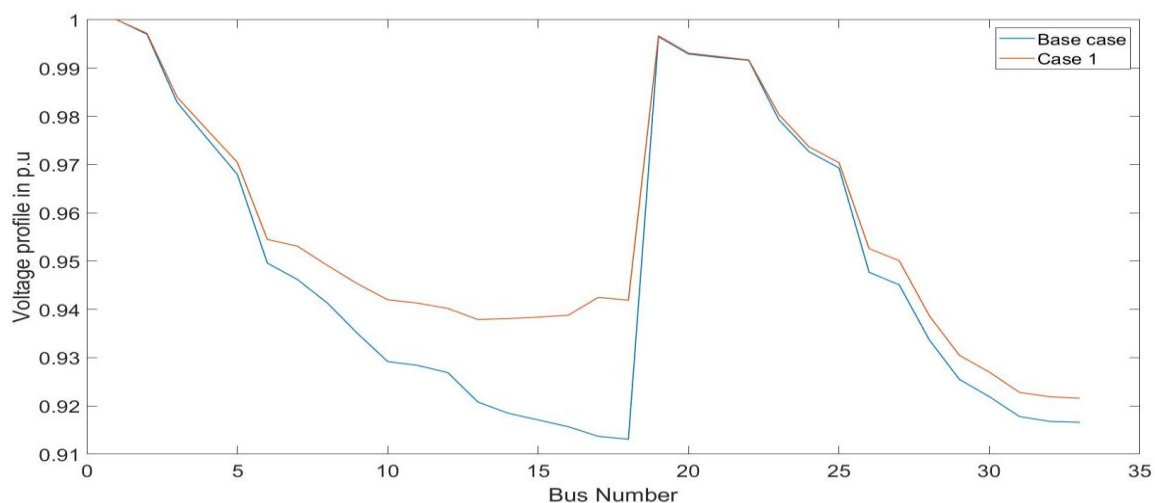


Fig.1.1. Voltage profile comparison of 33 bus system (Base case, Case 1)

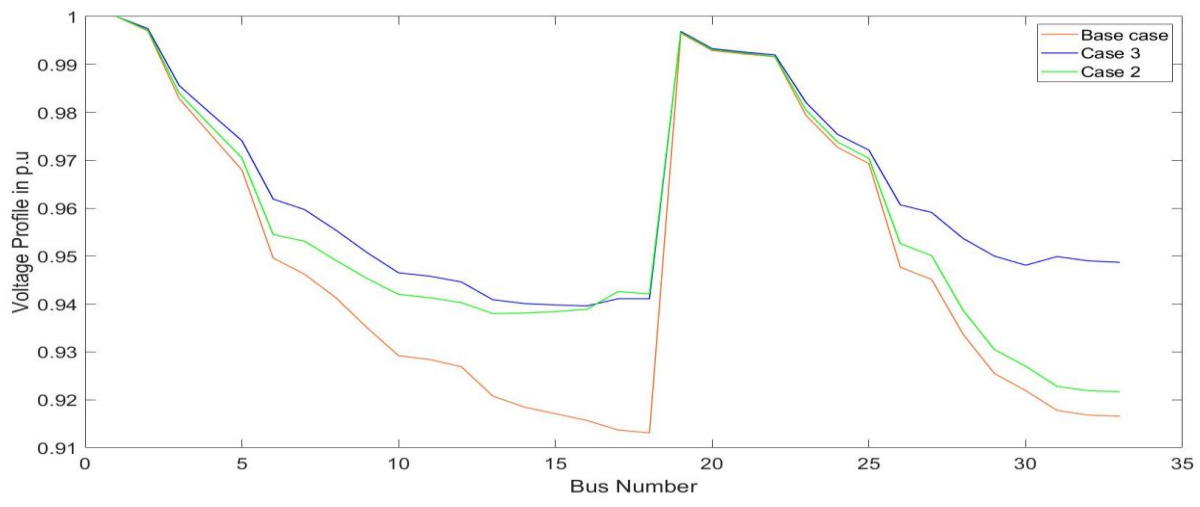


Fig.1.2 Voltage profile comparison of 33 bus system (Base case, Case 2, Case 3)

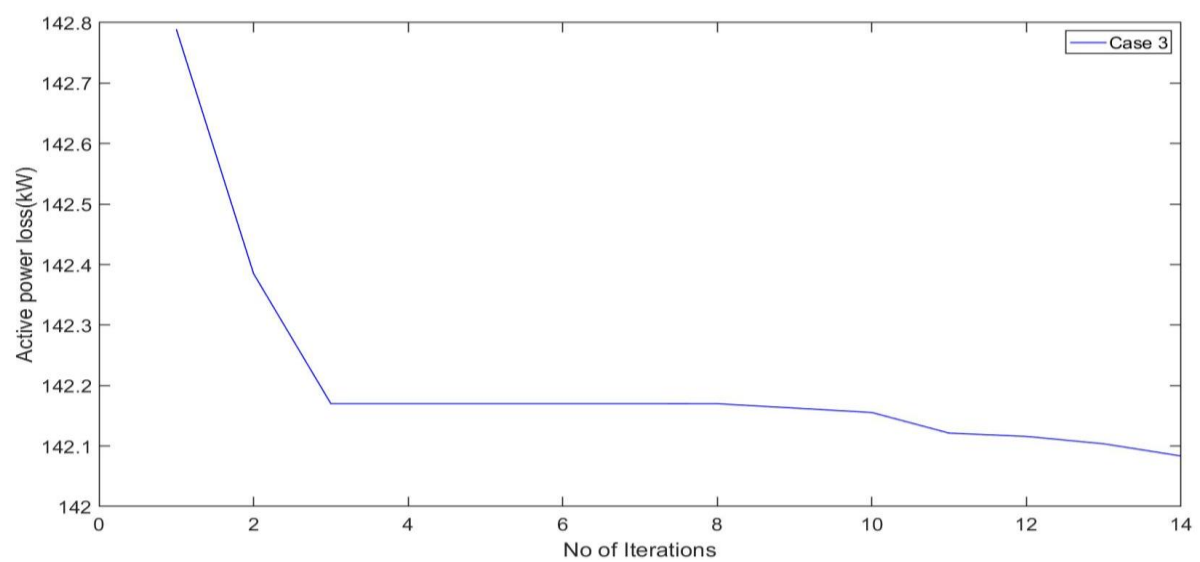


Fig 1.3 Convergence curve of Political Optimizer algorithm for case 3 for 33 bus system.

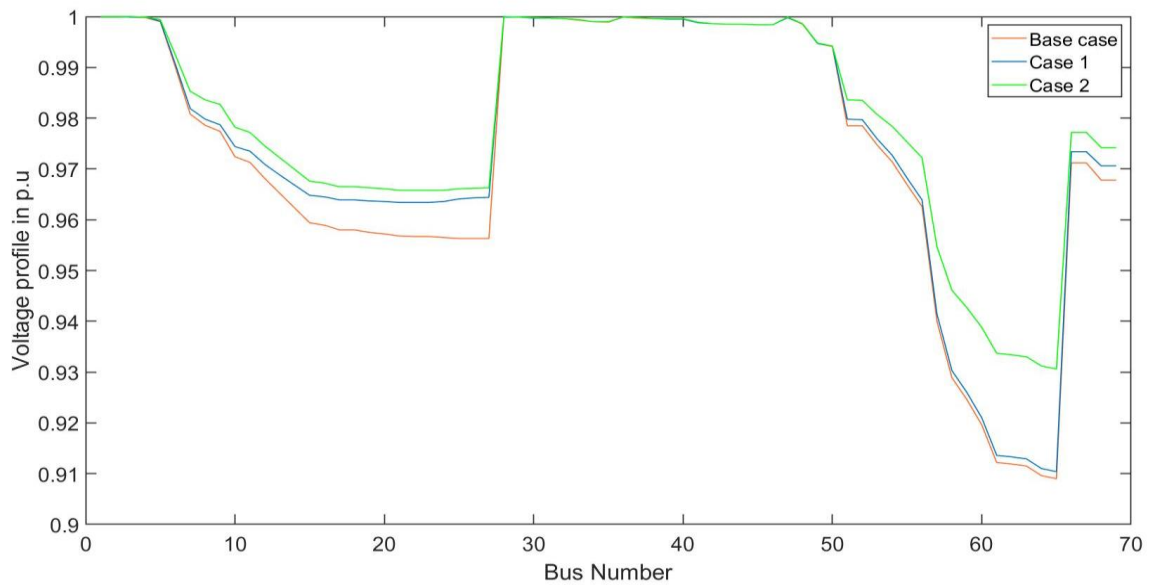


Fig.2.1. Voltage profile comparison of 69 bus system (Base case, Case 1, Case 2)

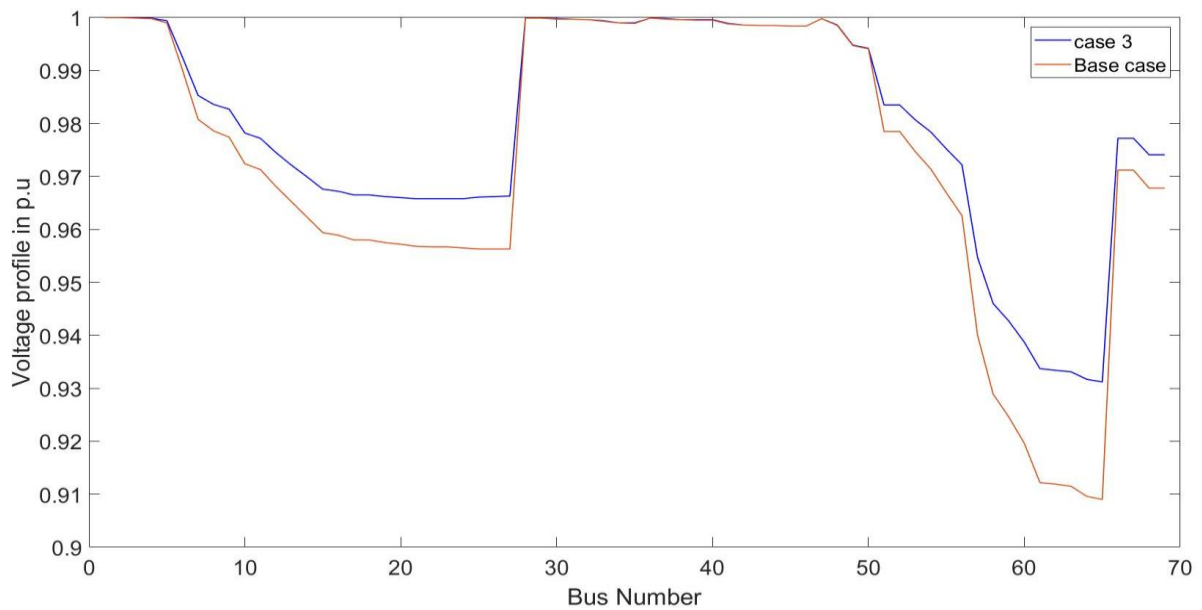


Fig.2.2 Voltage profile comparison of 69 bus system (Base case, Case 3)

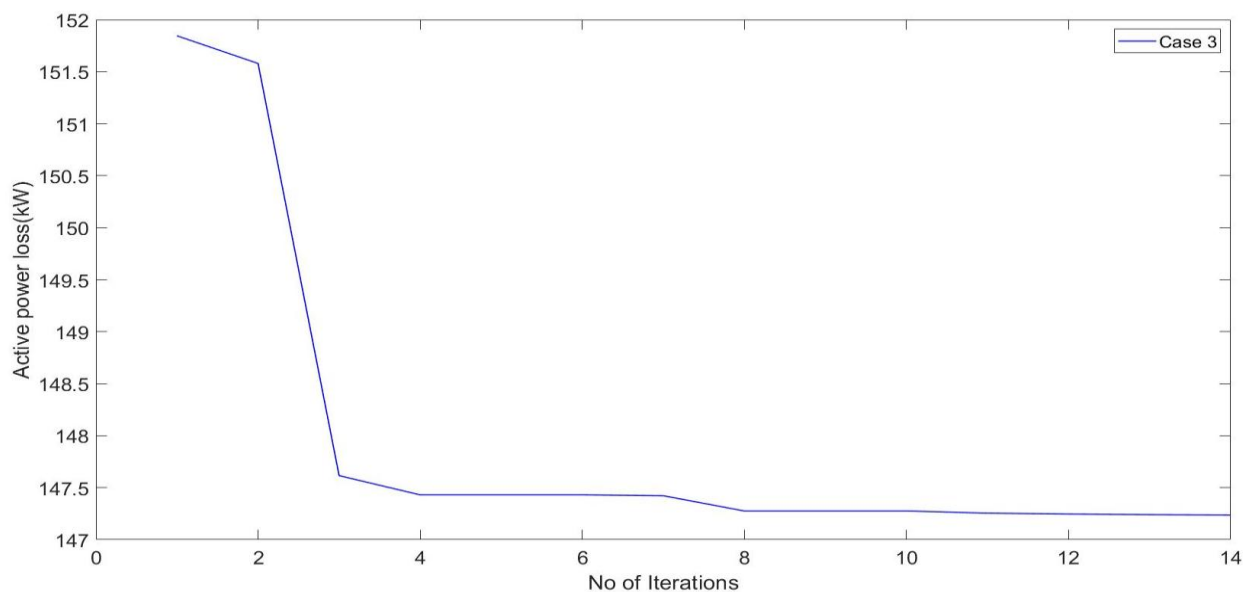


Fig 2.3 Convergence curve of Political Optimizer algorithm for case 3 for 69 bus system.

VI. CONCLUSION

This paper presents a hybrid approach dependent on VSI and a political optimizer algorithm to settle CPP in DN. Also, practical 33 and 69 bus systems are considered for the analysis. Further, various cases are viewed for example position of a single capacitor and multiple capacitors and, study the performance. From obtained results, it is checked that placement of an ideal number of capacitors in appropriate locations with best sizes limits the DN losses to a reasonable extent. Additionally, voltage profile is improved in cases after CPP. At last, it tends to be concluded that placement of a greater number of capacitors in DN doesn't lessen the power losses to the maximum extent. The only suitable number of capacitors placed in appropriate locations with the best sizes reduces losses and improves the system's performance efficiency.

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