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Design and implementation of MAC based FIR filters using logic optimization techniques

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ABSTRACT
In present scenario, a finite impulse response (FIR) filter is mostly used for DSP applications in communication and digital systems. The main purpose of the FIR filter is to afford high performance, greater flexibility and low cost. For this, the demand for FIR filter applications is increasing day by day in order to extract the raw signals from the noisy signal by using filtering techniques. One such filtering technique which plays the key role to remove the noise is FIR filter because of its characteristics such as linearity, stability and BIBO. In the design of FIR filter, adders and multipliers plays the vital role as they decide the cost, area, power and speed of the FIR filter. Here, the new implementing approach for adder was adopted by the CSLA dominated by carry generation logic and multiplier design was adopted by Square Architecture Based Vedic Multiplier using Multiplexer Based Full Adders for designing MAC based FIR filter using logical gates. In this paper, coding is done by using Verilog HDL and Simulation and synthesis is done by using Xilinx Vivado v2017.2 software tool. MAC based FIR filter for 16-tap using Full adder 2 has better reduction in power consumption i.e. 1.3871% in terms of watts, Combinational delay i.e. 2.4710% in terms of milliseconds and the overall LUT's i.e. 9.6408% than the MAC based FIR filter for 16-tap using fulladder1.

Keywords - CSLA dominated by carry generation logic, Vedic multiplier using Yavadunam sutra, A MAC based FIR filter for 16-tap using different full adders.

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I. INTRODUCTION

Digital filters are the most frequently used elements in signal processing applications. Among digital filters, FIR filters are preferred due to their stability, easily achievable linear-phase property, and low quantization word length sensitivity. All these desirable properties come with a drawback compared to their recursive counterparts IIR filters: increased computational workload. This leads to excessive amount of power applications. In most of the digital signal processing (DSP) Multiplication and Accumulation are used as most important operations. Thus, the FIR filter uses different types of multipliers, adders and the delay unit. If we use this structure area, delay and time consumption will be more. Thus, the entire structure as shown above can be replaced with a MAC (Multiplier and Accumulate unit). Multiplier and Accumulator unit (MAC) consumes low energy and the gained excessive overall performance of the digital signal processing system is the key point of MAC unit. In order to eliminate or remove the excess noise in ECG signals Finite impulse response (FIR) filters are widely used because of its notable characteristics such as linearity, stable and BIBO. Many architectures are developed by using various MAC unit models by replacing many multipliers along with adders units. It also suits for portable and area efficient applications where high speed is not their primary objective. Many researches were done on different methodologies to reduce the area efficiency. One of the predominantly used filter is FIR which implements in transposed direct form [1]. FIR filter architecture to trade off filter performance for dynamic power consumption [2]. The hardware-efficient fixed-point FIR filters in an expanding sub expression space [3]. Linear phase response and desirable numerical property to perform FIR filters

[4-5]. Implementation of wireless applications [6]. The following sections i.e. the architecture of different full adders, the design architecture of Square Architecture Based Vedic Multiplier using Multiplexer Based Full Adders (multiplier) and the designed architecture of carry select adder dominated by carry generation logic (adder). And simulation results of obtained MAC based FIR filter for 16-tap using different full adders are discussed below.

II. MAC BASED FIR FILTERS

The main elements in the design of MAC based FIR filters are multiplier, adder, accumulator and a delay unit. Multiplier unit is designed by using Square based yavadunam sutra as discussed in section IV. In the design of multiplier adders are used for partial product additions which are done by full adders Adder unit is designed by using carry select adder dominated by carry generation logic as discussed in section V.

III. ARCHITECTURES OF DIFFERENT FULLADDERS

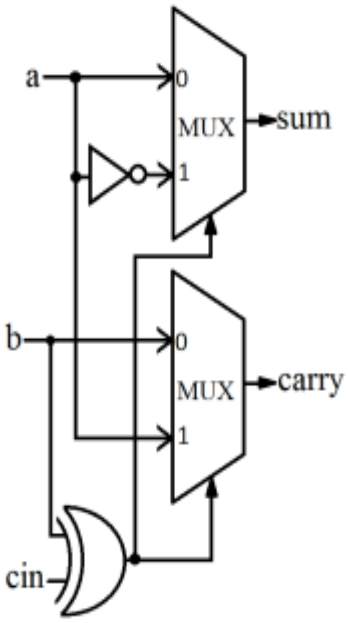

Fig.2: Architecture of fulladder1.

The design of multiplier in MAC based FIR filter is carried out by using vedic multiplier using yavadunam sutra in which the main element is a adder as it performs addition for partial products. Adder design is carried out by using different full adders. In fulladder1, the design is carried out by using one XOR gate, one NOT gate and two sets of 2:1 Multiplexers as shown in fig.2.

Similarly, in fulladder2 the design is carried out by using XOR gate, NXOR gate and two sets of 2:1 multiplexer as shown in fig.3

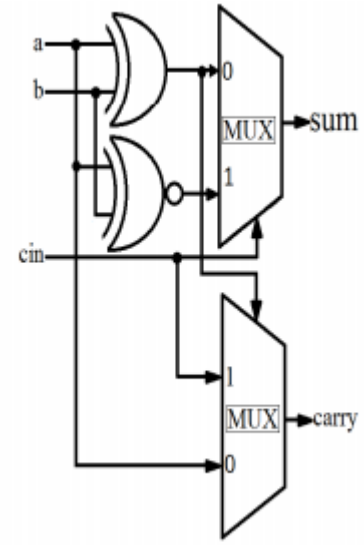

Fig.3: Architecture of fulladder2

IV. SQUARE BASED ARCHITECTURE

The design of square architecture based on yavadunam sutra is shown in fig.4.

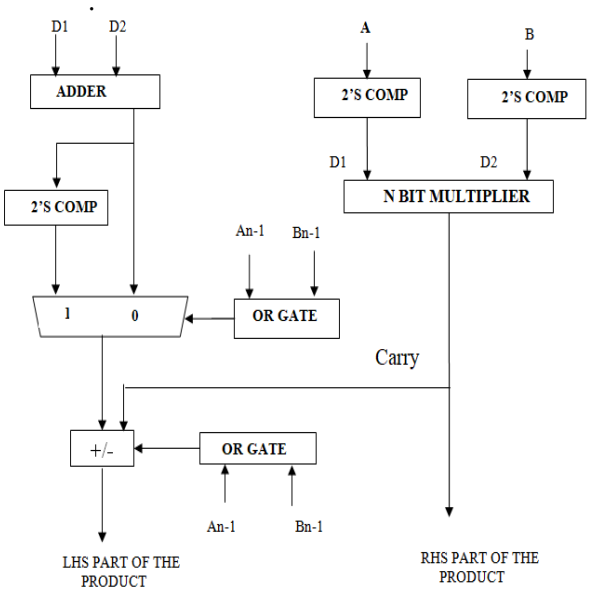

Fig.4: Square based Architecture.

Here A and B are given as inputs to square architecture. The 2's compliment of A is taken as deficiency D1 and 2's compliment of B is taken as deficiency D2. With the help of N bit multiplier, the two deficiencies i.e. D1 and D2 are multiplied. By using N bit multiplier the product of D1 and D2 are obtained as RHS part of the product. On the other

D1 and D2 are added and the obtained result will perform 2's compliment and it is taken as '1' on one hand and direct obtained output is taken as '0' in another hand after performing OR operation. The carry obtained by the RHS is added and the sign varies with the input. Based on input LHS part of the product will be obtained

V. DESIGN OF CARRY SELECT ADDER

The designed architecture mainly focuses on achieving lower area circuit and reducing the delay and power consumption.

The architecture consists of three blocks, they are: Primary carry Unit, Wave carry Unit, Final Selection Unit as shown in fig.5.

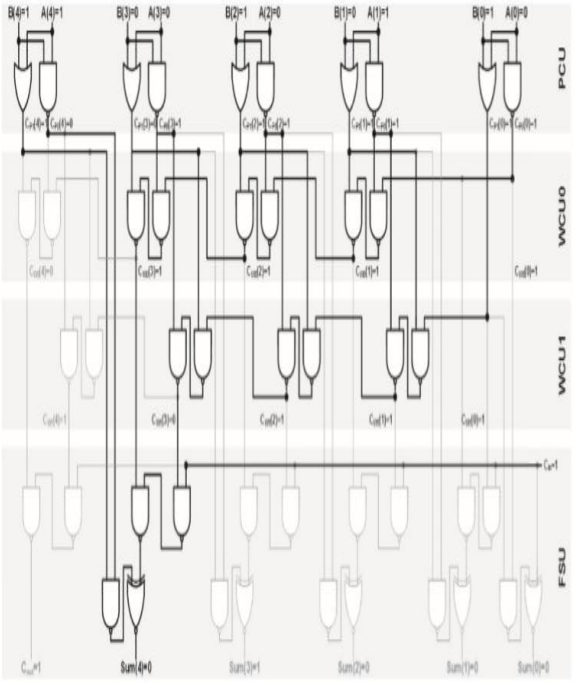

Fig.5: CSLA dominated by carry generation logic.

Block-1: The PCU generates the primary carry with two inputs A and B and produces outputs CP0 and CP1 and the PCU consists of a NAND-gate and an OR-gate for each bit and does not require Cin as an input.

Block-2: The two WCU units work simultaneously assuming a carry input for 'Cin=0' and 'Cin=1,' and it is chosen at FSU by Cin. The PCU sends their outputs CP0 and CP1 to WCU0 and WCU1, respectively.WCU0 and WCU1 will output CW0 for Cin ='0' and CW1 for Cin ='1', which are vertical carry propagation, to FSU.

Block-3: The FSU calculates the final outputs Sum and Cout. Both PCU and WCU are different from FSU where FSU requires the initial input as Cin. The PCU and WCU provide input variables to the FSU. With the help of three NAND-gates and one XNOR-gate a bit slice of FSU is designed. The FSU also has a constant delay regardless of the size of the bit-width since a bit's lice logic directly produces the final output. The power consumption and area efficiencies are more effective in CSLA dominated by carry generation logic when compared to other adders.

VI. SIMULATION RESULTS

The RTL schematics diagram of MAC based FIR filter for 16-tap as shown in fig.6 and fig.7.

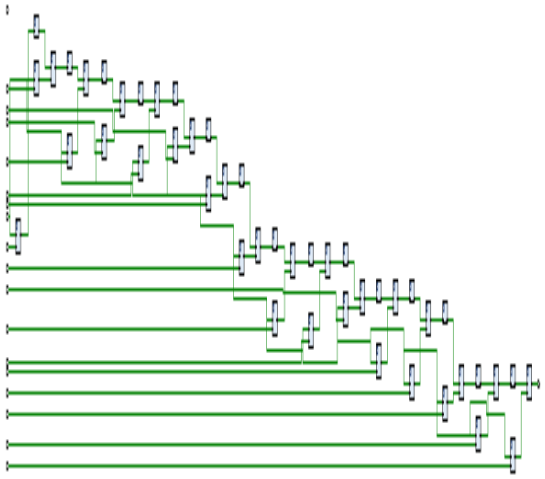

Fig.6: RTL Schematic diagram for MAC based FIR filter for 16-tap using fulladder1.

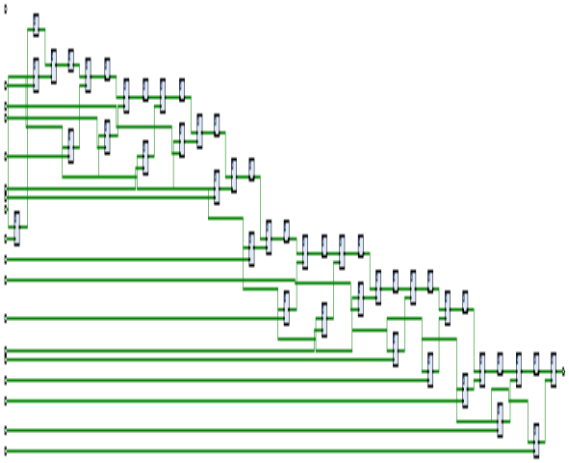

Fig.7: RTL Schematic diagram for MAC based FIR filter for 16-tap using fulladder2.

The simulation results of MAC based FIR filter for 16-tap using fulladder1 and fulladder2 are shown in fig.8 and fig.9.

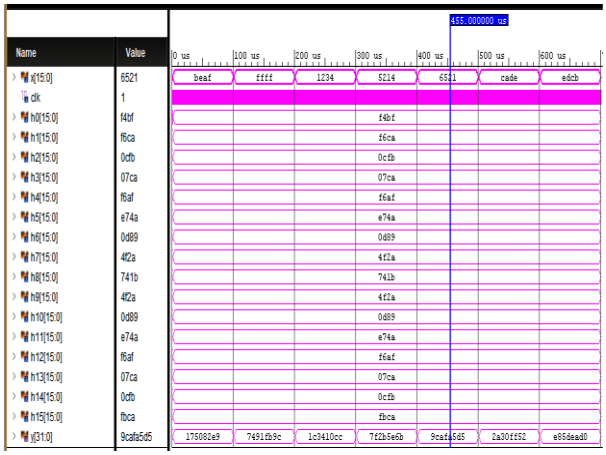

Fig.8: Simulation results for MAC based FIR filter for 16-tap using fulladder1.

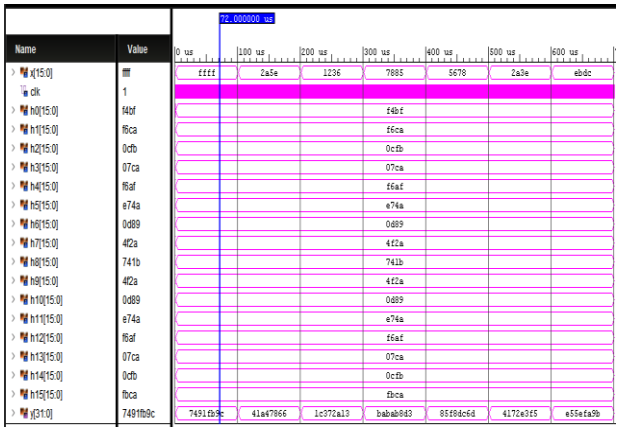

Fig.9: Simulation results for MAC based FIR filter for 16-tap using fulladder2.

After completion of synthesis and implementation, the total LUT's and power consumption are obtained for MAC based FIR filter for 16-tap using fulladder1 and fulladder2 are shown in fig.10 and fig.11.

Total Power	Failed Routes	LUT
		1587
150.159	0	1576

Fig.10: LUT's and power for MAC based FIR filter for 16-tap using fulladder1.

Total Power	Failed Routes	LUT
		1434
148.076	0	1423

Fig.11: LUT's and power for MAC based FIR filter for 16-tap using fulladder2.

Lastly the Combinational Delay is obtained for MAC based FIR filter for 16-tap using fulladder1 and fulladder2 are shown in fig.12 and fig.13.

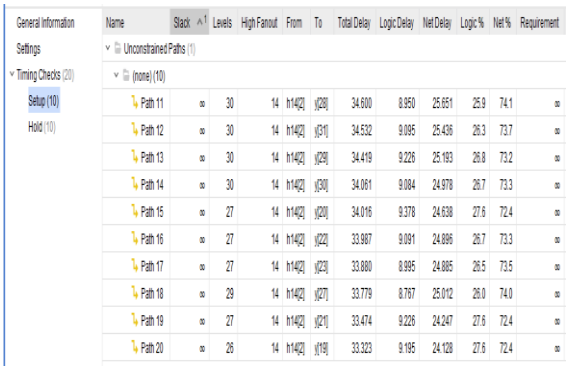

Fig.12: Delay for MAC based FIR filter for 16-tap using fulladder1.

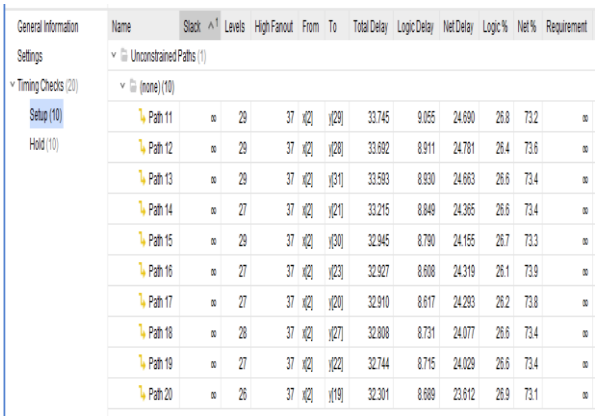

Fig.13: Delay for MAC based FIR filter for 16-tap using fulladder2.

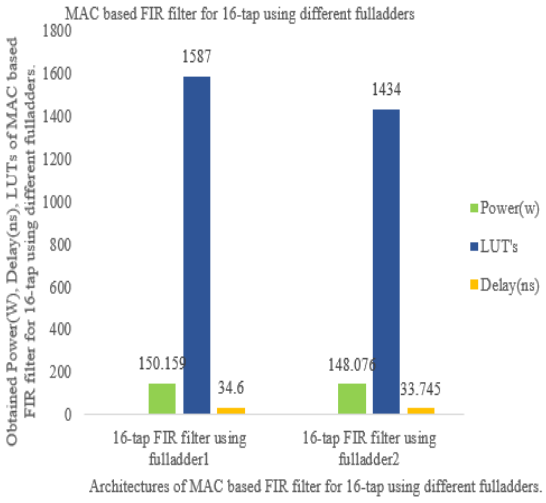

Fig.14: Comparison between Power, Delay and LUT's of MAC based FIR filter for 16-tap using fulladder1 and fulladder2.

TABLE 1: LUT's, Delay and Power for MAC based FIR filter for 16-tap using fulladder1 and fulladder2.

S.NO	ARCHITECTURE OF DIFFERENT FULL ADDERS	LUT's	DELAY (ns)	POWER (W)
1	FIR Filter using Full adder1	1587	34.600	150.159
2	FIR Filter using Full adder2	1434	33.745	148.076

VII. CONCLUSION

The implementation of MAC based FIR filter using CSLA dominated by carry generation logic adder and Square Architecture Based Vedic Multiplier using Multiplexer Based Full Adders are designed. Simulations and synthesis results are done using Vivado 2017.3 software. MAC based FIR filter for 16-tap using Full adder 2 has better reduction in power consumption i.e. 1.3871% in terms of watts, Combinational delay i.e. 2.4710% in terms of milliseconds and the overall LUT's i.e. 9.6408% than the MAC based FIR filter for 16-tap using fulladder1.

VIII. FUTURE SCOPE

Design can be further extended by using higher order taps.

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