Anjana Goen, et. al. International Journal of Engineering Research and Applications
www.ijera.com
ISSN: 2248-9622, Vol. 10, Issue 7, (Series-III) July 2020, pp. 46-50

RESEARCH ARTICLE OPEN ACCESS

FPGA Based Digital Phase Locked Loop using VHDL Coding

Anjana Goen[1], Akarshika Singhal[2]
[1]*Associate Professor, Department of Electronics & Communication Engineering, Tekanpur, Gwalior, India*
[2]*Graduate Student, University of Baltimore County, Maryland, USA*

Abstract PLL is contributing vital role in advancement in electronic and digital communication since 1932. In analog television receivers since at least at late 1930s, phase locked loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal. PLL may be implemented either in analog circuit or in digital circuits. Analog and digital PLL circuits consists of four basic element i.e phase detector, low pass filter , variable frequency oscillator and feedback path. There are several variation of PLL, DPLL is one of the variation. This paper gives basic details and design of DPLL by using edge trigger JK as phase detector and NCO in VHDL using Xillinx.

Index Terms—DPLL (Digital Phase Locked Loop), PLL (Phase Locked Loop), NCO (Numerically Controlled Oscillator), VHDL (Very high speed integrated circuits Hardware Description Language)

Date of Submission: 23-06-2020 Date of Acceptance: 11-07-2020

I. INTRODUCTION

Phase Locked Loop generates an output signal whose phase is related to the phase of an input signal. The simplest PLL is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. Keeping the input phase and output phase in lock step also implies keeping the input and output frequencies the same. Phase-locked loops are widely employed in radio, telecommunications and other electronic applications. A single IC can provide a complete phase-locked-loop building block; the technique is widely used in modern electronics devices [2], [5], with output frequencies from few hertz to gigahertz. An analog PLL with a digital phase detector as edge-trigger JK [3] and may have digital divider in the loop as NCO. Phase-locked loops are widely used for synchronization purpose, demodulate frequency-modulated signals [1],[4], [14].

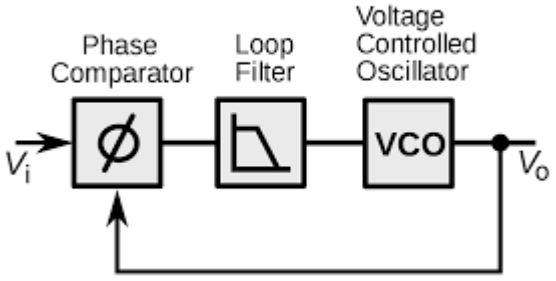

Fig.1 General block Diagram of PLL

II. DPLL DESIGN

2.1 Block Diagram

Block diagram of DPLL consists of digital blocks. It takes digital signal only as input signal. Structure of DPLL consists of three basic blocks Phase Detector, Loop filter and NCO [6]. Fig. 1 gives basic block of PLL. The main aim of DPLL is to make synchronization among the phase of input signal and output signal and also the frequency [23]. Phase detector is used to reduced the signal error differences among two signals, loop filter is used to removed the noise and the output of NCO is used to make the output signal closer to the input signal.

2.2 Phase Detector

Phase Detector is also known as Phase Comparator it makes comparison between input signal and NCO output signal. In this paper the Phase Detector is design by using Edge triggered JK flip-flop. It contains a JK flip flop. These circuits have the advantage that whilst the phase difference is between $\pm$ 180˚ a voltage proportional to the phase difference. AC components are not produced when the loop is out of lock and the output from the phase detector can pass through the loop filter to bring the PLL into lock [23].

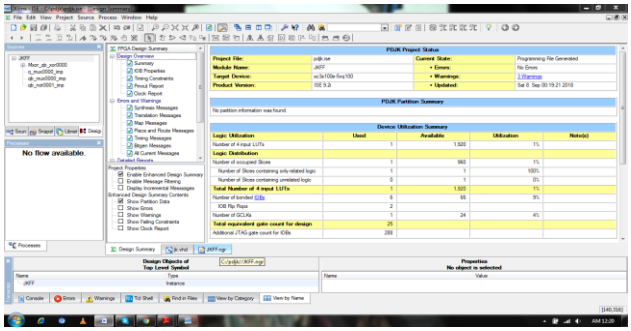

Fig.2 Design Utilization Summary of Phase Detector

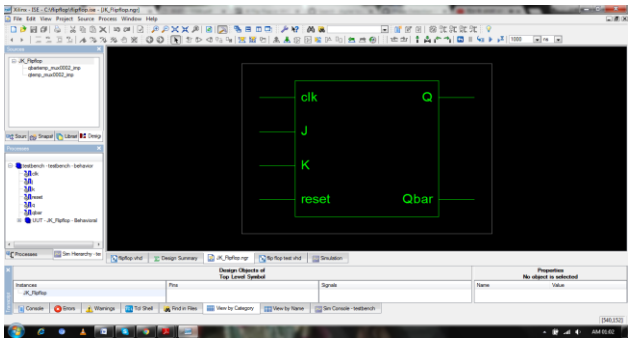

Fig. 3a RTL Schematic of Phase Detector

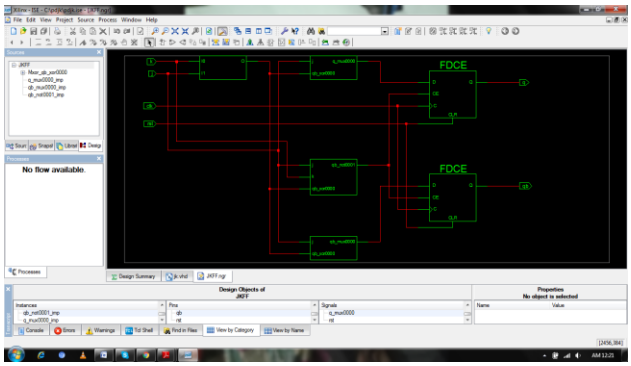

Fig. 3b RTL Schematic of Phase Detector

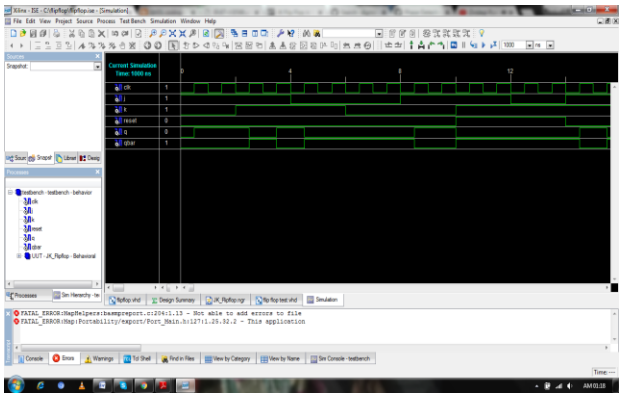

Fig.4 Output waveform of Phase Detector

2.3 Loop Filter

Loop filter is an integrator. It is crucial to the operation of the whole PLL. The PLL filter is needed to remove any unwanted high frequency components which might pass out of the phase detector and appear in the NCO tune line[24]. They would then appear on the output of the NCO, NCO as spurious signals. The filter also affects the ability of the loop to change frequencies quickly. If the filter has a very low cut-off frequency then the NCO will not be able to change its frequency as fast, conversely a filter with a higher cut-off frequency will enable the changes to happen faster. The loop filter also governs the stability of the loop. If the filter is not designed correctly then large signals will appear on the tune line.

In this paper the Loop Filter is designed with the help of UP/ down counter because it is very simplest loop filter. It is incremented on each up pulses and decremented on each down signals and for getting clock and direction signal pulse forming circuit is used. So its work line now behaves as an integrator.

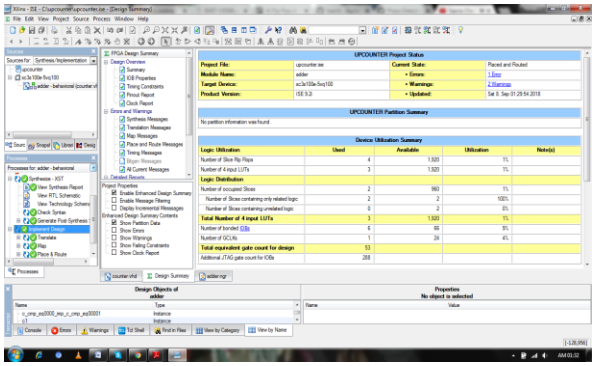

Fig. 5 Device Utilization Summary of Loop Filter

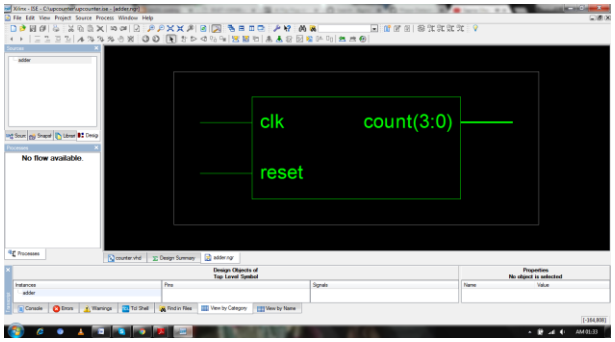

Fig. 6a RTL Schemantic of Loop Filter

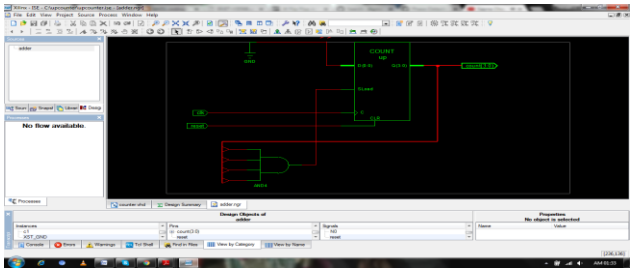

Fig. 6b RTL Schemantic of Loop Filter

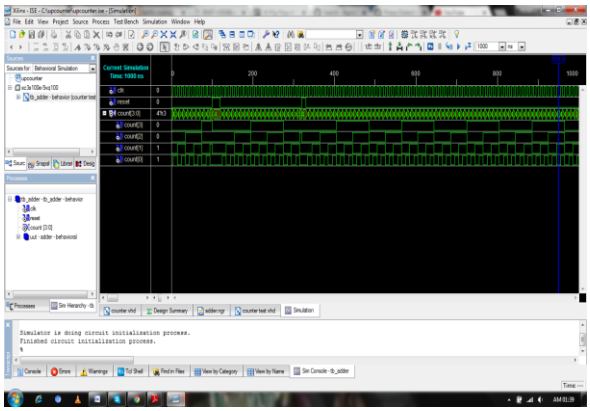

Fig. 7 Output Waveform of Loop Filter

2.4 NCO (Numerically Controlled Oscillator)

A numerically controlled oscillator is a digital signal generator which creates a synchronous, discrete-valued representation of a waveform usually sinusoidal. NCO are often used at the output to create a DDS. NCO offers accuracy, stability and reliability.

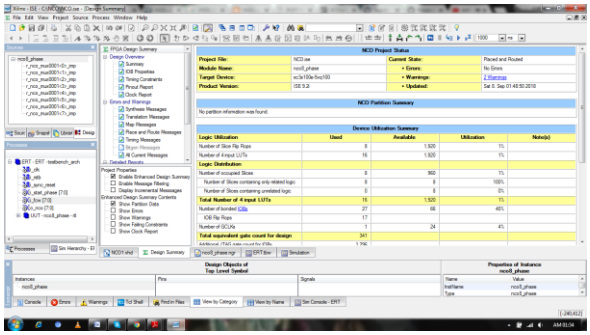

Fig. 8 Device utilization summary of NCO

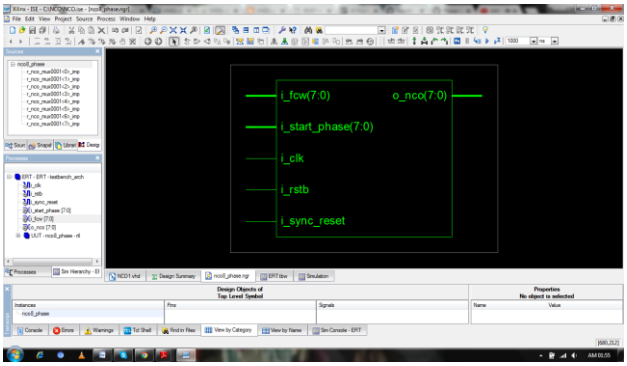

Fig.9a RTL Schematic of NCO

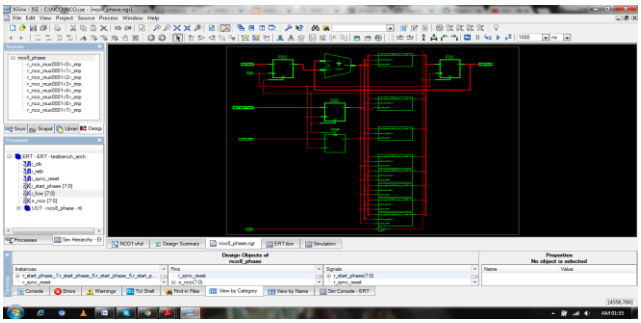

Fig.9b RTL Schematic of NCO

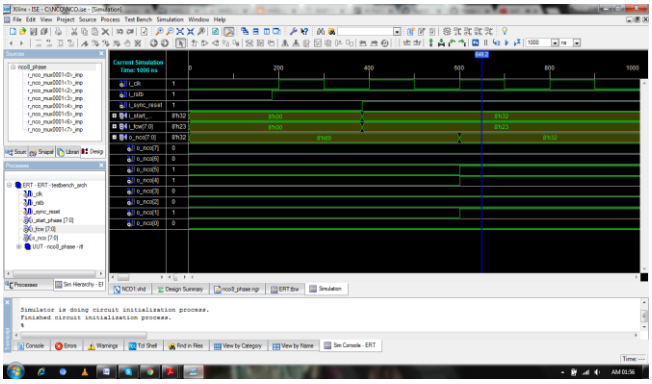

Fig. 10 Output waveform of NCO

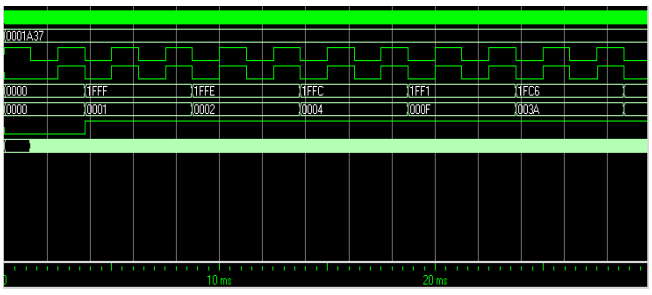

Fig. 11 Overall DPLL output

III. CONCLUSION

An important aspect of using this circuit, is that once the phase locked loop has found the desired frequency, noise in the received signal causes only very small (random) changes in the input clock. The regenerated clock continues to provide a good reference that may be used to find the center of each received bit [21].

REFERENCES

[1]. A. H. Khalil, K. T. Ibrahim, and A. E. Salama, "Digital of ADPLL for good phase and frequency tracking performance," in *Proc. of the Nineteenth National Radio Science Conference (NRSC 2002)*, Alexandria, pp. 284 – 290, March 2002.

[2]. N. Rahmatullah, "Design of All Digital FM Receiver Circuit," Project report in Institute Technology Bandung, Indonesia, March, 2005.

[3]. C. H. Shan, Z. Chen, and Y. Wang, "An All Digital Phase-Locked Loop Based on Double Edge Triggered Flip-flop," in *Proc. of 8th IEEE International Conference on Solid-State and Integrated Circuit Technology, (ICSICT '06)*, China, pp. 1990-1992, 2006.

[4]. M. J. P. Brito and S. Bampi, "Design of a digital FM demodulator based on a 2nd-order all digital phase locked loop," *Journal of Analog Integrated Circuit and Signal Processing*, Springer, Netherland, May 28 2008, Numbers 1-2/November 2008.

[5]. I. Hatai and I. Chakrabarti, "FPGA implementation of Digital FM Modem," *IEEE International Conference on Information and Multimedia Technology, ICIMT'09*, India, pp. 475 – 479, *2009*.

[6]. M. Kumn and H. Klingbeil, "An FPGA-Based Linear All- Digital Phase-Locked Loop," *IEEE Trans. on circuit and systems*, vol. 57, no. 9, September 2010.

[7]. T. Y. Yau and T. Caohuu, "An Efficient All-Digital Phase-Locked Loop with Input Fault Detection," in *Proc. of IEEE conference, Information Science and Applications (ICISA)*, 2011.

[8]. R. E. Best, *Phase Locked Loops Design Simulation and Applications*, McGraw-Hill Professional, ch. 6, pp. 205-246, 5th Edition, 2003.

[9]. A. Babu and B. Daya, "All Digital Phase Locked Loop Design and Implementation," Project report, University of Florida, Gainesville, FL, 32608, USA.

[10]. A. Chandra, "Phase Locked Loop," presentation in ECE Department, NIT Durgapur, Winter School on VLSI Systems Design, WB, Jan 24, 2009.

[11]. S. Vallabhaneni, S. Attri, N. Krishman, S. Sharma, and R. C. Chauhan. Design of an all-Digital PLL core on FPGA. [Online]. Available: http://klabs.org/mapld04/abstracts/sharma_a.doc

[12]. S. C. Hong, "An all digital phase-locked loop system with high performance on wideband frequency tracking," *IEEE Trans. on Circuit and* Systems, vol. 52, no. 10, 2009.

[13]. Q. Zhang, "Research and application of all digital phase locked loop," in *Proc. of the Second International Conference on Intelligent Networks and Intelligent Systems*, USA, pp. 122 – 125, 2009.

[14]. J. Pablo, M. Brito, and S. Bampi, "Design of a digital FM Demodulator based on a 2nd order All-digital Phase Locked Loop," in *Proc. of the 20th Annual Conference on Integrated Circuits and Systems Design (SBCCI'07),* New York, pp. 137 – 141, 2007.

[15]. Staszewski, *et al*., "All-digital PLL and transmitter for mobile phones," *Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2469-2482, Dec. 2005.

[16]. C. C. Chung and C. Y. Lee, "An all-digital phase-locked loop for high-speed clock generation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 347-351, Feb. 2003.

[17]. Z. J. Cheng, D. Q. Jin, and T. Kwasniewski, "A 4GHz Low Complexity ADPLL-based Frequency Synthesizer in 90nm CMOS," in *Proc. of IEEE Custom Integrated Circuits Conference, CICC '07*, Ottawa, pp. 543-546, 2007.

[18]. R. B. Staszewski, C. M. Hung, K. Maggie, J. Walberg, D. Leipold, and P. T. Balsara, "All-digital phase-domain TX frequency synthesizer for Bluetooth radios in 0.13µm CMOS," in *Proc. of IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, Texas Instruments, Dallas, TX, USA, pp. 272 – 527, Feb. 2004.

[19]. G. N. Sung, S. C. Liao, J. M. Huang, Y. C. Lu, and C. C. Wang, "All –Digital frequency synthesizer Using a Flying adder," *IEEE Transactions on Circuits and Systems*, vol. 57, no. 8, pp. 597 – 601, Aug. 2010.

[20]. A. R. Qureshi, "Implementation of low power, wide range ADPLL for video applications," Master Degree Thesis, Linkoping University, Department of Electrical Engineering, Electronics System.

[21]. T. Y. Hsu, B. J. Shieh, and C. Y. Lee, "An ADPLL-based Clock Recovery Circuit," *IEEE*

Journal of Solid-State Circuits, vol. 34, no. 8, pp. 1063-1073, 1999.

[22]. Y. R. Shayan and T. L. Ngoc, "All Digital phase-locked loop: concepts, design and applications," *Radar and Signal Processing*, vol. 136, no. 1, pp. 53 – 56, Feb. 1989.

[23]. Tanu Trushna Mohapatra, and Madhusmita Panda, "FPGA Implementation of CORDIC Based ADPLL for Signal Processing Application", International Conference on Systemics, Cybernetics and Informatics (ICSCI 2014), CS-3.1, pp.01-07, 2014.

[24]. Akarshika Singhal, Anjana Goen and Tanutrushna Mohapatra, "FPGA Implementation and Power Efficient CORDIC based ADPLL for Signal Processing and Application", 2017 7th International Conference on Communication Systems and Network Technologies ©2017 IEEE pp. 325-319.

Anjana Goen, et. al. "FPGA Based Digital Phase Locked Loop using VHDL Coding". *International Journal of Engineering Research and Applications (IJERA)*, vol.10 (07), 2020, pp 46-50.