RESEARCH ARTICLE OPEN ACCESS

Modeling of Plasma Etching Reactors based on Numerical Study

1st Shyamal Kumar Roy
Assistant Professor, Department of Electrical Engineering, Guru Nanak Institute of Technology
157/F, Nilgunj Road, Panihati, Kolkata– 700114, West Bengal, India.

2nd Suman Ghosh
Assistant Professor, Department of Electrical Engineering, Guru Nanak Institute of Technology
157/F, Nilgunj Road, Panihati, Kolkata– 700114, West Bengal, India

ABSTRACT
The paper presents research in the understanding of how the manufacturing control parameters affect the physical processes inside low pressure plasma etch reactor. The flow inside the reactor varies from continuum flow to near free molecular flow. In addition, electromagnetic effects are important due to r_f heating, magnetic confinement, and wafer potential bias acceleration. Numerical simulation allows the full characterization of both neutral and ion behavior inside the reactor. With simulation, it is also possible to study etch reactor design changes before building of hardware.
Keywords: silicon Etching, DSMC, SAC process, CF gas

Date of Submission: 01-10-2020 Date of Acceptance: 14-10-2020

I. BACKGROUND (PLASMA ETCH REACTOR)

Plasma etch is the use of a plasma, generated with suitable gases, to chemically remove material from the wafer surface. So the plasma etch is to reproduce the etch mask in the film on the surface of the wafer or to chemically remove material from the wafer surface in a less specific way. The mask pattern may be transferred to a film or stack of films that have been deposited on the wafer or etched into the silicon wafer itself. For many critical manufacturing steps, the etch process must also be able to shape the feature being produced on the wafer surface in a specified way. Plasma etch is also used to chemically remove films that completely cover the wafer. The most critical application of plasma etch, which results in properly shaped features produced on the wafer.

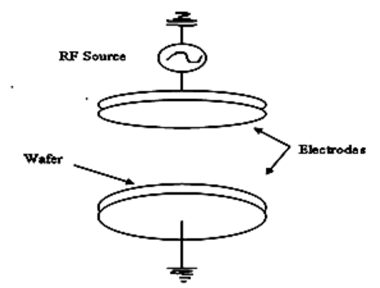


Fig 1. Schematic Diagram of Plasma Etch Reactor

The plasma etch process includes both the chemical removal of material and the deposition of a thin coating of material to protect selected areas and assist in creating the desired features on the wafer. Physical bombardment of the wafer with accelerated ions is often utilized to assist in the process although there are several plasma etch operations that do not require bombardment

II. ABOUT PLASMA SILICON ETCHING

The progress of digital electronics and information technology based on silicon devices that followed the 1947 invention of the transistor at Bell laboratories is unprecedented in the history of technology. The driving force behind this progress has been the miniaturization of devices during the past few decades. Low pressure radio frequency (rf) glow discharges, called low temperature plasmas, has been widely used in the fabrication of microelectronic devices and the manufacture of new materials. Unlike dc glow discharge plasmas, low temperature r.f. plasma are maintained even in an electrode less chamber as well as between metallic and dielectric electrodes. They are used to produce chemically activated neutrals and ions responsible for surface reactions I plasma etching and in plasma chemical vapor deposition.

In silicon fabrication, chemical removal of polysilicon or amorphous silicon and silicon nitride layers can be performed using both wet and dry etching techniques. Dry etching is especially well-suited for precise line width and profile and nanostructure fabrication. However, wet etching still plays an important role where line size or profile control is not critical, or where the removal of a blanket film is required. For such applications, wet etching can offer advantages of high etch rate combined with high selectivity to dissimilar material layers, while avoiding the problem of plasma or radiation damage that may be present in dry etching techniques.

III. INTRODUCTION

Micro-electronic circuits wafers are typically manufactured using plasma etch reactors. Manufacturing is accomplished by depositing layers of conducting or insulating material onto a silicon wafer and then etching circuit features into them. The etch process involves bombarding the silicon wafer with a reactive neutral gas and an ion stream in a near-vacuum condition to carve out circuit features in a preferred direction. In order to improve the manufacturing process, increase yield, and raise quality, the flow field inside a chlorine plasma etch reactor is under study.

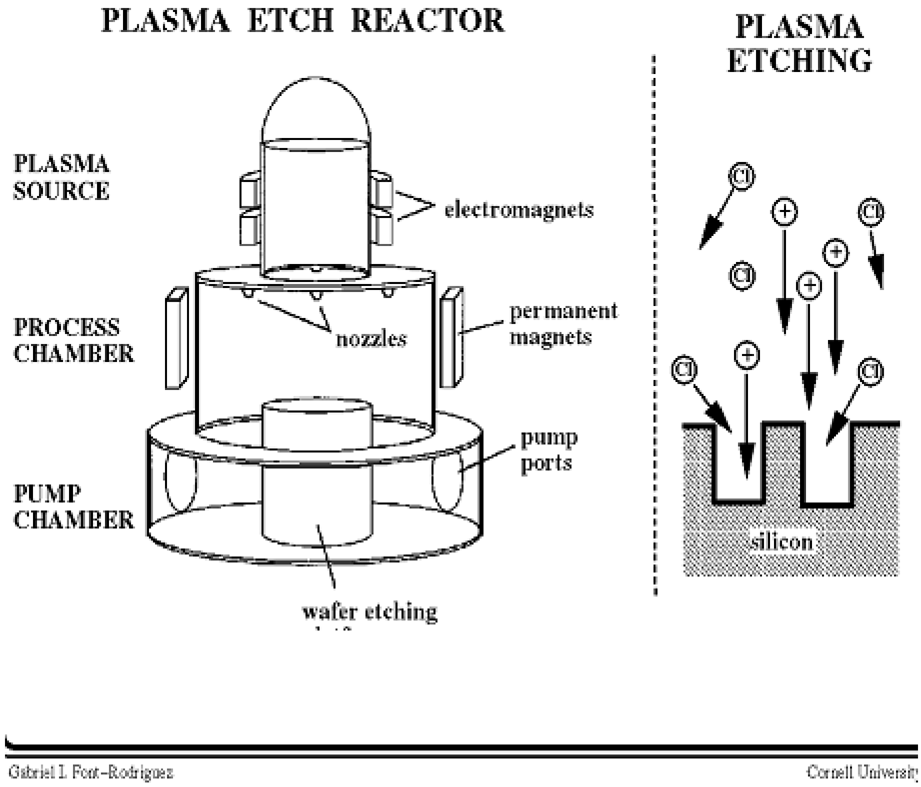


Fig 2. Schematic of Typical Plasma Etch Reactor with the Process of Silicon Etch

IV. RESEARCH PBJECTIVES AND IMPACTS

The general objective of the proposed work is to develop and research is to aid in the understanding of how the manufacturing control parameters affect the physical processes inside a low pressure plasma etch reactor. The flow inside the reactor varies from continuum flow to near free molecular flow. In addition, electromagnetic effects are important due to rf heating, magnetic confinement, and wafer potential bias acceleration. In order to correctly model the convective and diffusive transport as well as the chemistry and electromagnetic effects, particle methods (DSMC-PIC) are used. Computations are carried out on a massively parallel architecture IBM SP2. The work is done in collaboration with industrial partners who provide the specifics of reactor design and experimental data. Numerical simulation allows the full characterization of both neutral and ion behavior inside the reactor. With simulation, it is also possible to study etch reactor design changes before building of hardware.

V. TECHNICAL APPROACHES

The objective of the proposed work is to develop and provide numerical solutions to each specific etching parameter configuration of the circuit component.

- Etching process and Selecting of a Nozzle
- Dimensions
- Shape
- Material
- Flux
- Mass of the material etched and deposited.

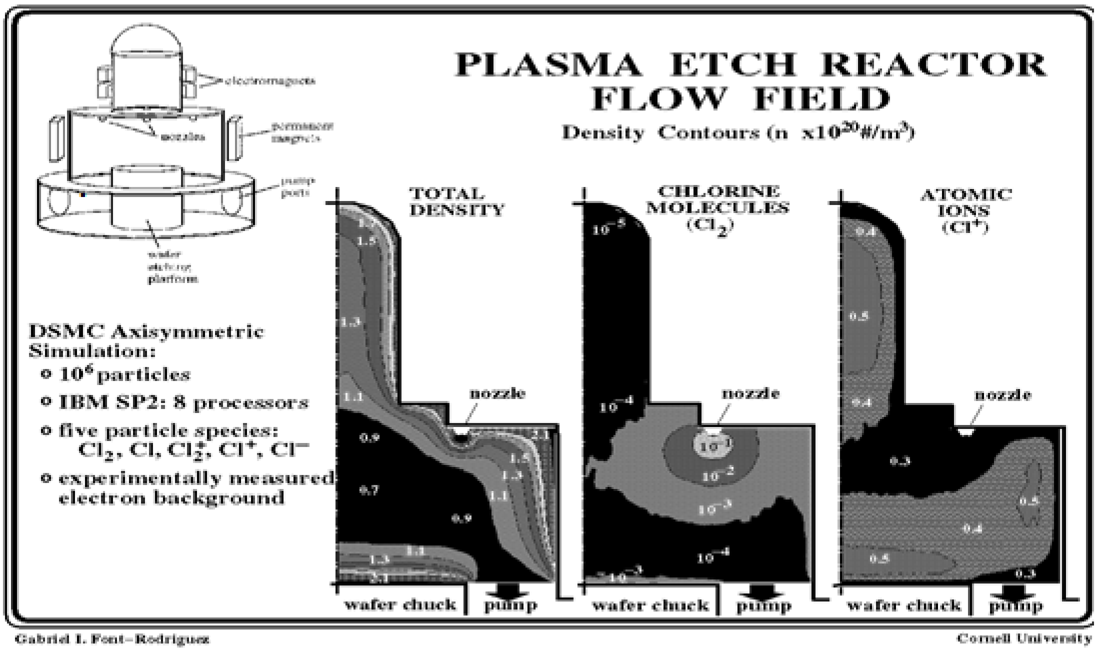


Fig 3. Plasma Etch Reactor Flow Field

A. Etching Process

The semiconductor processing technology field reactive ion etching (RIE) that realized a directional etch profile without an undercut for fine line delineation was developed. Now a days most popular etching SiO2 with SAC (self aligned contact) process, especially the RIE system and the high selective SiO2 etching applying to the SAC process. The selective etching of SiO2 over Si was performed by fluorocarbon (CF) gas. The process in the RIE with CF4 and H2 gas mixture as shown in figure 4, where H2 flow rate increasing and Si flow rate decreasing, so the ratio of flow rate H2/CF4 = 70%. The results shown us SiO2 high selective condition, the Si surface is covered by a CF thin film, so the CF thin film protected the surface from ion bombardment. CF gave very high selectivity between the films; even CF caused film deposition on the oxide. Based on the ion beam experiment results, it was investigated that the plasma chemistry utilizing C4F8 gas in the magnetron RIE. C4F8 gas was decomposed as follows:

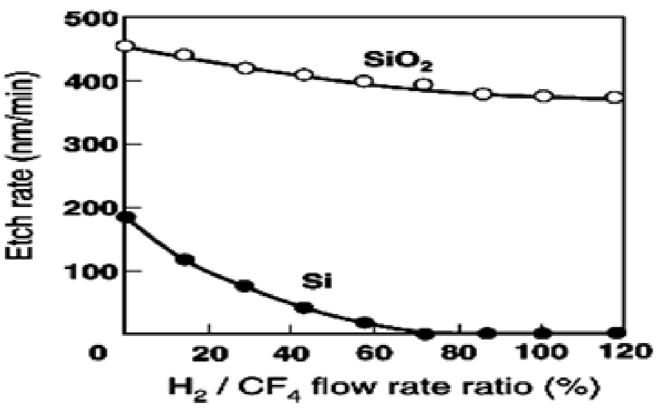


Fig4. Figure 4 Etch rate SiO2/Si in RIE as a function of CH4 and H2 Gas mixture ratio

ISSN: 2248-9622, Vol. 10, Issue 10, (Series-II) October 2020, pp. 01-05

C4F8 → C2F4 → CF2

CF2 → F → CF3

CF2 → F → CF

TABLE I. GAS FLOW RATE CONDITIONS

Gas	C4F8
Flow Rate	5
SiO2	5

Plasma etching in the project we used reactor setup of 27 MHz radio frequency (RF) excited capacitive coupled plasma (CCP) source with some diagnostics. Gas and flow rate C4F8 was 11 sccm (standard cubic centimeter), Gas pressure 30 mTorr,

800 KHz wafer bias and top plate mat was Si and C. RF and CCP as a reference for the tool evaluation, because it is very high etch performance and its uniformity of plasma in the narrow gap makes it easier to analysis the reactions in the gas phase and surface.

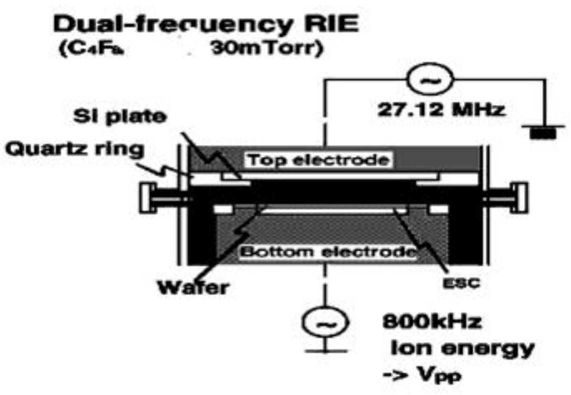


Fig5. Reactor Setup

B. Selecting of a Nozzle

The parameters for the plasma reactors in figure 3 used in the project were summarized in Table 1. It is not easy to compare them since many external parameters are so different in each tool, such as the volume, gases, flow rate, pressure, etc. However, the table shows some interesting aspects for controlling processing plasma.

C. Summary

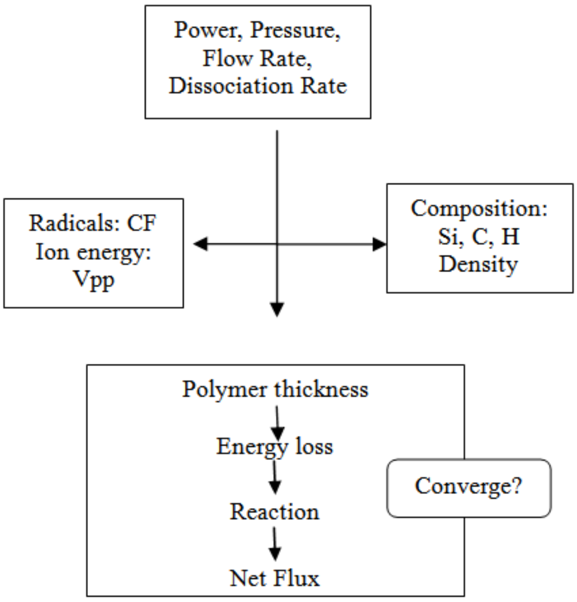
The following is the summery of the investigated

1. Etching rate would be considered for deposition rate.
2. Plasma growth technique used, rate of growth inversely related to temperature.
3. Selection of opening shielding spot.
4. Logical calculation for the parameters.
5. How much material to etch.
6. A magnetron RIE tool and an SAC hole process were introduced as tropics for the technology evolution. This research conducted on the SiO2 etching using CF plasma. The CF gas molecule is proposed as important parameters to control the gas dissoSciation and etch species flux to the surface. An etch reaction model was proposed and successfully predicted the etch rates of Si containing materials. Requirements for the development of next generation etch tools were discussed.

VI. CONCLUSIONS

For flow field inside plasma etch reactor, impressive experimental techniques exist that can be used to obtain the information required to develop a quantitative description of plasma-surface interactions relevant to plasma etching. A strong need exists to develop and employ beam sources of realistic plasma species in order to facilitate controlled investigations of relevant plasma-surface interactions. An improved understanding of the interaction of specific reactive particles with a surface and the synergistic effects that become important when several species react simultaneously, coupled with modeling should make it possible to identify key mechanisms. The situation is not as promising for microstructures. Novel phenomena that are absent for surfaces occur in microstructures and ultimately determine the usefulness of a particular plasma process. Significant efforts will be needed to further develop means to establish particle fluxes and identify fundamental surface processes in microstructures as a function of microstructural dimensions.

VII. NUMERICAL SOLUTIONS



REFERENCES

[1]. Yeh, C. P., Zhou, W. X., and Wyatt, K., "Parametric Finite Element Analysis of Flip Chip Reliability," *Proceedings of 1995 IEPS Conference*, pp. 297-306, 1995.

[2]. Font, G.I. and Boyd, I.D., "Numerical Study of Reactor Geometry Effects on a Chlorine Plasma Helicon Etch Reactor," Journal of Vacuum Science and Technology A, Vol. 15, 1997, pp. 313-319.

[3]. Nguyen, L., Chen, A., and Lo, R., "Interfacial Integrity in Electronic Packaging," *Application of Fracture Mechanics in Electronic Packaging and Materials*, EEP-Vol. 11, pp. 35-44, ASME, 1995.

[4]. H. Abe, Y. Sonobe, T. Enomoto, Jpn, J. Appl. Phys. 12 (1973) 287.

[5]. R.A. Heineeke, Solid State Electron, 19 (1976) 1039.

[6]. Semiconductor Industry Association, Int, Technology Road map for Semiconductors '99, San Jose, 1999. http://public.itrs.net;

[7]. M.N. Hirsh, H.J. Oskam (Eds), Gaseous Electronics, Vol. 1, Electrical Discharges, Academic Press, New York, 1978.

Shyamal Kumar Roy, et. al. "Modeling of Plasma Etching Reactors based on Numerical Study." *International Journal of Engineering Research and Applications (IJERA)*, vol.10 (10), 2020, pp 01-05.