

## FPGA Implementation of an Algorithm to Identify a BPSK (Barker) signal

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### Abstract—

Modern radars use phase modulated signals to spread their spectrum to improve the processing gain. The Identification of the modulation format of a detected signal, the intermediate step between signal detection and demodulation, is a major task of an intelligent receiver, with various civilian and military applications. Obviously, with no knowledge of the transmitted data and many unknown parameters at the receiver, such as the signal power, carrier frequency and phase offsets, timing information, etc., blind identification of the modulation is a difficult task. This becomes even more challenging in real-world scenarios. An algorithm is designed to identify the BPSK (Barker) signal using an STFT Process and calculating the chip rate from the spectrum.

*Keywords*—Radars, ADC, Barker, STFT, Signal Identification

### I. INTRODUCTION

Modern radars use phase modulated signals to spread their spectrum to improve the processing gain. There are several approaches of using the phase modulation. The phase change can be  $\pi$ ,  $\pi/2$ ,  $\pi/4$ , and so forth. When the phase change is  $\pi$ , it is referred to as biphas shift keying (BPSK). Communication signals use various types of phase modulations, this paper is mainly for BPSK because it is more popular in radar applications. It is important to detect the existence of a BPSK signal for an electronic warfare (EW) receiver. The detection of a BPSK signal can help identify the radar type, which is important information. If more information can be obtained from the signal, the identification approach can be easier. In this study the requirements are to detect the existence of a BPSK signal and find the frequency and its chip time (or chip rate). The chip time is the shortest time between two consecutive phase shifts in a BPSK signal and the chip rate is the inverse of the chip time.

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various civilian and military applications. Obviously, with no knowledge of the transmitted data and many unknown parameters at the receiver, such as the signal power, carrier frequency and phase offsets, timing information, etc., blind identification of the modulation is a difficult task. This becomes even more challenging in real-world scenarios. So a new method has been developed to identify the Bpsk (Barker) signal. This is achieved using an STFT Process and by calculating the chip rate from the spectrum.

### II. BARKER CODES

In 1953, R. H. Barker presented binary sequences for synchronization purposes in telecommunications the binary Barker sequences are finite length, discrete time sequences with constant magnitude, and a phase of either  $\phi_k = 0$  or  $\phi_k = \pi$ . The formal definition of a Barker sequence is given below

#### Definition

A Barker sequence is a finite length sequence  $A = [a_0, a_1, \dots, a_n]$  of  $+1$ 's and  $-1$ 's of length  $n \geq 2$  such that the aperiodic autocorrelation coefficients (or side lobes) satisfies  $|r_k| \leq 1$  for  $k = 0$  and similarly  $r_{-k} = r_k$

The Barker code is a short sequence and popular for radar applications. The Barker codes have different sequence lengths. The side lobes generated from the autocorrelation of the Barker code have constant amplitude. The maximum length of a Barker code is limited to 13

Consequently, a binary Barker sequence has elements  $a_i \in \{-1, +1\}$ , which are only known for lengths  $N_c = 2, 3, 4, 5, 7, 11, \text{ and } 13$ . The longest code is of length  $N_c = 13$ . The nine sequences are listed where a  $+1$  is represented by a  $+$  and a  $-1$  is represented by a  $-$ . It has been shown that binary Barker sequences with lengths greater than 13, with  $N_c$  odd, do not exist. Also, it has been proven that binary Barker sequences with  $4 < N_c < 1, 898, 884$  with  $N_c$  even do not exist. It has been conjectured that sequences with  $N_c \geq 1, 898, 884$  with  $N_c$  even also do not exist.

is not possible as it contains several peaks in a particular bin, but the frequency or phase will be calculated at every bin

number as a result of which several frequencies and phases are missed using an fat, This is the main reason why we have designed STFT process for time to frequency conversion of a signal

#### IV ALGORITHM FOR THE IDENTIFICATION OF BARKER SIGNAL

A BPSK signal is generated and the basic properties will be studied. Once the signal is generated STFT will be performed on the signal. The purpose of this operation is to find the time to frequencydomain conversion of a BPSK (Barker) signal. The Algorithm for the identification of a Barker Signal is given below

BARKER CODE	PHASE SHIFT
BARKER_2	+ -
BARKER-3	+ + -
BARKER-4	+ + + -
BARKER-5	+ + + - +
BARKER-7	+ + + - - + -
BARKER-11	+ + + - - - + - - + -
BARKER-13	+ + + + - - + - - + -

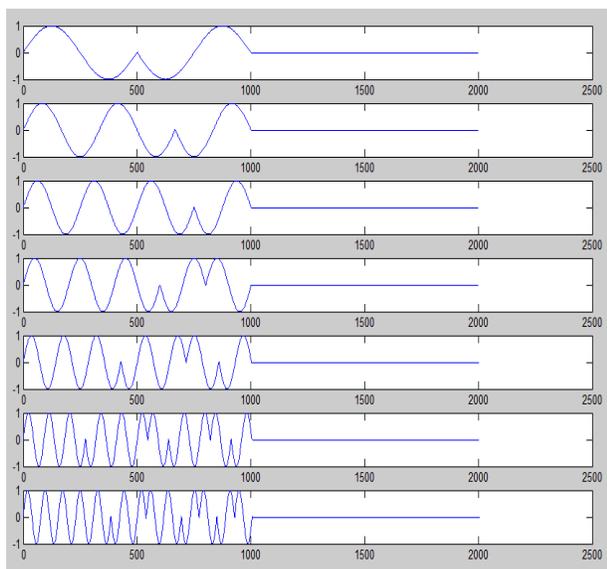


Fig 1 Barker Signal

#### III SHORT TIME FOURIER TRANSFORM(STFT)

Short time Fourier Transform is a process, which involves repetitiveFFT operations for small intervals of time. The given time period is divided into 'n' number of slots where 'n' is the no of samples/ No of Point FFT, Therefore the time resolution for the calculation of FFT is ' T/n' where T is the Total time period of the received signal.

STFT is used to know the phase and the frequency at different instants of time so that the signal modulation type is possible whereas in FFT the frequency and phase calculation

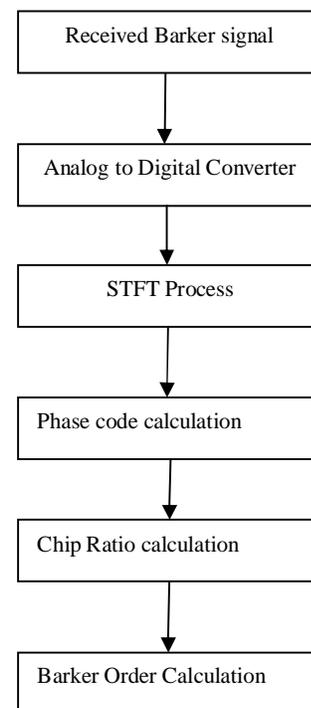


Fig 2 Barker signal identification design flow

#### ALGORITHM

- i. Received Bpsk (Barker) signal is converted into a digital signal using an ADC.
- ii. An STFT operation is performed on the digital Bpsk Signal
- iii. The amplitude (Magnitude) and the Frequency (Index) values are processed in the analysis block.

- iv. Read the amplitude and index for each frame
- v. Calculate the bin number corresponding to the peak amplitude
- vi. Calculate the amplitude for the 4 bin numbers before and after the max bin number
- vii. Calculate the min/max ratio for the above bin numbers
- viii. Now compare the min/max ratios with respect to the threshold
- ix. If min/max greater than threshold than phase shift occurs
- x. The Chip rate for the Code formed from the different frames is calculated.
- xi. The signal type can be classified using the chirp rate

code bits) .The Phase code is initialised to '0' and for every frame a phase shift (either 0 or 1) is concatenated as result of

which a complete phase code of 'n' bits is formed when  $i > n$  condition is satisfied.

The order of the Barker is calculated from the derived phase code using the Chip rate using the formula given below

$$\text{Barker order} = \text{no. of code bits } (n) / \text{chip rate}$$

Where chip rate is defined as the minimum number of frames (code bits) between any two phase shifts.

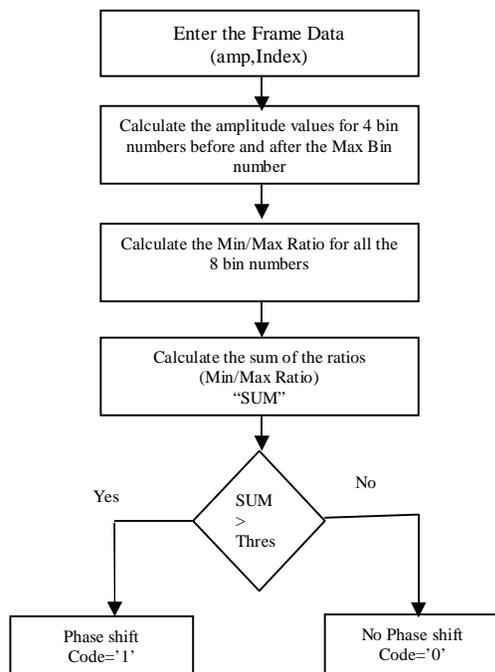


Fig 3 Phase shift calculation flow

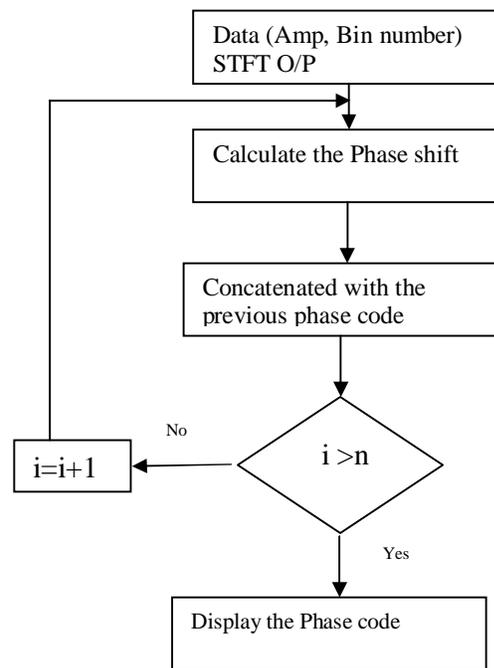


Fig4 Barker identification flow chart

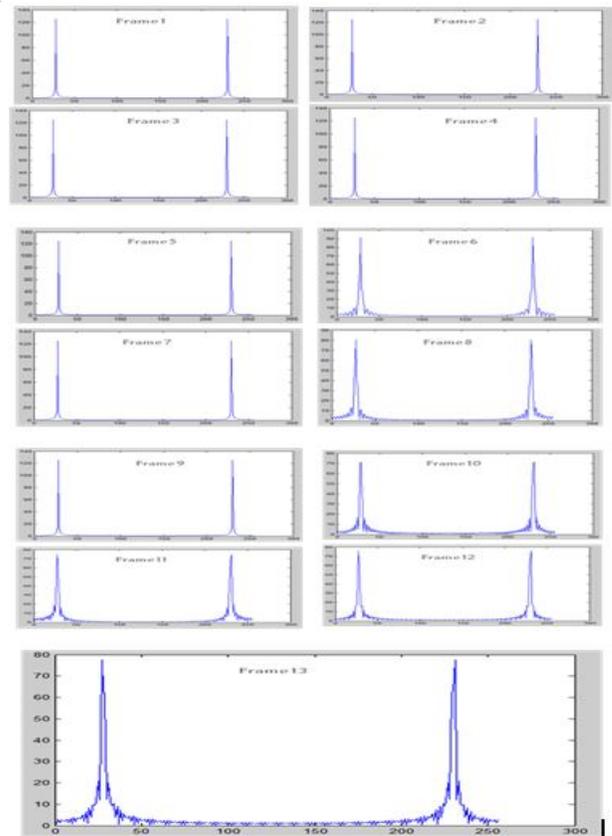
The above flow chart is used to calculate the phase shift, the inputs to this block are the magnitude(amp ) and bin number from the STFT and the output will be the phase shift '0' for no phase shift and '1' for phase shift .

The phase shift is calculated for every frame of data and a phase code is formed as per the flow chart show in figure 4. Here 'i' is an integer initialized to '1' and is incremented until it is greater than 'n' where 'n' indicates no of frames (no of

## V. RESULTS AND DISCUSSION

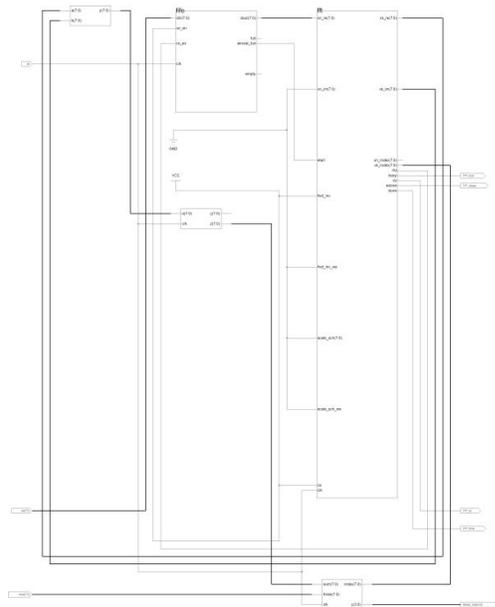
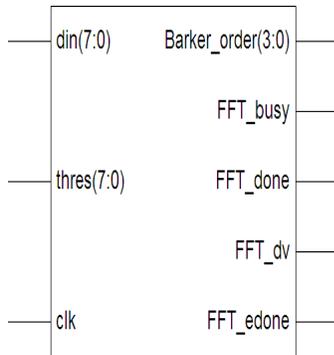
The algorithm is first modelled in Matlab to estimate the Hardware Resources. A sample Barker signal is generated in Matlab and applied as an input to the design. The Matlab results for the algorithm are shown below.

```
code =  
Columns 1 through 9  
1 1 1 1 1 1 1 1 1  
Columns 10 through 18  
1 1 1 1 1 1 1 1 1  
Columns 19 through 27  
1 1 1 1 1 1 1 1 1  
Columns 28 through 36  
1 0 0 0 0 0 0 0 0  
Columns 37 through 45  
1 1 1 1 0 0 0 0 1  
Columns 46 through 52  
1 1 1 0 0 0 0  
  
chip_rate_barker =  
4  
  
Frames =  
52  
  
barker_order =  
13  
  
*****The received signal is barker of order 13*****
```

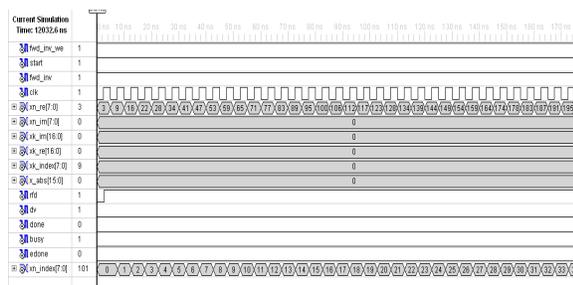


The Matlab generated Signal is given as input an Analog to digital converter and thus the obtained digital samples are given to the FPGA as an input. The algorithm consists of fifo , STFT operations to be performed and the obtained outputs are given to the Barker analysis block which classifies the type of Barker signal . The algorithm is designed using VHDL language , Synthesized in Xilinx 10.i ,Simulated in Xilinx ISIM 10.1 i. The synthesis and simulation results are show below

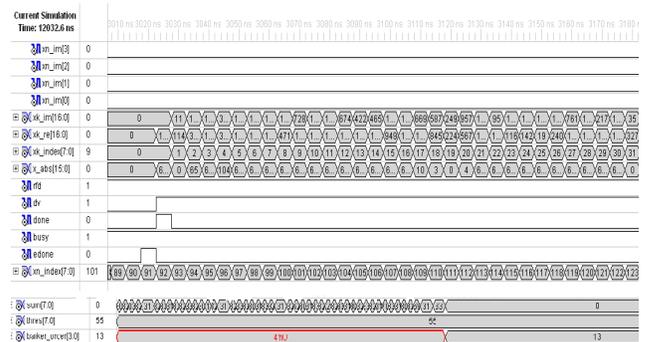
RTL Schematic:



Inputs



Outputs



## VI CONCLUSIONS

This paper describes an algorithm for the identification of BPSK (Barker) signal which is based on the time to frequency analysis.

DSP processors are used for implementing many of the DSP applications. Although DSP processors are programmable through software, the DSP processor hardware architecture is not flexible. Therefore, DSP processors are limited by fixed hardware architecture such as bus performance bottlenecks, a fixed number of multiply accumulate (MAC) blocks, fixed memory, fixed hardware accelerator blocks, and fixed data widths. The DSP processor's fixed hardware architecture is not suitable for certain applications that might require customized DSP functions implementations.

FPGAs provide a reconfigurable solution for implementing DSP applications as well as higher DSP throughput and raw data processing power than DSP processors. Since FPGAs can be reconfigured in hardware, FPGAs offer complete hardware customization while implementing various DSP applications. Therefore, DSP systems implemented in FPGAs can have customized architecture, customized bus structure, customized memory, and customized hardware accelerator blocks.

So keeping in view of the advantages of using FPGAs as compared to other customized devices this work can further be increased to the designing & implementation of a Barker Identification algorithm. The generosity of the design facilitates not only the rapid Signal Identification, but moreover, it explores the performance of different implementations in order to obtain the most suitable solution for a particular Electronic Warfare system. Some of the generic parameters of Barker Identification are, frequency (bin number), amplitude, chip rate, threshold, min/max ratio, sum of the ratios,

The Above design is implemented on Xilinx Virtex-5 SX240t

an virtex-5 Fx200t,an 8 bit ADC is used to covert the analog signal into a digital signal the IC used is ADC08D1520,Using these hardware the design implemented on the Fpga and the algorithm is verified and has given Accurate and efficient results.

The above algorithm is an efficient algorithm, which is technologically feasible for the fast interception of signals without any parameter extraction (Pulse width, Pulse Repetition Interval, direction of arrival). It outperforms the previous approaches in terms of speed, sensitivity, accuracy in the identification of a BPSK (Barker) signal.

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