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Analysis Of High Speed Wallace Tree Multiplier Using Compressors For DSP Applications

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ABSTRACT
Multiplication is an important arithmetic operation employed in digital systems and signal processing applications. Most of the multipliers are time, area and power consuming circuits. Improvement in any of these parameters will improve the efficiency of the circuit. But ever increasing demand for faster multipliers motivated several researchers to go a step ahead and present some novel approach. This work presents an analysis & approach towards the reduction of delay in the Wallace tree multipliers by using compressors with full adders and half-adders for partial product reduction. The proposed multiplier has been analyzed using Xilinx ISE Design Suite 7.1, Modelsim and Cadence Virtuoso tool.

***Keywords* :** Binary counter, Compressors, Cadence, Xilinx

I. INTRODUCTION

In present days speed, power and area are the important conflicts in VLSI design technology, because of ever increasing demand for the faster operations. Many technologies have been used to achieve high speed and low power [1] digital circuits and among that pass transistor logic has been intensively studied as a breakthrough for producing new advancement in the field of digital circuits. In digital systems architecture are well established in the literature to develop modern arithmetic processors and the use of latest innovations and advanced technologies dedicated to special logic circuits. Specifically multiplier design is critical in signal processing applications of digital system where it requires larger number of multiplications. The multiplication operation is used in digital system for various applications and multipliers are important part of systems like ALUs and DSP processors. The performance [2] of the system depends on the multiplier because they are often called the slowest components. So reduction of delay is important in this research.

Wallace tree multiplier is fast multiplier [3] compared to the available multiplier as they are used carry save addition algorithm for the final product addition. In multipliers if there is a small increase in speed will improve the operating frequency of a digital signal processor. Hence many attempts are done on multipliers to make it faster. When designing a multiplier, huge amount power and delay are generated, to minimize that, adders and compressor [4]are used. The proposed Wallace tree multiplier uses higher order compressors such as 3-2, 5-3 and 7-3 compressors to reduce delay and to achieve high-speed [5]. The higher order compressors are developed by merging binary counter property with compressor property. The design of wallace tree multiplier consist of three essential steps.

1. Generation of partial products
2. Reduction of partial products
3. Addition of reduced partial products to produce final product.

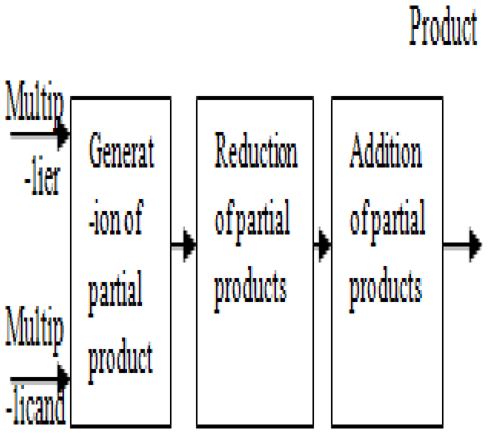

Product
Multip -lier
Multip -licand
Generat -ion of partial product
Reduction of partial products
Addition of partial products

Fig.1: Block diagram of Wallace tree multiplier

In multiplier design if speed is not a problem the design complexity can be reduced by adding partial products serially. For high speed multipliers, consider 16 bit partial products are generally added using Wallace tree method. In this approach generated partial products are compressed at each column into two or more bits.

II. ALGORITHM PROPOSED

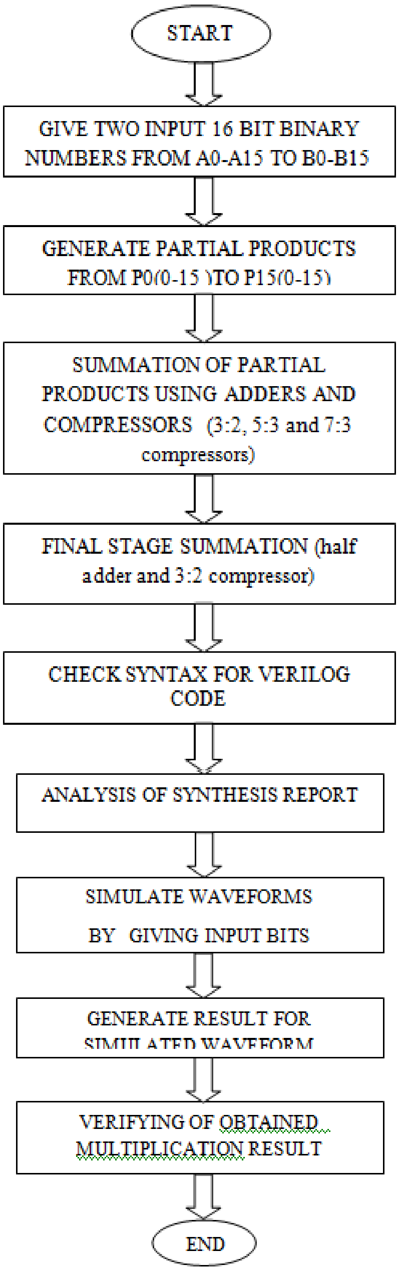

START
GIVE TWO INPUT 16 BIT BINARY NUMBERS FROM A0-A15 TO B0-B15
GENERATE PARTIAL PRODUCTS FROM P0(0-15)TO P15(0-15)
SUMMATION OF PARTIAL PRODUCTS USING ADDERS AND COMPRESSORS (3:2, 5:3 and 7:3 compressors)
FINAL STAGE SUMMATION (half adder and 3:2 compressor)
CHECK SYNTAX FOR VERILOG CODE
ANALYSIS OF SYNTHESIS REPORT
SIMULATE WAVEFORMS BY GIVING INPUT BITS
GENERATE RESULT FOR SIMULATED WAVEFORM
VERIFYING OF OBTAINED MULTIPLICATION RESULT
END

Fig.2: Algorithm proposed

III. PROPOSED WALLACE TREE MULTIPLIER ARCHITECTURE AND DESCRIPTION

The design of 16*16 Wallace tree architecture is shown in the Figure 3. In this architecture, addition of partial products including four stages. To limit the stage operations, adders along with various compressors are used. The utilization of adders and compressors in the partial product [6] reduction cautiously to limit the number of outputs generated. Consider line number ten where partial products are added using two 5-3 compressors at the first stage, produce six outputs. As a substitute of this using one 7:3 compressor and one full adder circuit produce five outputs. So that number of outputs propagated to the next stage will be decreased.

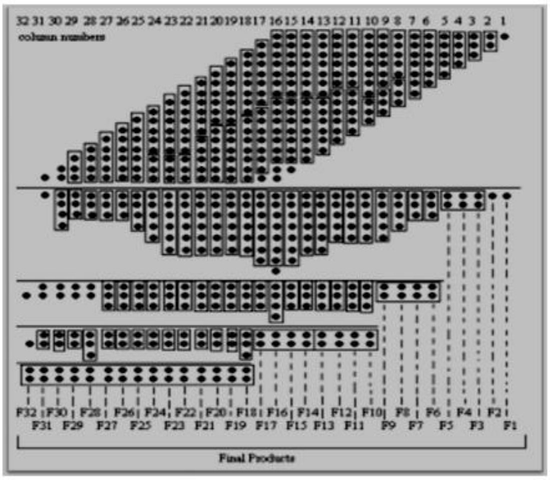

32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
column numbers
F32 F30 F28 F26 F24 F22 F20 F18 F16 F14 F12 F10 F8 F6 F4 F2
F31 F29 F27 F25 F23 F21 F19 F17 F15 F13 F11 F9 F7 F5 F3 F1
Final Products

Fig.3: 16*16 Wallace Tree Multiplier architecture **[6]**

Consider line number sixteen where the generated partial products are added by using single 7:3 compressor, 6:3 compressor and single full adder circuit. Including of all these three structures will produce eight outputs. As a substitute of this and to reduce the complexity of the design the proposed method uses two 7:3 compressors produces six outputs and the remaining two bits will propagated to the next stage. So at final eight bits are remained for the second stage of addition without using another extra adder. It shows that use of limited number of adders and compressors at the time of partial product addition with stage. It is noticed that each compressors assume 5-3 and 7-3 compressors has three outputs of bit position jth, (j+1)th and (j+2)th. At this instant assume, compressor is used at the column number six then its jth output will go to the line number six and another (j+1)th output will go to the line number seven and remaining output will go to the line number eight for the next stage. Here jth represents sum and (j+1)th represents carry, (j+2)th represents one more carry that is cout [6]. In this method partial product are added in two stages but existing approach involves three stages. In conventional method eight bits are generated after completion of first stage. But in this proposed method six bits are generated. This proves that critical path delay is reduced by using higher order compressors in proposed method compares to the conventional method. The reduction [6] of bits by the use of compressors is represented in dot structure. Every dot indicates a single binary bit and that dots are covered by distinctive rectangles including various number of dots .If the rectangles contain two or three bits represents half adder and full adder, if it contains five dots represents 5-3 compressor, similarly the others [6].

IV. ANALYSIS OF IMPLEMENTATION DESIGN AND CONCEPT

The Wallace tree [7] multiplier can be implemented by using half adder, full adder as well as compressors.

1) Half adder

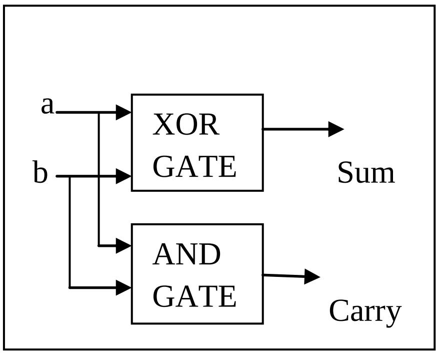


Fig.4: Logic diagram of Half adder

Sum= a (Ex-or) b; Carry= a.b

Half adder utilized in the designing of Wallace tree multiplier, when we are having two input bits which generates output as sum and carry. If both the input bits are 0 then outputs, sum=0and carry=0.If both the input bits are 0 and 1then outputs, sum=1 and carry=0. If both the input bits are 1 and 0 then outputs, sum=1 and carry=0.If both input bits are 1, sum=1 and carry=1.

2) 3:2 compressor

In Wallace tree multiplier full adders are replaced by 3:2 compressors owing to their multiplexer design along with use of minimum amount of XOR gate delays. Hence, highly suitable for signal processing applications to perform the complex operations like ternary add capability. The below figure 5 shows that two 3-LUT design can be easily merged with the contiguous logic.

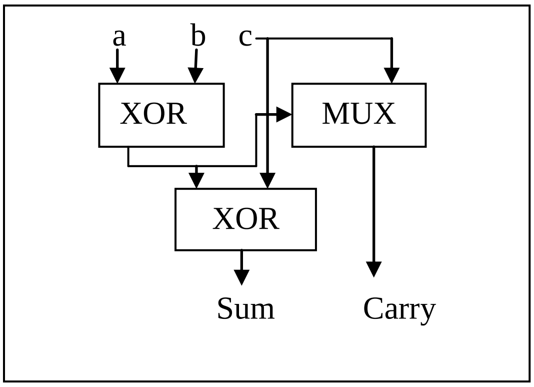


Fig.5: Logic diagram of 3:2 Compressor

Sum= (a Ex-or b Ex-or c)
Carry= (a Ex-or b).c + (a Ex-nor b).a

In wallace tree multiplier, 3:2 Compressor utilizes 3 input bits A, B and C to generate two outputs of sum and carry. When all three input bits are zero then outputs sum and carry will be zero. It shows that 1 is not present at any of the input. If anyone input bit is 1 then sum=1 and carry=0, It indicates that single 1 appears at the input. If two input bits are 1, then outputs sum =0 and carry=1, implies that two ones are present at the input. When all three input bits are 1 then outputs sum=1 and carry=1. It shows three ones are present at the input.

3) 5:3 compressor

The 5:3 compressor consist of five inputs such as A, B, C, D and Cin to produce three outputs called Sum, Carry and Cout. The output sum and four inputs of 5:3 compressor holds same weight. But one more input Cin is obtained from the output generated in previous least significant bit of the compressor. The remaining outputs carry and Cout will holds another significant weight of arriving of sum bit. In 5:3 compressor consider, all five inputs are 0 then outputs of Sum, carry and Cout will be 0. If anyone input is one then Sum=1, Carry=0 and Cout = 0. If two inputs are one then Sum=0, Carry=1, and Cout=0. When all five inputs are 1 then outputs Sum, Carry and Cout will be 1.

Sum= (a Ex-or b Ex-or c Ex-or d Ex-or cin)
Carry= (a Ex-or b Ex-or c Ex-or d).cin + [not(a Ex-or b Ex-or c Ex-or d)].d
Cout= (a Ex-or b).c +[not(a Ex-or b)].a

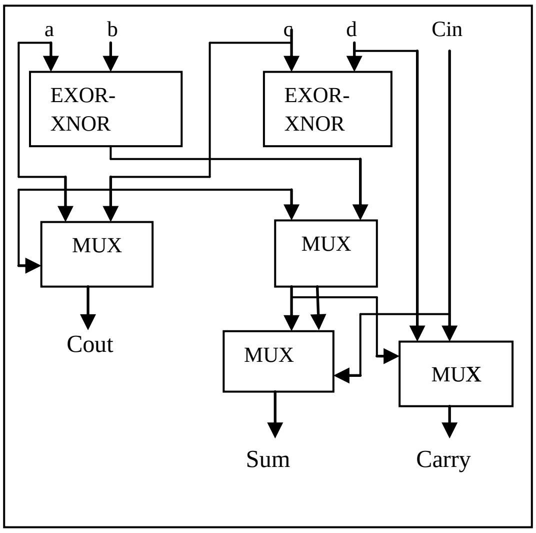


Fig.6: Logic diagram of 5:3 Compressor

4) 7:3 Compressor

The 7:3 compressor consisting of four 3:2 compressors linked from one to another in such a way that it accepts seven inputs and produce three outputs called Sum, Cout1 and Cout2. The output of Sum and seven inputs holds significant amount of same weight. While remaining output bits Cout1 and Cout2 holds successive two major weights after arrival of Sum bit.

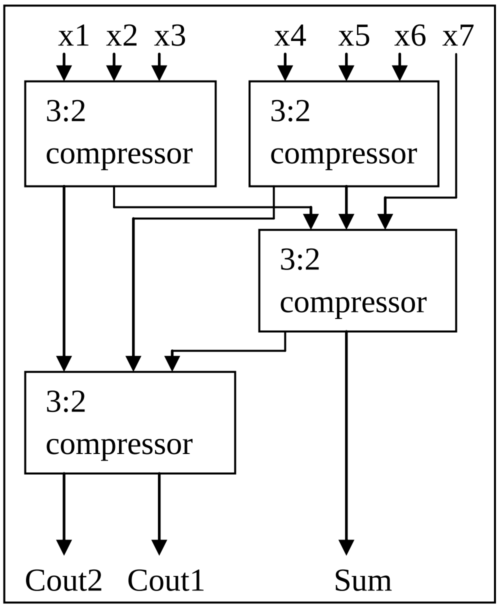


Fig.7: Logic diagram of 7:3 Compressor

V. RESULTS & DISCUSSION

The Wallace tree multiplier is designed for 4-bit, 8-bit, 16-bit, and 32-bit. The obtained results are simulated and synthesized using Xilinx ISE 7.1, Modelsim 6.3f and Cadence virtuoso tool to get maximum combinational path delay, Logic delay and route delay.

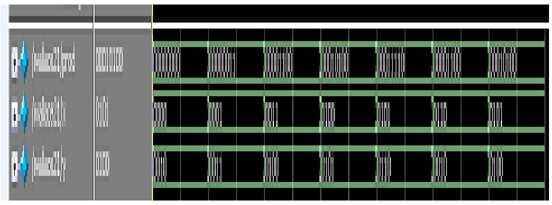


Fig.8: Simulation of 4x4 wallace tree multiplier

If inputs x and y are 4 bit. The output product will be 8 bit.
x=0000, y=0010 then product=00000000.
x=0001, y=0011 then product=00000011.

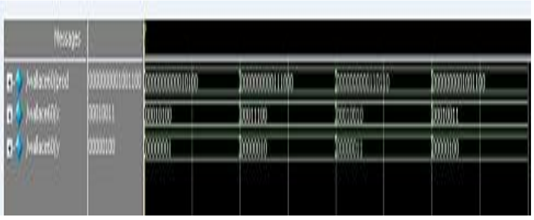


Fig.9: Simulation of 8x8 wallace tree multiplier

If inputs x and y are 8 bit. The output product will be 16 bit.
x=00010100, y=00000001 then
product=0000000000010100

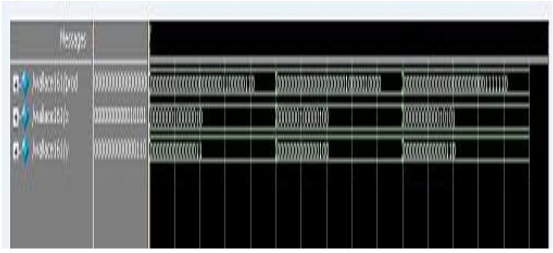


Fig.10: Simulation of 16x16 wallace tree multiplier

If inputs x and y are 16 bit. The output product will be 32 bit.
x=0000000000000010, y=000000000000011 then product= 00000000000000000000011000000110

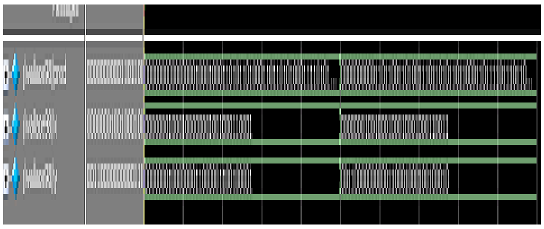


Fig.11: Simulation of 32x32 wallace tree multiplier

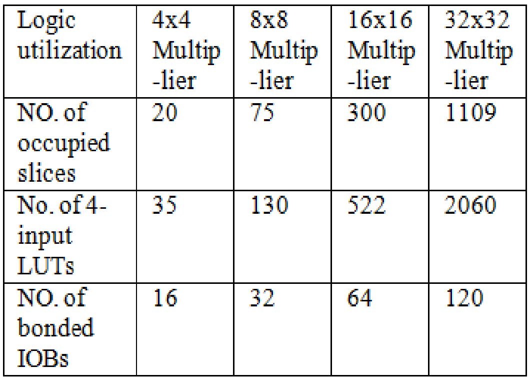
If inputs x and y are 32 bit. The output product will be 64 bit.
x=00010001001000100011001000001001
y=00100001001100010001001000110010
product=00000100011010010101000001001100001111010010100000101….

The designed Wallace tree multiplier can be analyzed by the terms of delay and amount of device utilization summary for 4-bit, 8-bit, 16-bit and 32-bit. The entire process is shown in the below table 1 and table 2.

Table 1. Analysis of delay for multipliers

Delay(in ns)	4x4 Multip -lier	8x8 Multip -lier	16x16 Multip -lier	32x32 Multip -lier
Maximum combinational path delay	20.326	32.129	64.376	126.619
Logic delay	10.414	14.725	26.221	48.734
Route delay	9.912	17.404	38.155	77.886

Table2. Total device utilization review of multipliers



Logic utilization	4x4 Multip -lier	8x8 Multip -lier	16x16 Multip -lier	32x32 Multip -lier
NO. of occupied slices	20	75	300	1109
No. of 4-input LUTs	35	130	522	2060
NO. of bonded IOBs	16	32	64	120

VI. CONCLUSION

The analysis design of Wallace tree multiplier is implemented in verilog. The simulation and synthesis results for 4-bit, 8-bit, 16-bit, 32-bit multipliers are obtained. The code is simulated using Xilinx ISE 7.1, Modelsim 6.3f and Cadence virtuoso tool. The results are analyzed in terms of speed, maximum combinational path delay, logic delay, route delay for different multipliers. For 16*16 Wallace tree architecture the maximum combinational path delay is 64.376 ns, logic delay is 26.221 ns, and route delay is 38.155 ns. This can be improved further.

Future Scope of Work

The designed Wallace tree multiplier can be further improved by using modified booth algorithm at the partial product generation stage. For faster multiplications, use of Kogge Stone Adder(KSA) to increase speed and Brent Kung Adder(BKA) for area reduce.

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