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Integration of Split Length Technique and Current Replication Branch in Two-Stage Class AB Operational Amplifier

Nimna Joseph[1]*, Nina Joseph[2], And Jobin Varghese[2]

[1]*Government Engineering College, Idukki, Kerala, India*

[2]*Microelectronics Research Unit,Faculty of Information Technology and Electrical Engineering University of Oulu,Oulu, FinlandFI-90014*

Corresponding Author:Nimna Joseph

ABSTRACT:A new two-stage class AB operational amplifier (op-amp) designed in which the differential-pair device N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOSFET) is replaced with split-length device and input stage is transformed into class AB using two-tail transistors. Current replication branch also incorporated in the design to increase output current. Hence, in this design, a class AB operation is achieved in both output and input. The entire design is implemented and simulated in Cadence design environment in 180 nm with 1.8 V supply. The newly designed op-amp exhibits high and symmetrical slew rate with the small amount of power consumption. Moreover, this design also improves gain and bandwidth and found to exhibit better performance as compared to other analysed existing topologies. The newly designed class AB op-amp works at 1.8 V supply with a positive slew rate of 57 V/µs and negative slew rate of 56 V/µs, again of 90.33 dB, thephase margin of 56.87, the bandwidth of 36 MHz, the power of 915 µW and settling time of 50 ns. Hence, this design exhibit excellent performance, which can satisfy the growing demands for energyefficient high-speed circuits in the modern electronic, and communication industry.

Index Terms—CMOSFET circuits, Operational amplifiers; slew rate; gain; phase margin; split length transistors

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I. INTRODUCTION

Operational amplifiers are considered as the backbone for many analog circuits. A fundamental building block utilizes high gain, high input resistance, low output impedance, high bandwidth and fast settling speed. The rapid growth of portable devices leads to the need for high speed and low power consumption. The design of high accuracy analog circuits is becoming a difficult task withscaling down of supply voltages and transistor channel length. MOS is the most successfulamong all because it can be scaled down to smaller dimensions for higher performance[1]. For getting higher performance, the size can be reducedtomicrometer or nanometer. Scaling down the transistor size helps to integrate a number oftransistors on the same size and hence result in a faster amplifier [2]. It leads to the continuous growth of the processing capacity per chip and operating frequency. Hence, most of the circuits require high-performance active cell. Designers are continuously working towards trade-offsolution between gain, input/output swings, speed, power dissipation and noise [3]. In most of the electronics circuits, the operational amplifiers (Op-Amp) is the most common building blocks used in modern instrumentation, communication and sensor systems [4]. The reduction in the transistor channel length and power supply pose continues challenges to the design on Op-amps. Speed and accuracy of these circuits depend on gain and slew rate of the Op-amp. Larger the value of gain and slew rate, higher the speed [5]. In applications such as sensor system, when the output changes rapidly, how fast the system responds to different levels that areinputandoutput level is necessary. Therefore, high slew rate based op-amp architecture is essential [6].

Several methods employed to improve slew rate in single stage Op-amps, but it has a disadvantage of low open-loop gain [7-9]. Which leads to the design of class A two stage Op-amps, which also failed to produce a vast improvement in slew rate [10]. Conventional class-A two-stage Miller-compensated op-amp exhibits highly asymmetrical slew rate and can be solved only by increasing the bias current (IB)which increase the static power dissipation [11].Hence class AB configurations of two stage Op-amps are developed to improve the slew rate. Many reported class AB two-stage Op-amps configurations developed to avoid the current limitations require additional circuitry or increased supply requirements and result in small slew rate enhancement [12], [13], [14], [15], [16]. In addition to this, it also decreases their current efficiency. A free class AB op-amp achieves high symmetrical slew rate, but it operates only at frequencies $f > 1/(2\pi R_b C_b)$[17], [18], [19].Another configura-

tion of class AB Op-amp with current replication branch shows slight improvement in slew rate and faces a challenge of low open loop gain[19]. Class AB two-stage op-amp configuration using adaptive loads achieved symmetrical slew rate but requires high power dissipation [19]. Reports about employing split length technology in Class AB Op-amp suggests that it can increase phase margin and unity gain bandwidth however it fails to attain symmetrical slew rate [20].

Hence, the design of two-stage Op-amp is a multidimensional optimization problem as an optimization of one or more parameters may easily result in the degradation of others [21]. The design motivates developing unique architecture, which improves the slew rates without affecting other parameters. In this paper, we designed a new power efficient high gain two stage op-amp with high symmetrical slew rate which is having better performance compared to existing topologies by integrating split length technology and current replication branch into the class AB configuration.

II. PROPOSED CLASS AB TWO STAGE OP-AMP

A new CMOS (Complementary Metal Oxide Semiconductor) class AB two-stage op-amp is designed by modifying the current free class AB two-stage op-amps for low-power, high gain, and high symmetrical slew rate operation. In this design, current replication branch [19] and split length technology [20] are incorporated into the class AB configuration, and the circuit diagram is shown in fig1.

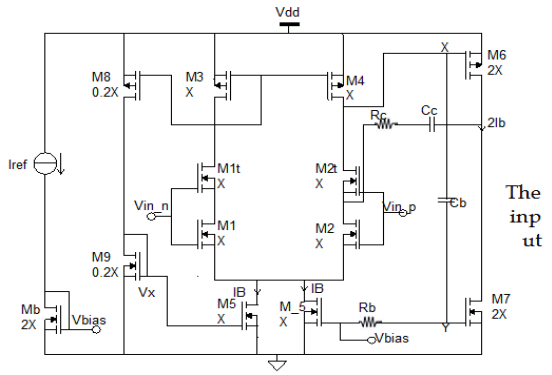

Fig 1. New design of class AB two-stage op-amp.

The input stage is transformed into a class AB circuit using two tail transistors M5 and a M_5 instead of the single tail transistor in class A configuration.The enhanced tail current of the differential pair for both positive and negative input differential voltages provides class AB operation to the stage of entry. The voltage at the gate of M1 is derived using a unity gain inverting amplifier formed by the current replication branch formed by M8 and M9 transistors scaled by a factor 0.2[19]. To create a low-impedance node, the length of differential pair transistor (NMOS) or load transistor (PMOS) is silted, and the compensation capacitor is connected to this low impedance node [21] as shown in Fig2.

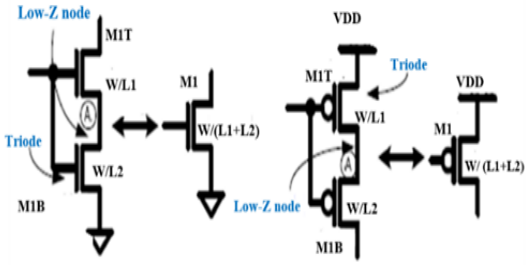

Fig 2.Schematic diagram of the split-length NMOS.

In this topology, thesplit-length device replaces the differential-pair device NMOS. The transistors M1t and M2t in the saturation region and transistors M1 and M2 in the triode region provides low impedance to node A. The capacitor C_b cannot charge or discharge easily as the resistor R_b is in cut-off. Hence, the voltage variation transfer occurs from node X to node Y. Thus, this setup renders to class AB output stage of the op-amp. The multiplying effect of the tail current boosting with the AB operation of the output stage provides enhanced AB operation.

III. SIMULATION RESULTS

CADENCE design environment in 180 nm CMOS process at 1.8 V supply carry out the design simulations. The AC and transient response of the designed op-amp models are simulated. The unitary transistor dimensions are (W/L) N= 50/1and (W/L)P = 140/1. IB = 100 µA, CL = 30 pF, VDD = 1.8 V, Rc= 2 kΩ,Cc= 10 pF.The Miller compensation net is the same in all the circuit.

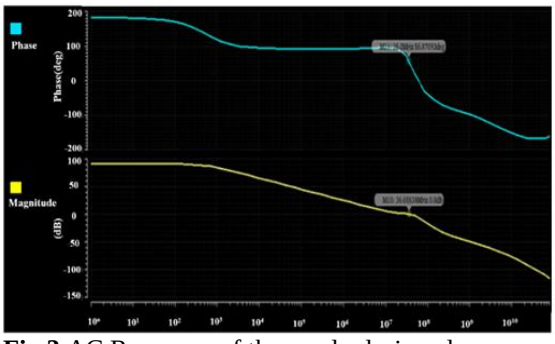

Fig 3.AC Response of the newly designed op-amp.

3.1AC Analysis

In AC analysis, an AC signal is applied to both the input terminals of the op-amp. By AC analysis, several performance parameters like gain, unity gain bandwidth, and phase margin can be estimated. The AC response of the designed op-amp is shown in Fig3. The Op-amp exhibited a gain of 90.33 dB, the phase margin of 56.87^0 and bandwidth of 36MHz over the measured frequency response.

3.2 Transient Analysis

The slew rate simulation is carried out performing a transient analysis. A step input is applied to the non-inverting terminal of the input stage with an inverting end connected to the output to form unity feedback configuration. Positive and negative slew rate value for the op-amp is calculated from this step response. Slew rate (SR) is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per second. Figure 4 shows the transient response of designed Op-amp. The input is a pulse between 0.8 and 1.6 V, the pulse width is 2µs, and load capacitance is 30 pF. Table 1 summarizes the performance of the designed class AB two stage op-amp and compares with other existing op-amp topologies. The newly designed op amp exhibits good performance with a high gain of 90.33 dB, the phase margin of 56.87, the bandwidth of 36 MHz, the power of 915 µW and settling time of 50 ns in addition to high and symmetrical slew rate and indicates the significance of this design.

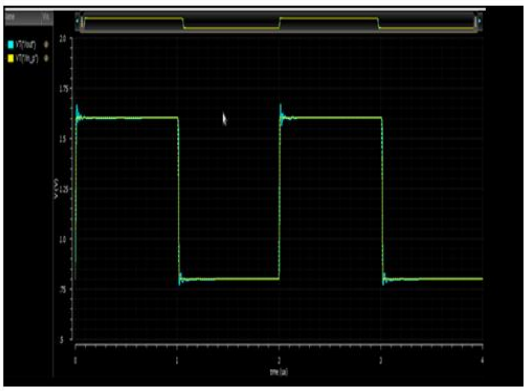

Fig 4 Transient response of newly designed op-amp.

To better understand, the importance and uniqueness ofthe present design, some of the existing topologiesare compared with the present design and simulated results. The existing topologies used in the pressseeennnt studies are conventional two stage Op-amp(conventional), free class AB (class AB), class AB op-amp with current replication branch(with CR), class AB two-stage op-amp with current replicating branch using adaptive load I at the input stage (Load I) and class AB two-stage op-amp with current replicating branch using adaptive load II at the input stage (Load II). All these existing topologies are redesigned using CADENCE design environment in 0.18 µm CMOS process for the comparison of present new design. Simulations of both existing and proposed designs at 1.8 V supply helps better comparison of the results. It is clearly evident from the Table 1, that the proposed circuit has high and symmetrical slew rate (SR) as well as good performance in terms of gain, phase margin, bandwidth, power dissipation and settling time compared to existing topologies. The combined effect of split technology and current replication branch in class AB-AB op-amp result in the high gain , unity gain bandwidth with high symmetrical slew rate with less amount of power consumption.All the above observations designate that the overall performance of the newly designed op-amp is better than existing designs. These good results specify that the new design can meet the potential demand for high speed and low power consumption circuits in the present growing electronics and communication world.

Specifications	Newly designed op-amp [Present work]	Conventional [10]	Class AB [21]	With CR [19]	Load I [19]	Load II [19]
Technology	180 nm	180 nm	180 nm	180 nm	180 nm	180 nm
Supply (V)	1.8	1.8	1.8	1.8	1.8	1.8
Gain(dB)	90.33	83	84.11	64.95	87.18	84.25
Phase Margin (o)	56.87	65.35	52.96	63.05	47.69	48.80
Bandwidth (MHz)	36	22.78	30.96	24.82	27.20	33.34
SR+ (V/µs)	57	19	20	20	24	23
SR-(V/µs)	56	4	8	10	22	19
Power(µW)	915	783	856	833	971	994
Settling time(ns)	50	185	163	181	160	150

Table 1 Comparison of the performance of newly designed op-amp with other existing topologies

IV. CONCLUSION

The present design and simulation of a new op-amp with class AB op-amp structure having low power capability and high and symmetrical slew rate. In this design, split-length device replaces the differential-pair device NMOSand input stage transforms into class AB using two tail transistors. CADENCE design environment in 180 nm CMOS process at 1.8 V supply implements the circuit designs. The newly designed op-amp also improve the gain and phase margin in comparison with the existing topologies. The newly designed class AB op-amp works at 1.8V supply with a positive slew rate of 57V/µs and negative slew rate of 56 V/µs and gain of 90.33 dB. It has a phase margin of 56.87, the bandwidth of 36 MHz,the power of 915 µW and settling time of 50 ns that is an added advantage to its numerous applications in the power efficient high-speed circuits in the modern electronics industry.

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First A. Nimna Josephreceived Bachelor of Technology from Government Engineering College, Calicut University, 2013. AndM.Tech from Government Engineering College, Idukki in 2016. Qualified national eligibility test Gate in 20013, Area of research interest is Microelectronics and Wireless Communications.

Second B. Dr. Nina Joseph received Bachelor of Science in Physics (2003-2006), Deva Matha College, Mahatma Gandhi University, Kerala India, Master of Science in Physics (2006-2008) School of Pure and Applied Physics, Mahatma Gandhi University, Kerala, India. Doctor of Philosophy (Major Subject: Physics/Materials Science) (2011-2015), Kerala University, Work done at CSIR-NIIST, Kerala, India. She is currently pursuing Post-Doctoralresearchat University of Oulu, Finland from 2015 onwards. She has published 11 SCI journal publications and 1 book chapter.

Third C. Dr. Jobin Varghese received Bachelor of Science in Physics (2003-2006) from Kerala University; Master of Science in Applied Electronics (2006-2008)from Bharathiar University, Master of Technology in Nanotechnology from VIT University and Doc-

toral degree from Cochin University of Science and Technology in 2015. Doctoral degree work done at CSIR-NIIST during 2010-2014. Presently doing Post-Doctoral research in University of Oulu, Finland. During the past seven years, Dr. Jobin working in the area of materials and its processing (HTCC, LTCC, ULTCC, Tape castingetc.) for advanced telecommunication applications. He has published 22 SCI journal publications, 1 Book Monograph, 3 Book Chapters, 2 Patents and 20International Conference presentations.

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