RESEARCH ARTICLE OPEN ACCESS

Implementation and Comparative analysis of Carry Select Adder using Kogge - Stone Adder in Adiabatic logic

[1]pallavi Sesham, [2]venkatalakshmi Thota, [3]kamaraju M
[1]M.Tech student, Gudlavalleru Engineering College, Gudlavalleru
[2]Associate Professor, Gudlavalleru Engineering College, Gudlavalleru
[3]Professor,Gudlavalleru Engineering College, Gudlavalleru
Corresponding auther: pallavi Sesham

ABSTRACT: Most important design consideration in integrated circuit after power is speed. Adders are one of the basic fundamental components in any digital systems. Due to rapid growth in technology there is need for fast processing. Addition is a basic operation in any digital,analog or control system, fast and accurate operation of digital system depends on the performance of adder. The major problem for binary addition is the propagation delay in the carry chain. As the width of the input operands increases the length of the carry chain will be increased. To reduce the carry propagation problem most of the modern adder architectures are represented as a parallel prefix adder structure. Kogge stone adder is one among the parallel prefix adders. This has the regular layout which makes them attractive adder in electronic technologies. This paper proposes the design of Carry Select Adder using Kogge stone adder inadiabatic logic. Specifically Positive Feedback Adiabatic Logic (PFAL) is used;this design will have proficiency of energy saving by reusing the energy which helps in reduction of power dissipation. Hence a fast adder with low power dissipation is designed.

Keyterms: Adiabatic logic, Positive Feedback Adiabatic Logic (PFAL), Kogge Stone Adder (KSA).

Date of Submission: 07-06-2018 Date of acceptance:22-06-2018

I. INTRODUCTION

Parallel Prefix adders (PPA) are established as the most efficient adders for binary addition in digital systems. These regular structure and fast performance attracts the users to implement them in VLSI design. The delay obtained in the parallel prefix adder (PPA) is directly proportional to the number of levels in the carry propagate stage. PPA executes an operation in parallel. It is done by segmentation of the operation in smaller pieces which are computed in parallel. The outcomes of the operation depends on the initial inputs, PPA is an advanced CLA. It is introduced to overcome the latency introduced by repelling effect of carry bits in RCA. It calculates one or more carry bits before the sum and thus reduces the wait time to calculate the result of large operands.

Kogge Stone Adder (KSA) is a PPA form of CLA. It generates the carry signals in lesstime and is widely considered as the fastest adder architecture design possible. It is the most common architecture for high performance adders in industry. In KSA carries are generated fast by computing them in parallel at the cost of increased area. The KSA has regular layout which makes them favored adder in electronic technologies.It will have minimal fan-out or minimum logic depth. The maximum fan-out is '2' for all widths of Kogge Stone Adder Prefix tree structures .It is widely used as it reduces the critical paths to great extent compared to RCA.

The complete functionality of KSA can be easily comprehended by analyzing it in terms of three distinct parts.

1.Pre-processing

This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B. These signals are given by the logic equations below.

$$P_i = A_i \oplus B_i \qquad (1.1)$$
$$G_i = A_i \cdot B_i \qquad (1.2)$$

2. Prefix stage

This block differentiate KSA from other adders and is the main focus behind its high performance. This step involves in the computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the following logic equations.

$$C_P = P_i \cdot P_{iprev} \qquad (1.3)$$
$$C_G = G_i + (P_i \cdot G_i) \qquad (1.4)$$

3.Post processing

This is the final step and is common to all adders of CLA. It involves computation of sum bits. Sum bits are computed by the logic given below.

$S_i = P_i \oplus G_i$ (or) (1.5)
$S_i = P_i \oplus C_{i-1}$

II. PARALLEL PREFIX ADDER

The PPA is like an advanced form of Carry Look Aheadadder. Theproduction of the carries in the prefix adders can be designed in many ways based on the different requirements. Generally we use tree structure form to increase the speed of arithmetic operations. The general prefix structure can be explained with the equations shown below.
let $A = a_{n-1} \ldots\ldots a_1 a_0$ and $B = b_{n-1} \ldots\ldots b_1 b_0$ be the n bit inputs, the binary addition is defined by equation below

$$S_i = a_i \oplus b_i \oplus c_{i-1} \quad (2.1)$$
$$C_i = a_i b_i + a_i c_{i-1} + b_i c_{i-1} \quad (2.2)$$

Prefix addition is carried in three steps.

1. Pre Processing

Preprocessing stage will generate and propagate signals. According to prefix computation the generate and propagate signals are defined by the equations given below as

$$G_i = a_i b_i \quad (2.3)$$
$$P_i = a_i \oplus b_i \quad (2.4)$$

2.Prefixcomputation

PPA construction mainly depends in the way how group carry and group generate signals are generated. Group generate and group propagate signals are defined by the equation

$$G_i = \begin{cases} g_i, & \text{if } i = k \\ G_{[i:k]} + p_{[i:k]} \cdot G_{[i-1:k]}, & \text{otherwise} \end{cases} \quad (2.5)$$
$$P_{[i:k]} = \begin{cases} p_i, & \text{if } i = k \\ p_{[i:k]} \cdot p_{[j-1:k]}, & \text{otherwise} \end{cases} \quad (2.6)$$

To simplify the representation of G and P an operator called as dot operator is introduced. It is represented as 'o'. It is introduced to create group generate and group propagate and is defined by the equation which is shown below.

$$(G,P)_{[i:k]} = (G,P)_{[i:k]} \circ (G,P)_{[j-1:k]} \quad (2.7)$$

3. Post processing

Post processing step involves formation of carry and sum bits for each individual operand bit. The equation for $C_i$and S_i are defined as

$$C_i = G_{[i:k]} \quad (2.8)$$
$$S_i = p_i \oplus c_{i-1} \quad (2.9)$$

III. ADIABATIC LOGIC

Two main parts that are present in an adiabatic system are its digital core design,which is made up of adiabatic gates and the power clock signal generator. Specifically in this paper, Positive Feedback Adiabatic Logic (PFAL) which has least power consumption among all adiabatic logic families is used to design the adder. The most important aspect of the adiabatic system is clock signal generator, high saving factor can be achieved by an optimal generation of four phase power clock.

1. PFAL:

PFAL is designed by the cross coupling of two inverters. They store the output state when the input signal decreases gradually. PFAL uses NMOS blocks for the implementation of logic, which are connected from the power clock Ø to the output nodes. It is a dual rail logic family constructed using a pair of cross coupled inverters (which is also called as latch and is known as adiabatic amplifier).Complementary inputs are given to the NMOS transistors to produce a low resistance between the power clock and the output. PFAL shows the best properties among the MOSFET only logic families.

2. Four phase clock generator:

Adiabatic circuits are operated withan oscillatory power supply which is called as the power clock. Based on the regarded adiabatic family more than one power clock signal is used to operate a system consisting of adiabatic logic gates. Each power clock cycle consists of four intervals, they are evaluate, hold, recovery and wait intervals.

In the evaluate interval the outputs are evaluated from the stable input signals. During the hold interval outputs are kept stable for providing the subsequent gate with a stable input signal. Energy is recovered in the recovery interval, and for symmetry purpose wait interval is inserted as symmetric signal are easier and more efficient to be generated.

IV. CHARGING PROCESS IN ADIABATIC LOGIC

To calculate the energy consumption by charging a capacitance and to explain it in the adiabatic circuits the equivalent circuit shown below is used.

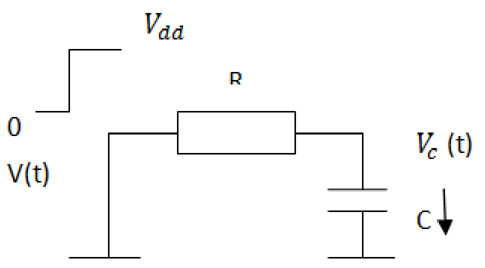

Fig: 1.Adiabatic charging equivalent circuit

R is the resistance in the charging path of the circuit,which consists of on resistance of transistor in the charging path and the sheet resistance of the signal line. For the observations of the energy dissipation R

is considered to be constant. The voltage is ramping from 0 to vdd within T time which is slow enough that Vc (t) ≈V (t).
Therefore the current into the circuit can be determined by

$$i(t)= c\frac{dv(t)}{dt} = c\frac{v_{dd}}{T} \qquad (4.1)$$

The energy for a charging event is calculated as given below

$$E = \int_0^T P(t)dt = \int_0^T v(t).i(t)dt$$

$$= \int_0^T Vr(t) + Vc(t).i(t)dt \ (4.2)$$

Replacing Vr(t) with i(t).R in above equation we get

$$E = \int_0^T R\,\frac{C^2Vdd^2}{T^2}\,dt=\frac{RC}{T}\,C\,Vdd^2(4.3)$$

Overall dissipation is given by

$$E_{al} = \frac{2RC}{T}\,Cvdd^2 \qquad (4.4)$$

From the above equations it shows that the operating speed impacts the energy dissipation. The slower the circuit is charged the less energy is dissipated. The opportunity which can be used for further reduction of power consumption is by scaling the supply voltage or by reducing the load capacitance. In contrast to static CMOS the size of the switch transistor also has an effect on the energy dissipation as R is found in the equation for the energy dissipation in adiabatic logic.

V. DESIGN OF KSA

The block diagram of the designed 8 bit Kogge Stone Adder can be shown below;

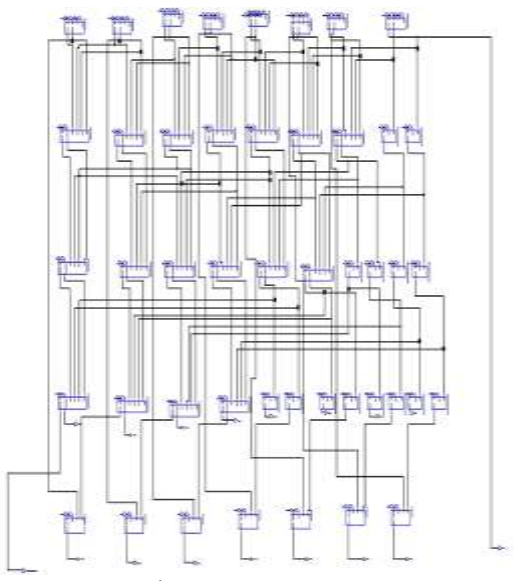

Fig: 2. Design of Kogge Stone Adder in adiabatic logic

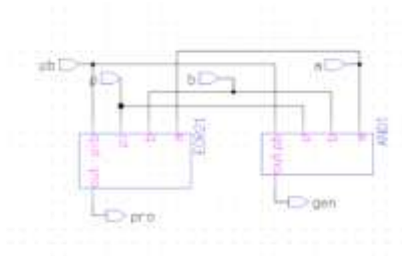

Fig: 3. Propagate and generate cell

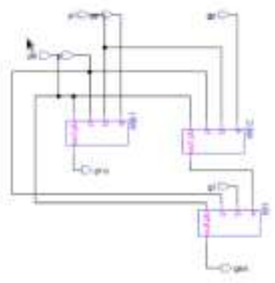

Fig: 4. Carry generate cell

From the above designed block we can observe the arrange ment of group propagate and group generate blcks. In the last stage the XOR gates are used to obtain the sums S_1 to S_8 and final carry is obtained as C_{out}.

VI. DESIGN OF CARRY SELECT ADDER USING KSA:

In this method replace any one of the RCA structure (i.e. cin =1 or cin =0) by parallel structure of D-latches. For n bit RCA structure it required n D-latches with enable pin as a clk. Latches are used to store one bit information. The RCA structure cin is replace by enable pin, where enable signal is clock signal. When enable pin en =1 then the RCA structure is calculate for cin=1 that result is stored in D-latch. When en =0 then it will calculate for cin =0 and the D-latch output and full adder output is given to the mux. By using selection line it will gives the proper output. Initially RCA structure will calculate for en=1 and then en =0.

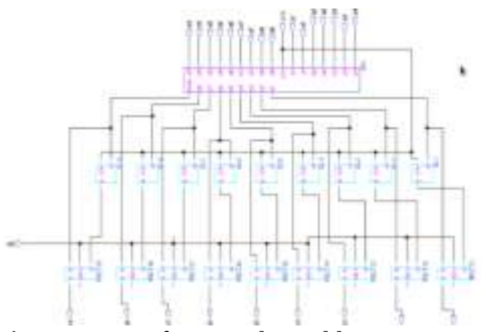

Fig.5. Design of carry select adder using KSA in Adiabatic logic

VII. SIMULATIONS AND EXPERIMENTAL RESULTS

The proposed Carry Select Adder using Kogge Stone Adder is designed in mentor graphics tool which is of 130nm technology. From the simulation results the great reduction in terms of power and delay has been observed when compared with the CMOS design. This particular fast adder such as Kogge Stone Adder is favored only because of its less delay characteristics which indicate its faster performance. Hence a fast processing processor or any a kind of fast system can be designed by replacing normal adders with kogge stone adder.

The sinusoidal signal is used as the power clock for the entire design which is of 1v amplitudeand the frequency used is50Mhz. the adiabatic logic will work effectively from 1KHz to 1MHzfrequency range and the power dissipation will depend on the supply voltage and equivalent resistance. The simulated wave forms are shown below

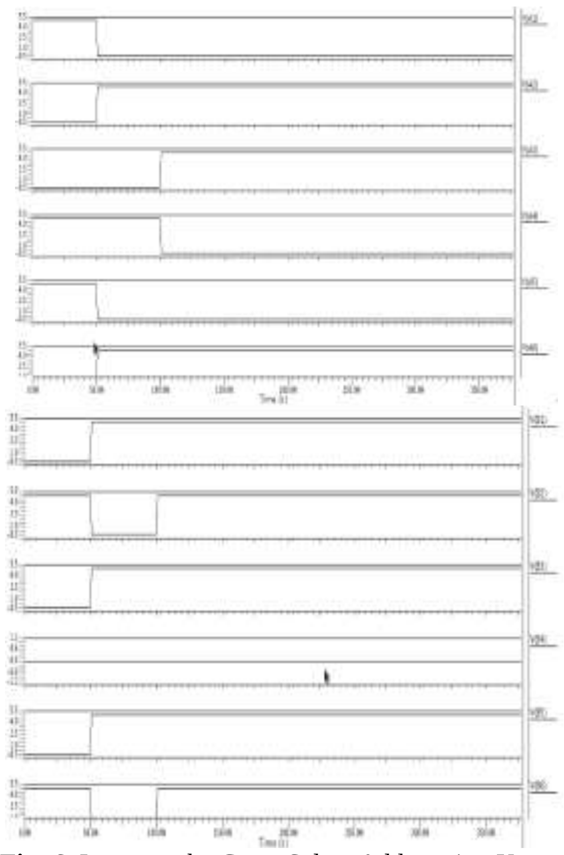
Fig: 6. Inputs to the Carry Select Adder using Kogge Stone Adder

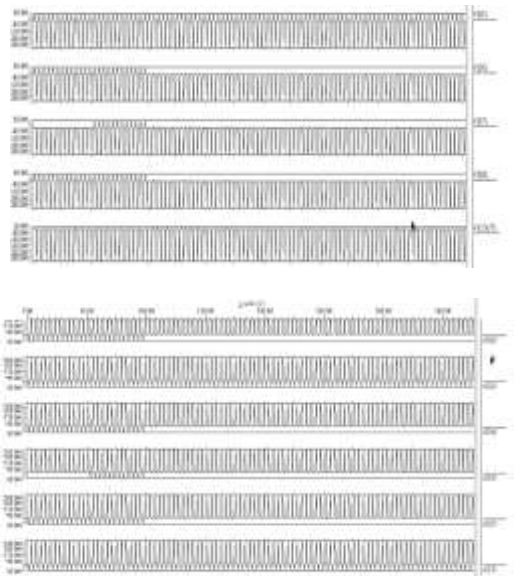
Fig: 7. Output waveforms of Carry Select Adder Kogge Stone Adder

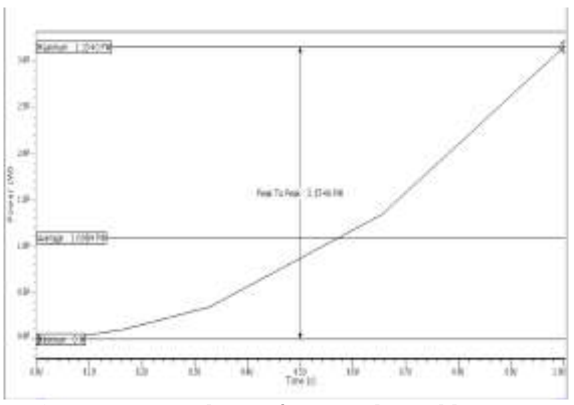
Fig.8. Power analysis of carry select adder using KSA

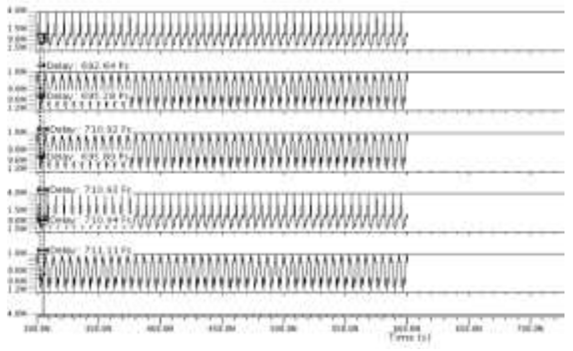
Fig.9. Delay analysis of carry select adder using KSA

Table: 1. Delay and power analysis of Carry Select Adder using Kogge Stone Adder

SUPPLY VOLTAGE	POWER DISSIPATION		AVERAGE DELAY	
	Adiabatic	CMOS	Adiabatic	CMOS
1V	1.098pW	161.5nW	277.9pS	69.4pS
0.7V	269.15fW	59.81nW	485.5pS	109pS

VIII. CONCLUSION

High speed and low power consumption are the most desirable factors in VLSI design; in the proposed design of Carry Select Adder using Kogge Stone Adder in adiabatic logic, adiabatic design logic is mainly chosen for ultra-low power VLSI design. Hence from the proposed design we can conclude that an efficient adder is designed with least power consumption.

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pallavi Sesham "Implementation and Comparative analysis of Carry Select Adder using Kogge - Stone Adder in Adiabatic logic "International Journal of Engineering Research and Applications (IJERA) , vol. 8, no.6, 2018, pp.22-26