Hitansu Sekhar Sahu Journal of Engineering Research and Application www.ijera.com
ISSN : 2248-9622, Vol. 8, Issue5 (Part -IV) May 2018, pp 73-77

RESEARCH ARTICLE OPEN ACCESS

Design And Implementation Of High Speed Vedic Multiplier

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ABSTRACT
Vedic mathematics is the ancient Indian system of mathematics. This paper proposed the design oh high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that has been modified to improve performance. Multipliers play a major role in processors and in many computational systems. The speed of these systems greatly depends on the speed of its multipliers. In order to enhance the speed of the systems the faster and efficient multipliers should be employed. Vedic Multiplier is one of the best solution which is capable of performing the quicker multiplications by eliminating the unwanted steps in the multiplication process. Vedic Multiplier deals with a total of sixteen sutras or algorithms for predominantly logical operations. In this paper it is used for designing a high speed, low power 4X4 multiplier. In the proposed design we have reduced the number of logic levels, thus reducing the logic delay. The proposed system is design using VHDL and it is implemented through Xilinx 8.1.

Keywords – Urdhva Tiryakbhyam Sutra, Vedic Mathematics, Vedic Multiplier

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Date of Submission: 07-05-2018 Date of acceptance: 22-05-2018

I. INTRODUCTION

Veda is a Sanskrit word which means 'Knowledge'. Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati Krsna Tirthaji (1884-1960). Vedic Mathematics [6] is a collection of Techniques/Sutras to solve mathematical arithmetics in easy and faster way. It consists of 16 Sutras (Formulae) and 13 sub-sutras (Sub Formulae) which can be used for problems involved in arithmetic, algebra, geometry, calculus, conics. The maximum famous amongst those sixteen are Nikhilam Sutram [3], Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakbhayam is the maximum efficient among those. Urdhva Tiryagbhyam is the most generalised sutra for implementation of Vedic Multiplier designs because with increase in number of bits both area and delay increase slowly [5]. The beauty of Vedic Multiplier lies in the fact that they can be used to solve cumbersome mathematical operations orally thereby improving speed. Vedic Multiplier has become highly popular as a faster method for computation and analysis [4].

Multiplication [8] is the most important arithmetic operation in many applications such as Central Processing unit (CPU), MAC (Multiply and Accumulate) unit [2], Image Processors and Digital Signal Processors [1] etc. As speed is always a major requirement in the multiplication operation, increase in speed can be achieved by reducing the no. of steps in the computation process. In DSP system to perform operations such as Convolution, Discrete Wavelet Transform, Fast Fourier Transform, and Filtering etc multipliers are essential. The speed of the system is majorly depends on the multiplier unit. This is the one of the apt place for employed Vedic mathematics to perform multiplication. Multipliers being the key components of Arithmetic and logic units, Digital signal processing blocks and Multiplier and accumulate units, determine the performance and throughput of the applications.

II. VEDIC MULTIPLICATIONS

Urdhva tiryagbhyam sutra [9] is a general multiplication formula applicable to all cases of multiplication.

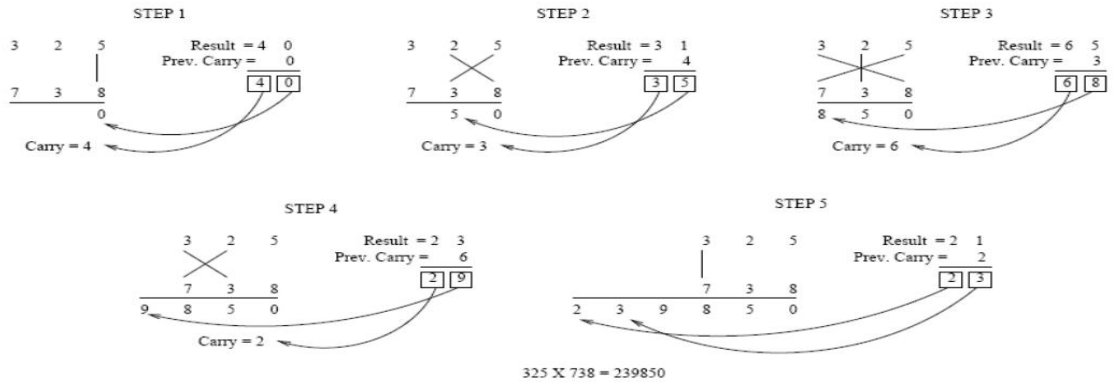


Fig 1 Multiplication of two decimal numbers by Urdhva Tiryagbhyam sutra [12]

It literally means "Vertically and crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 728). Line diagram for the multiplication is shown in Figure 1. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be zero [7].

Urdhva Tiryagbhyam Sutra is used for two decimal numbers multiplication [12]. This Sutra is used in binary multiplication as shown in Figure 2.

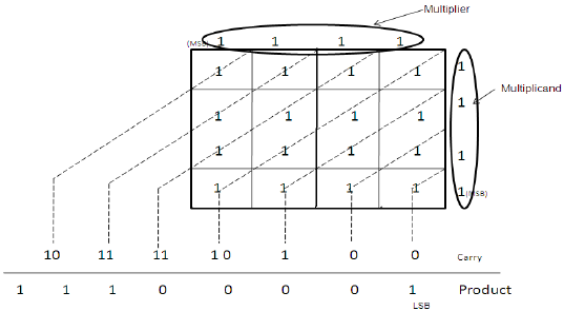


Fig 2 Multiplication of two 4-bit binary numbers by Urdhva Tiryagbhyam sutra

The 4-bit binary numbers [10] to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each bit of the multiplier has a small box common to a digit of the multiplicand. Each bit of the multiplier is then independently multiplied (logical AND) with every bit of the multiplicand and the product is written in the common box. All the bits lying on a crosswise dotted line are added to the previous carry. The least significant bit of the obtained number acts as the result bit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero. We can extend this method for higher order binary numbers.

III. EXISTING 4X4 VEDIC MULTIPLIER

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules. Let's analyse 4x4 multiplications, say a= a3 a2 a1 a0 and b= b3 b2 b1 b0. The output line for the multiplication result is – s7 s6 s5 s4 s3 s2 s1 s0. Let's divide a and b into two parts, say a3 a2 & a1 a0 for a and b3 b2 & b1 b0 for b. Using the fundamental of Vedic multiplication, taking two bits at a time and using 2-bit multiplier block C.

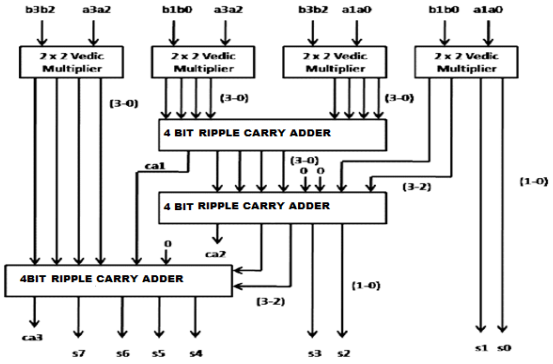


Fig 3 Diagram of 4X4 multiplier

RIPPLE CARRY ADDER (RCA)

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used.

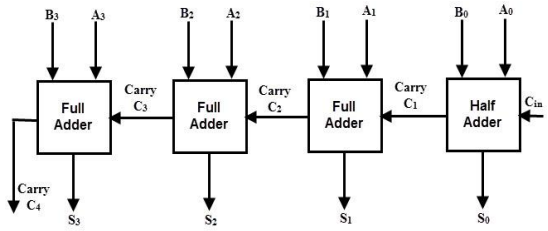


Fig 4 4-bit Ripple Carry Adder

IV. VEDIC MULTIPLIER USING PROPOSED 4X4 ADDER

4-bit adder performs the function of 4-bit addition that gives two bits of sum and one carry as output. Its block diagram contains one full adder (FA) and two half adders (HF) is given in Figure 5 [11].

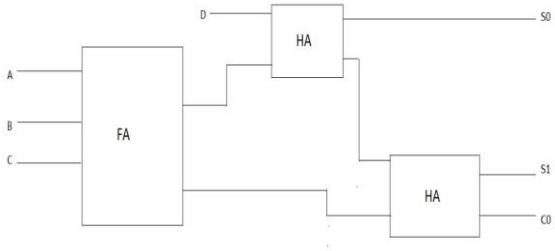


Fig 5 Proposed 4-bit adder

Here, A, B, C, D are four inputs. S0 and S1 are LSB and MSB of Sum outputs respectively and Sum is the sum of four inputs. C0 is the carry bit.

To reduce the delay, a 4X4 multiplier is implemented using half adder, full adder and the proposed 4-bit adder as shown in Figure 5.

FULL ADDER USING MUX PROPOSED METHOD

The Vedic multiplier can be made more efficient by further reducing the critical path delay. The same can be achieved by using proposed full adder. Each multiplexer has been realized by using two transistors, for the realization of the full adder circuit. The major source of power dissipation in any circuit is short circuit current, leakage current and logic transition. Since in this circuit there is no probability of direct path formation between source and ground.

In Vedic structure the partial products are divided into certain levels. In each level, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement is provided as inputs to the first multiplexer. The other two inputs are given to XOR gate, the output of which will act as a select line to both the multiplexers. The inputs of the second multiplexer are the bits other than the carry bit. This unique way of designing leads to the reduction of the switching activity, which in turn reduces the power. In addition to this, the critical path delay is also reduced compared to the existing designs discussed in literature, which leads to reduction in delay and thus increasing the speed. Operation of the proposed full adder can be explained as follows:

a) When B and C = 0 or 1 then sum = A;
b) When B = 0 or C = 1 vice versa then sum=A;
c) When B and C = 0 or 1 carry= B;
d) When B = 0 or C = 1 vice versa then carry=A.

FULL ADDER USING MUX

Full adder using MUX performs the function of addition of 4 bit that gives two bits of SUM and one CARRY as output. Its block diagram contains two 2X1 MUX and one XOR gate as shown in Figure 6.

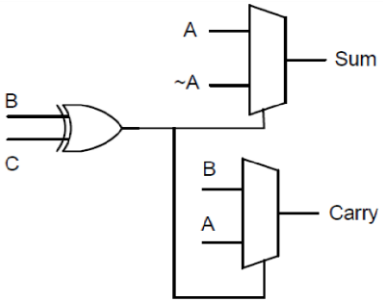


Fig 6 Proposed full adder

V. PROPOSED VEDIC MULTIPLIER

Here A, B are 4-bit inputs to each of the blocks as shown in the Figure 7. P0 to P7 are the outputs of the proposed Vedic using MUX full adder. The Block diagram is shown below.

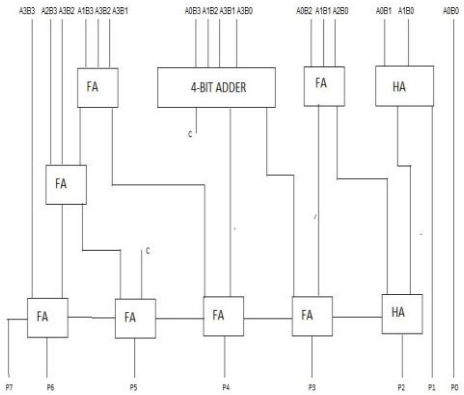


Fig 7 4X4 Vedic Multiplier using MUX full adder

VI. RESULT AND DISCUSSION

The proposed 4x4 multiplier is coded in VHDL, simulated using Xilinx 8.1 simulator, synthesized using Xilinx XST and verified for possible inputs given below. Inputs are generated using VHDL test bench. The simulation result for 4x4Vedic multiplier is shown in below.

SCHEMATIC DIAGRAM

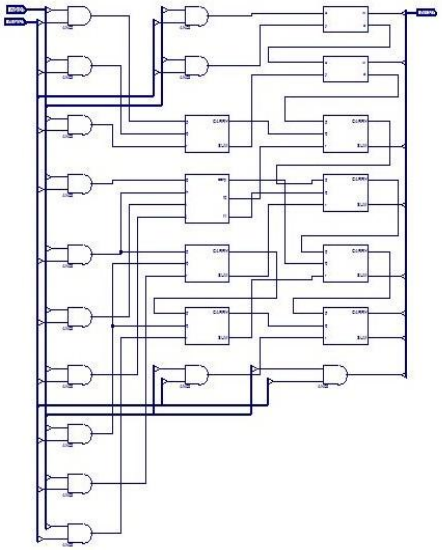


Fig 8 RTL diagram of Proposed 4x4 Vedic multiplier

SIMULATION WAVEFORM

4x4 Vedic multiplier using full adder and 4x4 Vedic multiplier using MUX full adder are compared with existing architecture in terms of total delay, logic delay, logic delay, route delay and number of logic

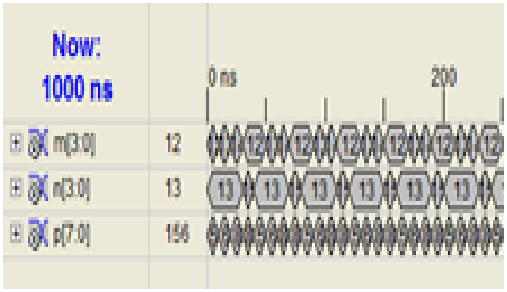
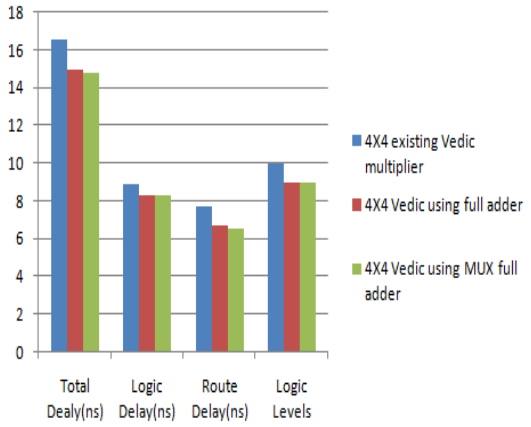


Fig 9 Simulation waveform of Proposed 4x4 Vedic multiplier

levels. The results obtained are tabulated in Table 1. From Table 1, it is evident that there is a reduction in both total delay and logic levels. The routing delay is found to be 6.493 ns, the logic delay is 8.300 ns; thus, giving a total delay of 14.793 ns. The number of logic levels is 9. Thus, it is clear that the proposed design is more efficient than the existing one. The proposed architecture can be used to develop a high-speed complex number multiplier with reduced delay.

Table 1 Comparison between 4x4 existing Vedic multiplier, 4x4 Vedic using full adder and 4x4 Vedic using MUX full adder

Multiplier Type	4x4 existing Vedic multiplier	4x4 Vedic using full adder	4x4 Vedic using MUX full adder
Total Delay(ns)	16.584	14.937	14.793
Logic Delay(ns)	8.912	8.300	8.300
Route Delay(ns)	7.672	6.637	6.493
Logic Levels	10	9	9
Total memory usage	190344 kilobytes	190280 kilobytes	184828 kilobytes



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Hitansu Sekhar Sahu "Design And Implementation Of High Speed Vedic Multiplier "International Journal of Engineering Research and Applications (IJERA) , vol. 8, no.5, 2018, pp 73-77