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Fault Tolerance Analysis of Modified Irregular Augmented Shuffle Exchange Network (MIASEN)

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ABSTRACT
Multistage Interconnection Networks (MINs) play a vivacious position to perform high performance within the discipline of VLSI, broadband communications, parallel and distributed systems designs. The problem of fault tolerance and cost effectiveness are the predominant challenges for calculating the overall performance of MINs. A MIN is better fault tolerant, if it may deal with the extra faults come across in different stages. The fault tolerance of proposed Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12] is examined in terms of bandwidth, processor utilization, throughput, probability of acceptance, and processing power. The performance and evaluation analysis indicates that the MIASEN is more fault tolerant than the existing Irregular Augmented Shuffle Exchange Network-2 (IASEN-2) and Modified Alpha Network (MALN).
Keywords - Fault tolerance, Multistage Interconnection Network

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I. INTRODUCTION

The performance of high-performance computing systems relies heavily on the efficiency of the multistage interconnection networks (MINs). Because of its high speed and low cost, MINs become more popular for multiprocessor systems as compared to single-processor systems. The problem of lack of fault tolerance is the major issue in MINs. The performance of MINs is depending on fault tolerance capability of that network. For example, single path MINs are less fault tolerant as compared to multipath MINs. A MIN is less reliable if it tolerate minimum faults. Fault tolerance can be increased by following methods:

(i) To increase the number of stages
(ii) To increase the number of links
(iii) To increase the number of switches
(iv) To replicate the entire network

In recent years, various research works have been done on fault tolerance techniques and to design new MIN to increase the fault-tolerance [1-6]. In this research paper, the fault tolerance analysis and routing algorithm of proposed Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12] have been discussed. The fault tolerance of proposed Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12] is compared with existing Irregular Augmented Shuffle Exchange Network-2 (IASEN-2) [9] and Modified Alfa Networks (MALN) [1].

Section 2 depicts basic structure of Irregular Augmented Shuffle Exchange Network-2 (IASEN-2) and Modified Alfa Networks (MALN) [1] and Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12]. The routing algorithm of MIASEN is also discussed in Section 3. Section 4 focuses on the Fault-tolerance analysis of MIASEN on different parameters. Section 5 concentrates on the results and comparison analysis of MINs. In Section 6, the conclusion has been presented.

II. STRUCTURE OF MULTISTAGE INTERCONNECTION NETWORKS

In this paper, the focus is on fault tolerance of irregular MINs. The basic structure of Irregular Augmented Shuffle Exchange Network-2 (IASEN-2) and Modified Alfa Networks (MALN) [1] and proposed Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12] are discussed below.

1.1 Modified Alpha Network

Modified Alfa Networks (MALN) [1] consists of N number of source and destination addresses with (2m-2) stages where $m=\log_2(N/2)$. Each source is linked with 2x1 MUX and each destination is linked with a 1x2 demultiplexer. All stages except the last stage consist of switching elements (SE) of size 3x3 and the last stage consists of switching elements of size 2x2. The switching elements in the stages n-3, n-2 and n-1 are connected to each other through auxiliary or alternate links where $n= \log_2 N$. The network is divided into two identical subnetworks G_0 and G_1 [1].

1.2 Irregular Augmented Shuffle Exchange Network-2

Irregular Augmented Shuffle Exchange Networks-2 (IASEN-2) [9] has N sources and N destinations with n=(log_2N) stages. Each source and destination is associated with the multiplexers (MUX) of size 2x1 and demultiplexers (DEMUX) of size 1x2 respectively. The first and last stages are linked with N/2 switching elements (SE) [9]. The first stage and last stage have SEs of size 2x3 and 3x2 respectively but SE of second stage and third stage has size 9x3 and 3x9 respectively. The second and third stage consist N/8 SEs. The SEs of each stage is associated with each other through alternative links. The first and last stages are linked with N/2 switching elements (SE)

1.3 Modified Irregular Augmented Shuffle Exchange Network

The Modified Irregular Augmented Shuffle Exchange Network (MIASEN) [12] consists of N number of source and N number of destination addresses. The MIASEN has N×N network size with [(log_2N)-1] number of stages. The first and last stages have N/2 switches (SEs). The size of each SE of first stage is 3×3 and the size of each SE of last stage is 2×2. The middle stage has (N/8) number of SEs and size of each SE is 5×5. MIASEN has N number of multiplexers (MUX) with size 2×1 each and N number of demultiplexers (DEMUX) with size 1×2 each. Each SE of the first stage and each SE of the last stage connected with two MUX and two DEMUX respectively. A 16×16 network size MIASEN with 3 numbers of stages is shown in Fig. 1.

MIASEN is fault tolerant network and reliable MIN, if any failure occurs in any switch in the network then there will be an alternate path to work properly.

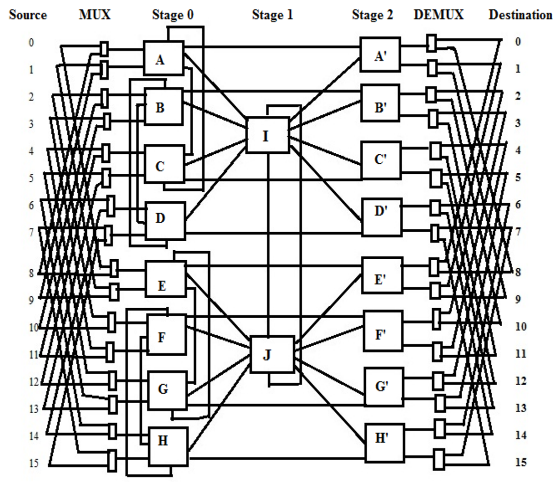

Fig. 1 Modified Irregular Augmented Shuffle Exchange Network (MIASEN)

III. ROUTING PROCEDURE OF MIASEN

Each source is connected to two switches (primary and secondary) via primary and secondary path in network. Primary path is the shortest path between source and destination while secondary path is the alternate path which consists of more switches and stages. For example, A is the primary SE and E is secondary SE for source 0. A request from given source to a given destination is routed through the MIASEN as:

- In routing of MIASEN, first step is to obtain the source address and its corresponding destination address. Each source send request to primary switch via primary path or link. If primary path or link is busy or faulty (i.e. either primary switch or MUX or both are faulty), then route the request to secondary switch via secondary path. If secondary path is also busy or faulty, then drop the request.
- For each switch in stage 0, request may arrive on any of the 3 input links. For each request if the required output link is busy or cannot be used because of a fault in the next stage, route the request via the alternate output links. If alternate links are also faulty or busy then drop the request otherwise send the request to the SE of next stage.
- For each switch in middle stage, request may arrive on any of five input links. Route it via corresponding output link if it is not available or faulty then send the request to the alternate output link. If the alternate link is faulty or busy then drop the request.
- For each switch in last stage, request may arrive on any of two input links. Route it via the corresponding output link. If the required output link is busy or faulty then drop the request.
- Each DEMUX can receive maximum of one request. Send the request to its destination through DEMUX. Each destination can receive two

Hence, MIASEN is a single switch fault tolerant MIN.

IV. FAULT TOLERANCE ANALYSIS OF MIASEN, IASEN-2, AND MALN

The fault tolerance analysis of MIASEN, IASEN-2 and MALN is measured in terms of performance evaluation parameters such as probability of acceptance, bandwidth, throughput, processor utilization, processing power.

3.1 Request Generation Probability (p)

"The expected numbers of destination receiving request in a given cycle is known as bandwidth of network [3] [12]". Let the network size is N× N. Then the bandwidth will be as follows:

$BW=N\times p_n$ (1)

Probability equation for MALN [1]:

$p_0=p$

Request generation probability for first stage

$p_1=1-(1-p_0/3)^3$ (2)

Request generation probability for second stage

$p_2=1-(1-p_1/6)^3$ (3)

Request generation probability for third stage

$p_3=1-(1-p_2/3)^3$ (4)

Request generation probability for fourth stage

$p_4=1-\{(1-p_3)\times(1-p_1/2)\}^2$ (5)

Probability equation for IASEN–2 [9]:

$p_0=p$

Request generation probability for first stage

$p_1=1-(1-p_0/2)^2$ (6)

Request generation probability for second stage

$p_2=1-(1-p_1/6)^{((N/2)+1)}$ (7)

Request generation probability for third stage

$p_3=1-(1-p_2/((N/2)+1))^3$ (8)

Request generation probability for fourth stage

$p_4=1-[(1-p_3)\times(1-p_1/2)]^2$ (9)

Probability equation for MIASEN:

$p_0=p$

Request generation probability for first stage

$p_1=1-(1-p_0/3)^3$ (10)

Request generation probability for second stage

$p_2=1-(1-p_1/5)^5$ (11)

Request generation probability for third stage

$p_3=1-[(1-p_2)*(1-p_1/2)]^2$ (12)

3.2 Data Transmission Time

“It is time that all generated data packets take from source to the given number of destinations [12].”

If network is non-faulty, then it is given as follows:

$t=(N_n-1)\ x\ T\ x\ N_{dp}\ x\ D_n$ (13)

If network has single switch fault, then it is given as follows:

$t_{SF}=t+(S\ x\ T)$ (14)

Where,

N_n=Number of nodes including source and destination

T= Routing Time between two nodes

D_n=Number of destinations

N_{dp}= Total number of generated data packets on a source node

S= total number of stages

t= If network is non-faulty, then data transmission time

t_{SF}= If network is single switch faulty, then data transmission time

3.3 Bandwidth

“The expected numbers of destination receiving request in a given cycle is known as bandwidth of network [3][12]”. Let the network size is N× N. Then the bandwidth will be as follows:

$BW=N\times p_n$ (15)

3.4 Probability of Acceptance (PA)

“Probability of Acceptance (PA) is the number of request accepted by the destination side that is sent by the source side in a transfer cycle [3][12]”. It is calculated as follows:

$PA=[BW/(D_n\times p)]$ (16)

3.5 Throughput (TP)

“It is the maximum number of traffic per unit time accepted by a network is called throughput [3][12]”.

$TP=(BW/N\times t)$ (17)

Where, t is the data transmission time.

3.6 Processor Utilization (PU)

“The percentage of time the processor is active doing computation without retrieving the global memory is known as processor utilization [3][12]”.

$PU=(BW/N\times p\times t)$ (18)

3.7 Processing Power (PP)

“The sum of processor utilization over the number of processors is known as processing power [3]”.

$PP=(N\times PU)$ (19)

V. COMPARISON AND ANALYSIS

The performance analysis and comparison is determined for IASEN-2, MALN and MIASEN on above parameters in faulty and non-faulty environment. Let the data packet is transferred from source 1 to destination 6. Let the routing time between two nodes is 0.01 ms, when network is non–faulty and 0.02 ms, when there is a single switch fault in network. Nodes can be anything either source or destination or SE. Let the value of request generation probability or offered load (p) is 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1. Therefore, comparison between IASEN-2, MALN and MIASEN is performed by bandwidth, probability of acceptance, throughput, processor utilization, and processing power in non-faulty and single switch fault environment.

5.1 Bandwidth (BW)

The performance analysis shows that the bandwidth of MIASEN is better than IASEN-2 and MALN.

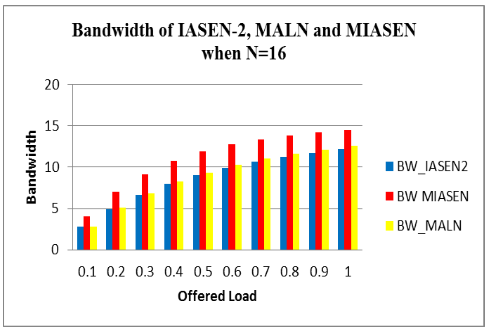

Fig. 2 Bandwidth Comparison under Non-Faulty and Faulty conditions

5.2 Probability of Acceptance (PA)

The Probability of Acceptance of MIASEN is greater than IASEN-2 and MALN.

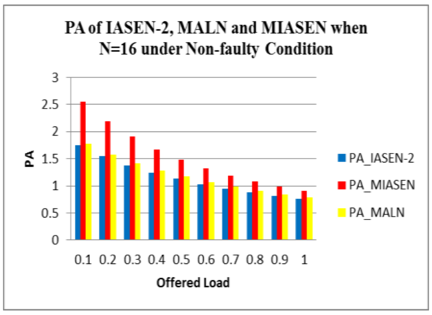

Fig. 3 Probability of Acceptance under Non-Faulty and Faulty conditions

5.3 Throughput (TP)

The performance comparison shows that throughput of MIASEN is better than IASEN-2 and MALN under non-faulty (without fault) and faulty (with single switch fault) conditions.

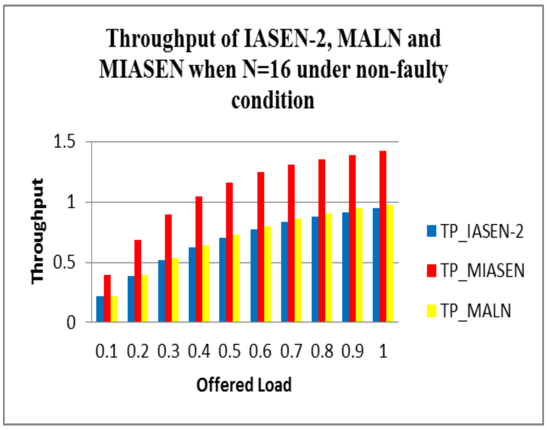

Fig. 4 Throughput under Non-Faulty condition

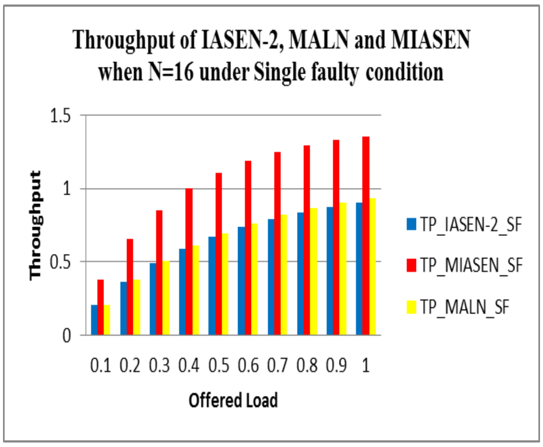

Fig. 5 Throughput under Single Fault condition

5.4 Processor Utilization (PU)

Processor utilization of MIASEN is better than IASEN-2 and MALN in both conditions.

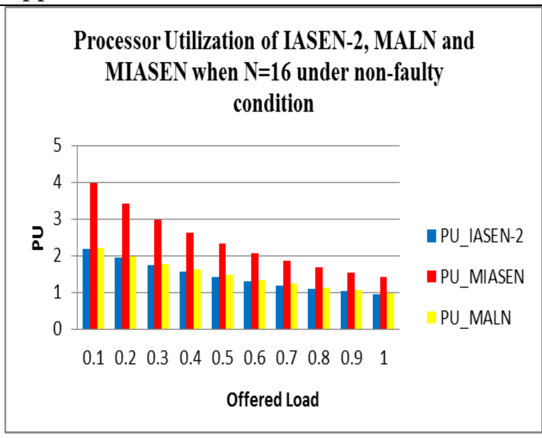

Fig. 6 Processor Utilization under Non-Faulty condition

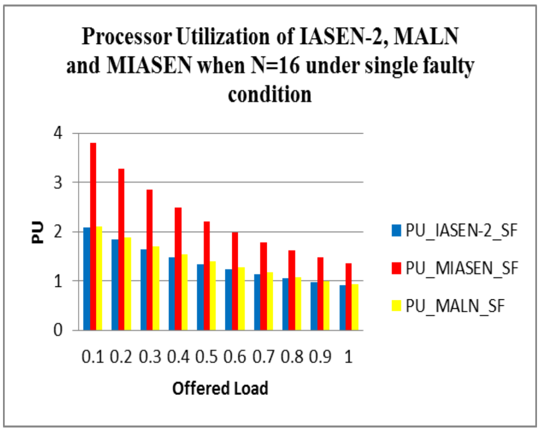

Fig. 7 Processor Utilization under Single Fault condition

5.5 Processing Power (PP)

Processing Power (PP) of MIASEN is greater than PP of IASEN-2 and MALN under faulty and non-faulty conditions.

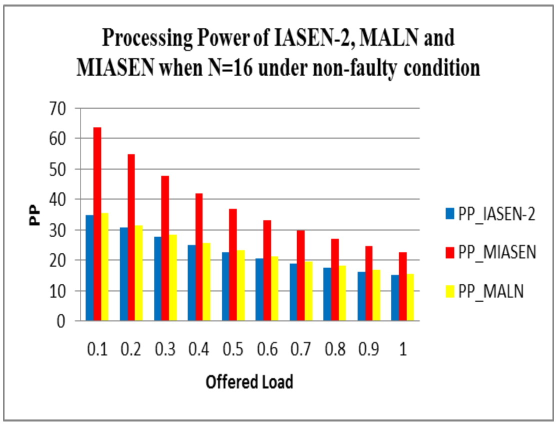

Fig. 8 Processing Power under Non-Faulty condition

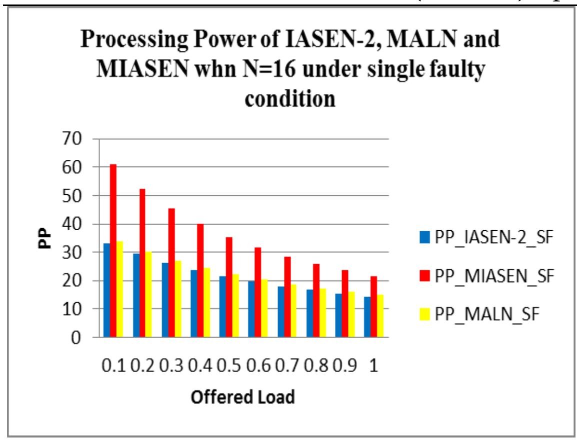

Fig. 9 Processing Power under Single Fault condition

VI. CONCLUSION

The results and analysis shows that the performance evaluation parameters of MIASEN give better results than that of IASEN-2 and MALN. The throughput, bandwidth, probability of acceptance, processor utilization and processing power of MIASEN are greater than IASEN-2 and MALN. Therefore, we can conclude that the Modified Irregular Augmented Shuffle exchange Network (MIASEN) is more fault-tolerant as compared to IASEN-2 and MALN.

REFERENCES

[1] Gupta A. and Bansal P. K., “Fault tolerant irregular modified alpha network and evaluation of performance parameters”. International Journal of Computer Applications. vol.4, no.1, 9–13, 2010.

[2] Rita Mahajan and Renu Vig, “A Performance and reliability analysis of new fault-tolerant advance omega network”, WSEAS Transactions on Computers, vol.7, no.8, 1280–1290, 2008.

[3] Mamta Ghai, Vinay Chopra, and Karamjit Kaur Cheema, “Performance analysis of fault-tolerant irregular baseline multistage interconnection network”, International Journal on Computer Science and Engineering, vol. 2, no. 9, pp. 3079–3084, 2010.

[4] C. C. Fan, and J. Bruck,“Tolerating multiple faults in multistage interconnection networks with minimal extra stages”, Comput. IEEE Trans., Vol. 49, no. 9, pp. 998-1004, 2000.

[5] P. H. Pham, J. Song, J. Park, and C. Kim, “Design and implementation of an on-chip permutation network for multiprocessor system-on-chip”, Very Large Scale Integration (VLSI) Syst. IEEE Trans., Vol. 21, no. 1, pp. 1537, 2013.

[6] J. Nathaniel Davis, William, Tsun-yuk Hsu and H. J. Siegel, “Fault location techniques for distributed control interconnection networks”, IEEE Transactions on Computers, Vol. C-34, No.10, October 1985.

[7] V. P. Kumar and S. M. Reddy, “Design and analysis of fault-tolerant multistage interconnection networks with low link complexity”, Proceedings of 12th International Symposium on Computer Architecture, 1985 June, pp. 376-386.

[8] Bansal, P. K., Joshi, R.C., Singh, K., “On a Fault tolerant Multistage Interconnection Network”, International Journal of Electronics and Electrical Engineering, 20(4), pp. 335-345,1994.

[9] V. P. Bhardwaj and Nitin, “A new fault tolerant routing algorithm for IASEN-2,” in Proceedings of the 2nd IEEE International Conference on Advances in Computing and Communications (ICACC ’12), pp. 199–202, 2012.

[10] Bansal P.K, Singh Kuldeep and Joshi R.C., “Quad Tree: A Cost-Effective Fault-Tolerant Multistage Interconnection network”, Proceeding of International Conference IEEE INFOCOM, 1992, pp. 6D.1.1-6D.1.7.

[11] Shobha Arya, Nipur Singh, “Reliability Analysis of Modified Irregular Augmented Shuffle Exchange Network (MIASEN)”, International Journal of Computer Science Issues, Vol. 14, No. 3, pp. 59-64, May 2017.

[12] Shobha Arya, Nipur Singh, “Performance Analysis of Fault Tolerant Advanced Irregular Shuffle Exchange Network (AISEN)”, Proceeding of ICTCS '16, March 04-05, 2016.

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