

## Optimization of Voltage, Delay, Power and Area for 16 bit Cyclic Redundancy Check (CRC) in VLSI Circuits using 45nm Technology

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### ABSTRACT

In Very-large-scale integration (VLSI) application area, delay and power are the important factors for any digital circuits. This paper presents 16 bit Cyclic Redundancy Check (CRC) mapped in Cadence Encounter(R) RTL Compiler Version v14.20-s013\_1. By efficiently mapping into cadence tool, area, power and delay are decreased. The results of mapping are viewed using RTL synthesis tool in cadence VIRTUOSO at 45nm technology and 0.7V. Based on digital signal processing (DSP) architectures, the code for low power is generated using 16 bit Cyclic Redundancy Check (CRC).

**Keywords:** High-Level Synthesis, 16 bit Cyclic Redundancy Check (CRC), low power, low area, delay, DSP, LUTs, VLSI.

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### I. INTRODUCTION

The design of complex chips has supported a series of transformations during the last twenty years. In the last few years, design for low power has initiated to change again how designers approach complex System on chip (SoC) designs. The aggressive increase in chip thickness drives the acceptance of synthesis provides the impressive growth in the era of millions of gate designs, engineers exposed that there was a restriction to how much new register transfer level (RTL) could be written for a new chip design. The result is that the IP and design related that the only way to design the VLSI chips relatively with few design units. This often plays an important role in receiver synchronization. R.Henkmat [2004] proposed a new model to calculate interference levels in wireless multi-hop ad-hoc networks. Robert C. Baumann [2005] presented radiation-induced soft errors in advanced semiconductor technologies. The once-ephemeral radiation-induced soft error has a key 14 threat to advanced commercial electronic components and systems. The soft errors have the potential for inducing the highest failure rate of all other reliability mechanisms combined. To prevent the SEU accumulation, TMR is often coupled with reconfiguration techniques such as full reconfiguration, partial reconfiguration (PR), or scrubbing. Most of the previous studies have used TMR with scrubbing or dynamic partial reconfiguration (DPR). DPR helps in hiding the configuration time and is effective for a

combinational circuit. X. Deng [2008] presented the RFID system; a reader recognizes tags through communications over a shared wireless channel. Using the simulation scheme, the reader detects a single tag from a tag population.

The system specifications are processor Intel (R) core (TM) i5-4570 CPU@3.20GHz.,3.20GHz.Installed memory (RAM) 4 GB (usable memory is 3.43GB) and system type: 32-bit operating system (OS).

This paper is formed as follows Section II presents the literature review on 16 bit CRC, LUTs and DSP Section III presents the methodology for 16 bit CRC and also discussed the low power analysis. Section IV shows the synthesis and simulation results and they are discussed clearly, finally the paper is concluded with Section V.

### II. LITERATURE REVIEW

It is really unreasonable for any data reporting or communication intermediate to be 100% perfect of the time over its entire expected useful life [1][2][3][4]. As more bits are arranged onto a square centimeter of disk storage, as information sending speeds increase, the likelihood of error increases sometimes geometrically. Thus, error detection and correction is critical to solid data transmission, storage and renewal. Check digits appended to the end of a long number can provide some protection against data input errors. Longer data streams have needed more efficient and practical error detection system. Cyclic redundancy checking (CRC) codes

provide error detection for large blocks of data. Checksums and CRCs are examples of systematic failure find. This group of bits is called a syndrome. As it is known CRCs are polynomials over the modulo 2 calculation field. They are use mathematics to tackle the problem of error detection [5][6][7]. CRC error checking is quite powerful and easily realized. In the presence of burst transmission errors, which each open and end with a bit error, with zero or more middle corrupted bits, the CRC can be a useful error find and improvement scheme [8][9][10].

CRC codes are based upon conducting bit strings as statements of polynomials with coefficient of 0's and 1's only. For example, 110001 has 6 bits and thus represents the six-term generating polynomial  $G(x) = x^5 + x^4 + 1$ . Polynomial arithmetic is done modulo 2, according to the rules of algebraic theory [11].

### III. DESIGN METHODOLOGY

#### A. Cyclic redundancy check

Error find is the process of observing data transmission and determining when errors have occurred. Error find techniques neither correct errors neither find which bits are in error they indicate only when an error has developed. The purpose of error detection is not to prevent errors from occurring but to prevent undetected errors from occurring. The most common error find techniques are redundancy checking, which includes vertical redundancy checking, check out, long redundancy checking, and cyclic redundancy checking.

#### B. CRC polynomial

The maximum reliable redundancy checking technique for error find is a convolution coding scheme called *cyclic redundancy checking* (CRC). With CRC, approximately 99.999% of all transmission errors are detected. In CRC-16, 16 bits are used for the block check sequence. Here, the entire data stream is treated as a long continuous binary number. CRC is considered a *systematic code*. CRC codes are often written as (n, k) cyclic codes where n are bit length of transmission and k is bit length of message. Therefore, the length of the Block Check Character (BCC) in bits is

$$BCC = n - k \dots \dots \dots (1)$$

A data information polynomial  $G(x)$  is branched by a particular generator polynomial function  $P(x)$ , the result is damaged and the rest is truncated to 16 bits and appended to the information as a BCS. The division is not accomplished with standard arithmetic division. Instead, modulo-2 division is used, since this remainder is derived from an exclusive or (XOR) procedure. 16 bit-CRC can be expressed as

$$G(x) \div P(x) = Q(x) + R(x) \dots \dots \dots (2)$$

where,

$G(x)$  = message polynomial

$P(x)$  = generator polynomial

$Q(x)$  = quotient

$R(x)$  = remainder

The generator polynomial for CRC-16 is

$$P(x) = x^{16} + x^{15} + x^2 + x^0 \dots \dots \dots (3)$$

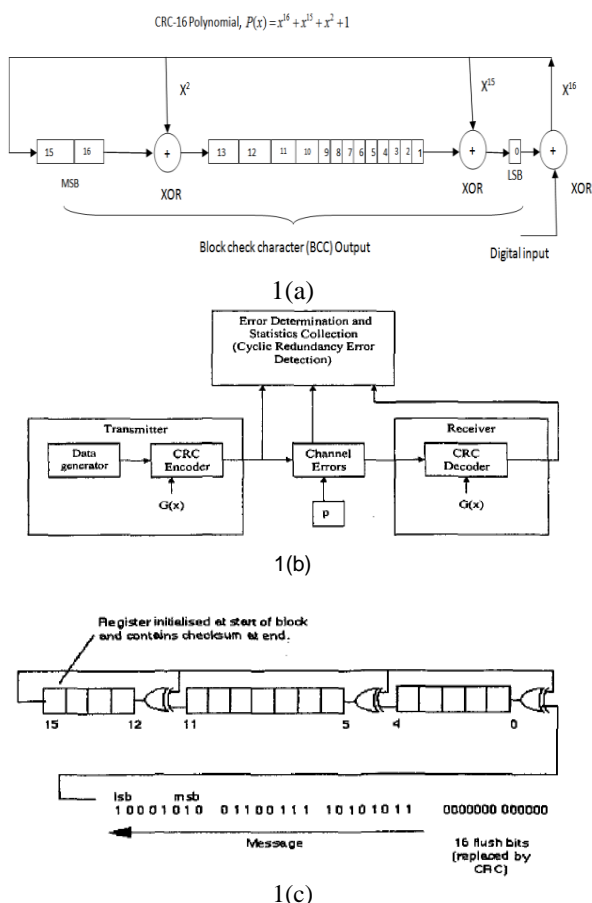


Figure 1 (a) CRC-16 Generating circuits [1], (b) Diagram of the basic digital communications and (c) basic Encoder and Decoder for 16-bit CRC [11].

A CRC generating circuit requires one shift register for each bit in the BCC.

#### C. Bit-to-symbol block

The 4 least significant bits (LSBs) (b0, b1, b2, b3) of each set is mapped into one data type and the 4 most significant bits (MSBs) (b4, b5, b6, b7) of each set is mapped into the next data type. Any group of protocol data unit (PPDU) is processed through the

bit-to-symbol block continuously, beginning with the Preamble field and opening with the end set of the PSDU.

## 2. Low Power analysis

### 2.1 Dynamic Power

The total power of System on Chip design consists of dynamic power and static power [12].

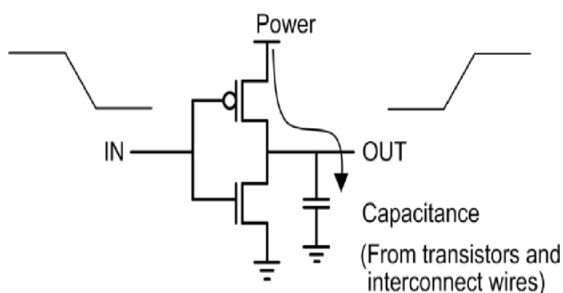


Figure 2: Dynamic Power [12].

Dynamic power is the power consumed when the material is in active mode. Whenever the device is in active mode the power dissipated in the device is called as Static power, but the signal values are unchanged.

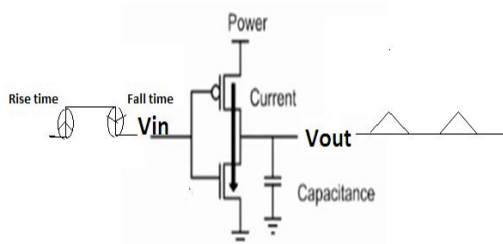


Figure 3: Short Circuit (Crow Bar) Power.

$$P_{SC} = I_{SC} * v \dots\dots\dots (2)$$

### 2.2 Static Power

Mainly the leakage currents are of four types. (Figure 4)

- Sub-threshold Leakage (ISUB): it is the current flows from drain to source which operates in inverse region.
- Gate Leakage (IGATE): it is the current flows from gate through oxide to the substrate [12].
- Gate Induced Drain Leakage (IGIDL): it is the current flows from drain to substrate caused by high voltage effect in MOSFET due to VDG.
- Reverse Bias Junction Leakage (IREV): it is the current caused because of minor drift and creation of electron hole pairs in the immobile region [12].

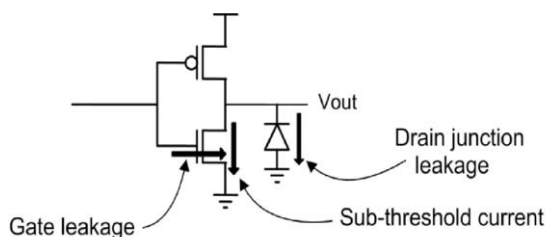


Figure 4: Leakage Currents [12]

$$P_{Static} = I_{Static} * v_{dd} \dots\dots\dots (3)$$

$$P_{Dynamic} = \alpha * c_L * v_{dd}^2 * f \dots\dots\dots (4)$$

$$P_{Shortcircuit} = I_{SC} * v \dots\dots\dots (5)$$

$$P_{Leakage} = V_{dd} * (I_S + I_G + I_D) \dots\dots\dots (6)$$

$$P_{Total} = P_{Dynamic} + P_{Leakage} \dots\dots\dots (7)$$

$$P_{Total} = (\alpha * c_l * v_{dd}^2 * f) + V_{dd} * (I_S + I_G + I_D) \dots\dots\dots (8)$$

Where  $\alpha$  is a switching activity factor,  $c_L$  is a load capacitance,  $V_{dd}$  is a voltage (drain to drain),  $f$  is a frequency,  $I_S$  (source current),  $I_G$  (Gate current) and  $I_D$  (Drain current) [12].

## IV. SYNTHESIS AND SIMULATION RESULTS

This paper presents 16 bit CRC is mapped in Cadence Encounter(R) RTL Compiler Version v14.20-s013\_1. By efficiently mapping into cadence tool, area, power and delay are decreased. The results of mapping are viewed using RTL synthesis tool in cadence VIRTUOSO at 45nm technology and 0.7V. Based on DSP architectures, the code for low power is generated using 16 bit CRC.

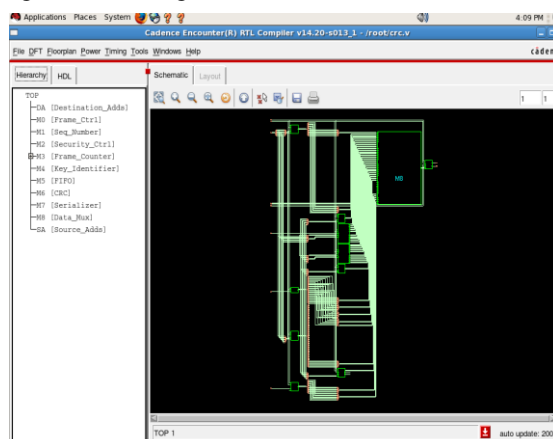


Figure 5 16 bit CRC schematic diagram of 45nm technology.

The proposed 16 bit CRC code is mapped into the cadence tool for synthesis and observed the schematic in figure 5.

We proposed mapping style into cadence tool 45nm using 16 bit CRC by observing the figure 8 16 bit CRC power attributes.

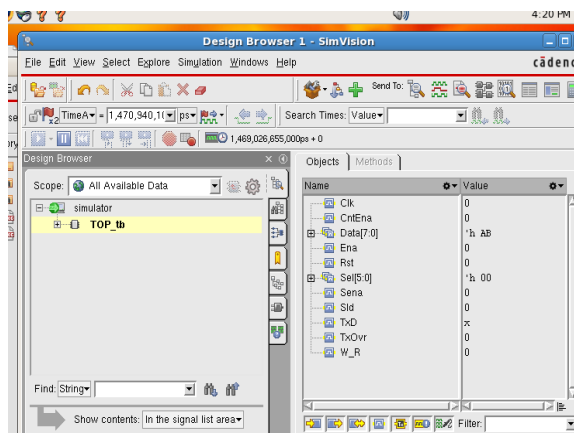


Figure 6 16 bit CRC design browser 1-simvision 45nm technology

The Figure 6 represents 16 bit CRC design browser 1-simvision. The 1-simvision gives the analysis of output waveforms respective input.

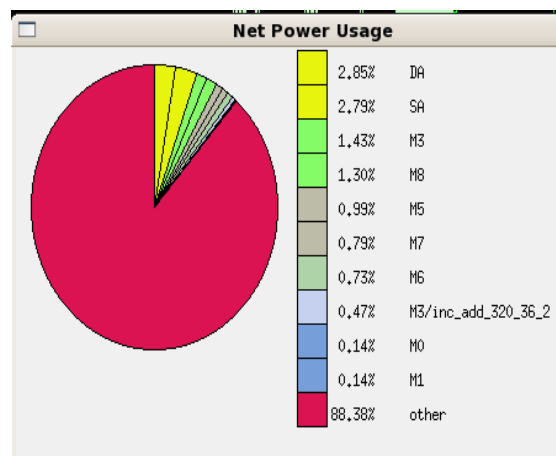


Figure 9 net power usages.

We proposed mapping style into cadence tool 45nm using 16 bit CRC. By observing the figure 9, 16 bit CRC net power usage

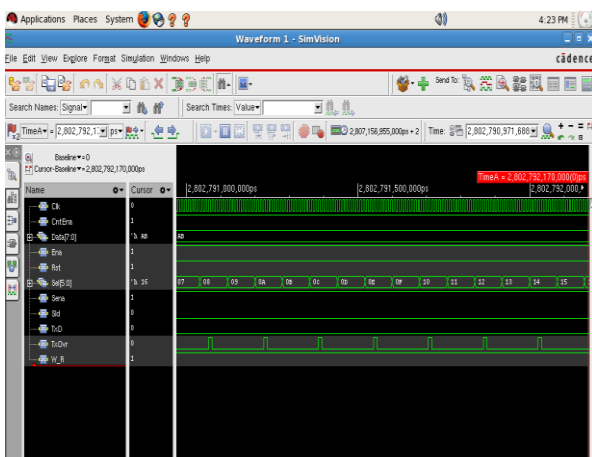


Figure 7 16 bit CRC of Simulation Result of 45nm technology.

In Figure 7, the design 16 bit CRC simulation is observed after mapping into the cadence tool at 45nm technology. The output of the 16 bit CRC waveform has the frequency of 356.2 mHz

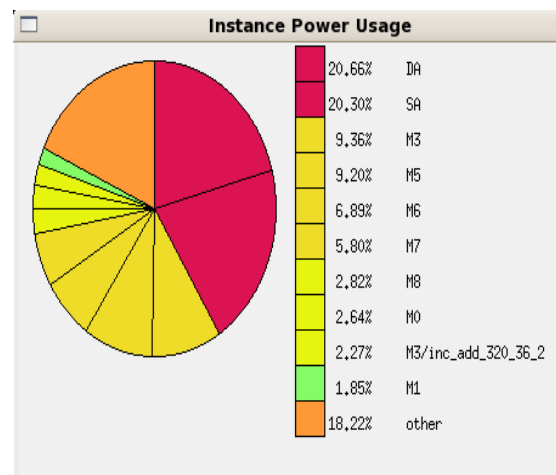


Figure 10 instance power usage.

We proposed mapping style into cadence tool 45nm using 16 bit CRC. By observing the figure 10, 16 bit CRC instance power.

Attribute	Value
Internal Power	39303.73
Leakage Power	179.79
Net Power	7960.79
Probability (default)	no_value
Toggle Rate (default)	no_value
Analysis Effort	medium

Figure 8 power attributes

Table 1 16 bit CRC area using cadence tool 45nm

Instance	Cells	Cell Area	Net Area	Total Area
TOP	963	3123	0	3123
SA	197	754	0	754
DA	197	754	0	754
M8	234	416	0	416
M3	125	356	0	356
inc_add_320_36_2	61	115	0	115
M5	62	260	0	260

M6	29	144	0	144
M7	39	138	0	138
M0	32	120	0	120
M4	16	60	0	60
M2	16	60	0	60
M1	16	60	0	60

We proposed mapping style into cadence tool 45nm using 16 bit CRC. By observing the table 1, 16 bit CRC area.

**Table 2** 16 bit CRC power dissipation using cadence tool 45nm

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
TOP	963	179.785	47264.519	47444.304
SA	197	43.082	10909.920	10953.002
DA	197	43.065	11111.119	11154.183
M3	125	22.012	5095.591	5117.603
inc_add_320_36_2	61	7.007	1289.045	1296.053
M8	234	21.475	1932.117	1953.591
M5	62	14.461	4817.515	4831.976
M6	29	8.704	3607.428	3616.132
M7	39	8.198	3118.946	3127.144
M0	32	7.497	1309.483	1316.980
M1	16	3.764	941.727	945.491
M2	16	3.764	941.727	945.491
M4	16	3.764	941.727	945.491

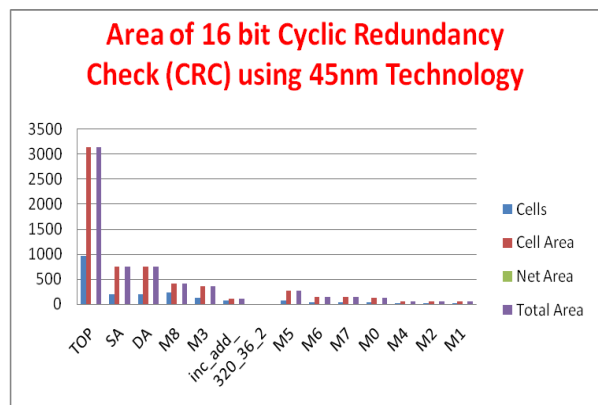
We proposed mapping style into cadence tool 45nm using 16 bit CRC. By observing the table 2, 16 bit CRC power dissipation.

**Table 3** 16 bit CRC delay using cadence tool 45nm

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
M3				0		0 R
Frame_Count_reg[0]_1/CK						
Frame_Count_reg[0]_1/Q	DDFRHQX1	4	1.7	15	+59	59 R
inc_add_320_36_2/A[0]					+0	59
g277/A						
g277/Y	NAND2BXL	2	0.8	22	+21	80 F
g275/AN					+0	80
g275/Y	NAND2BXL	2	0.8	22	+27	108 F
g273/AN					+0	108
g273/Y	NAND2BXL	2	0.8	22	+27	135 F
g271/AN					+0	135
g271/Y	NAND2BXL	2	0.8	22	+27	162 F
g269/AN					+0	162
g269/Y	NAND2BXL	2	0.8	22	+27	189 F
g267/AN					+0	189
g267/Y	NAND2BXL	2	0.8	22	+27	216 F
g265/AN					+0	216
g265/Y	NAND2BXL	2	0.8	22	+27	244 F
g263/AN					+0	244
g263/Y	NAND2BXL	2	0.8	22	+27	271 F
g261/AN					+0	271
g261/Y	NAND2BXL	2	0.8	22	+27	298 F
g259/AN					+0	298
g259/Y	NAND2BXL	2	0.8	22	+27	325 F
g257/AN					+0	325
g257/Y	NAND2BXL	2	0.8	22	+27	352 F
g255/AN					+0	352
g255/Y	NAND2BXL	2	0.8	22	+27	380 F
g253/AN					+0	380
g253/Y	NAND2BXL	2	0.8	22	+27	407 F
g251/AN					+0	407
g251/Y	NAND2BXL	2	0.8	22	+27	434 F
g249/AN					+0	434
g249/Y	NAND2BXL	2	0.8	22	+27	461 F
g247/AN					+0	461
g247/Y	NAND2BXL	2	0.8	23	+27	488 F
g245/AN					+0	488
g245/Y	NAND2BXL	2	0.8	23	+27	516 F

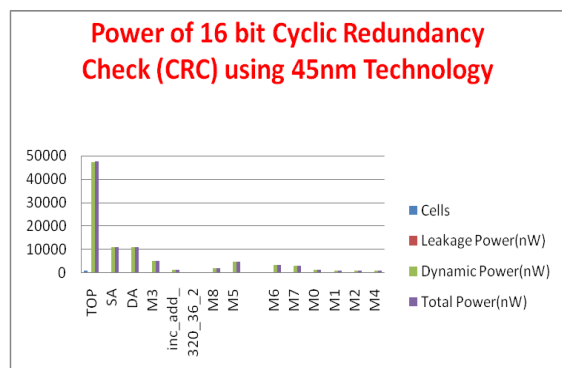
g243/AN					+0	516	
g243/Y	NAND2BXL	2	0.8	23	+27	543 F	
g241/AN					+0	543	
g241/Y	NAND2BXL	2	0.8	23	+27	570 F	
g239/AN					+0	570	
g239/Y	NAND2BXL	2	0.8	23	+27	597 F	
g237/AN					+0	597	
g237/Y	NAND2BXL	2	0.8	23	+27	624 F	
g235/AN					+0	624	
g235/Y	NAND2BXL	2	0.8	23	+27	652 F	
g233/AN					+0	652	
g233/Y	NAND2BXL	2	0.8	23	+27	679 F	
g231/AN					+0	679	
g231/Y	NAND2BXL	2	0.8	23	+27	706 F	
g229/AN					+0	706	
g229/Y	NAND2BXL	2	0.8	23	+27	733 F	
g227/AN					+0	733	
g227/Y	NAND2BXL	2	0.8	23	+27	760 F	
g225/AN					+0	760	
g225/Y	NAND2BXL	2	0.8	23	+27	788 F	
g223/AN					+0	788	
g223/Y	NAND2BXL	2	0.8	23	+27	815 F	
g221/AN					+0	815	
g221/Y	NAND2BXL	2	0.8	23	+24	842 F	
g219/AN					+0	842	
g219/Y	NAND2BXL	1	0.5	17	+35	866 F	
g217/B					+0	866	
g217/Y	XNOR2X1	1	0.3	6	+24	901 R	
inc_add_320_36_2/z[31]					+0	901	
g68/A							
g68/Y	AND2X1	1	0.4	6	+24	925 R	
Frame_Count_reg[3]_1/D	DDFRHQX1				+0	925	
Frame_Count_reg[3]_1/CK	setup				0	+21	946 R

We proposed mapping style into cadence tool 45nm using 16 bit CRC. By observing the table 3, 16 bit CRC delays.



**Figure 11** area of 16 bit CRC in 45nm technology.

We Design mapping style in cadence tool. Figure 11 gives the area of 16 bit CRC in 45nm technology.



**Figure 12** power dissipation of 16 bit CRC in 45nm technology.

We Design mapping style into cadence tool. Figure 12 gives power dissipation of 16 bit CRC in 45nm technology.

## V. CONCLUSION

In this paper, we proposed mapping style into cadence tool using 16 bit CRC. Table 1 gives 16 bit CRC of area at 45nm technology, table 2 represents 16 bit CRC of power dissipation at 45nm technology and table 3 represents 16 bit CRC of delay at 45nm technology and power given is 0.7V. With the help of DSP architectures, the code is generated which results in low power.

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