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Utilizaton of Wallace Tree Multiplier in the Design of Scalable Microprogrammed Fir Filter Architectures

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ABSTRACT
Field programmable gate array (FPGA) is widely used for efficient hardware realization of digital signal processing (DSP) circuits and systems. FPGAs have emerged as a platform of choice for faster and efficient realization of computer-intensive applications. Finite impulse response (FIR) filter is the core of any DSP and communication system To improve the performance of FIR filter, an efficient multiplier is required..Wallace multiplier used in this project for the implementation of sequential and parallel microprogrammed FIR filter architectures.The designs are realized using Xilinx Spartan-6 FPGA.
Tools used: Xilinx ISE 14.1, Spartan-6 FPGA.
Keywords: FPGA; FIR Filter; micro programmed; multiplier.

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I. INTRODUCTION

Filtering is one of the fundamental steps in many digital signal processing (DSP) applications such as video processing, image processing and wireless communication. Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communication channels, signal detection or analysis in radar applications. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. These building blocks are arranged and interconnected in different ways according to the filter architecture. Different architecture of digital filters can be realized to achieve the same transfer function. The architectures possess different attributes in the form of speed, complexity and power dissipation [1].

Finite impulse response (FIR) and infinite impulse response (IIR) are two such filters used in different applications. FIR filters are the important building blocks for digital signal, video and image processing applications. Basically, FIR filter performs a convolution on a window of N data samples. A common implementation of the FIR filter is shown in fig. 1, which is also known as direct form FIR filter. As can be seen from the figure, N-tap or (N-1)th order FIR filter consist of N shift registers, N multipliers and N-1 adders. The impulse response of the FIR filter can be directly inferred from the tap coefficients (W). The multiplier is the fundamental component which decides the overall performance of the FIR filter [2].

The objective of this paper is to extend the work originally proposed in [5-8] by implementing the sequential and parallel micro programmed FIR filters using Wallace tree multipliers in FPGA and evaluating their performance for different number of taps.

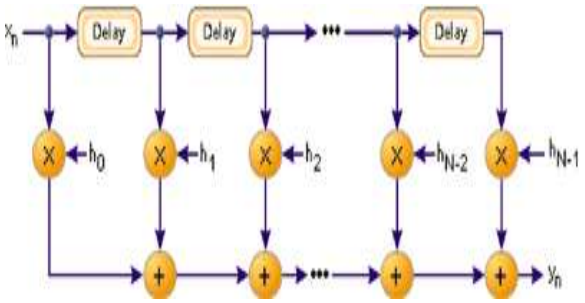


Figure 1.1: The Logical Structure of an FIR filter

II. MICRO PROGRAMMED FIR FILTER

2.1 Micro programmed FIR Filter

The microprogrammed FIR filter consists of a data path and microprogram control unit (MCU). The most important advantage of the MCU is its flexibility. It consists of two main parts. The first part is designed for addressing the microinstructions stored in the control memory and the second part is designed to hold and generate microinstructions for the data path unit.

2.2 Sequential Architecture of Microprogrammed FIR Filter

The sequential architecture of *N*-tap microprogrammed FIR filter is shown in Fig. 2.1 It basically comprises of a MCU and a datapath unit. The MCU consists of a microprogram counter and microprogram memory. The datapath unit comprises of 2*N* data (X) and coefficient (W) registers and *M*-to-*N* decoder (*M = log2N*), two *N*-input multiplexers for selecting the data and coefficients, a multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 16-bit accumulator and a 16-bit register to latch the data.

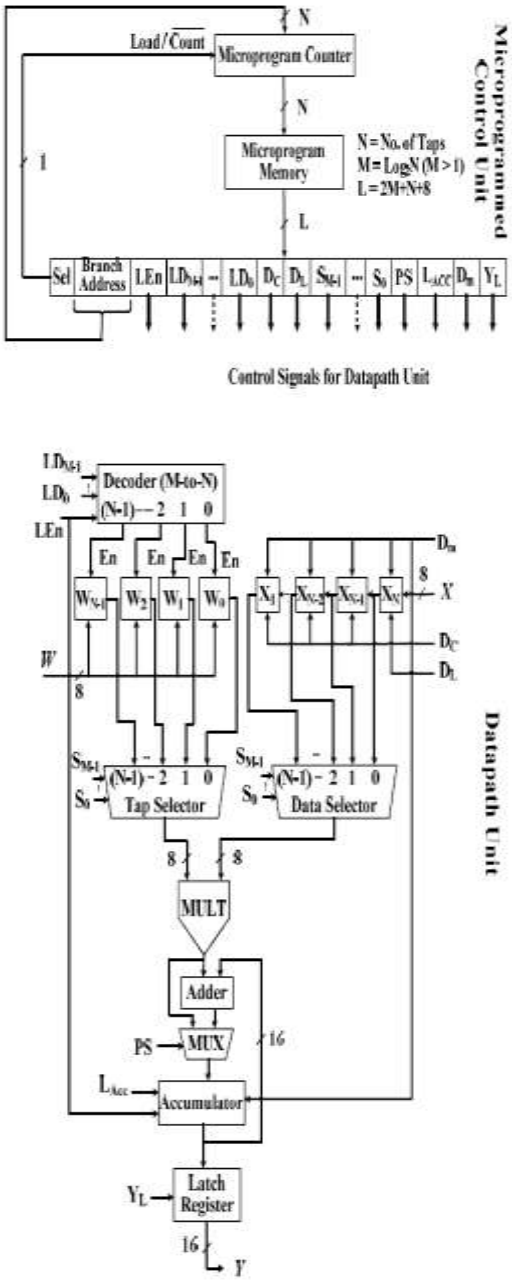


Fig. 2.1Architecture of sequential microprogrammed FIR filter

2.3 Parallel Architecture of Microprogrammed FIR Filter

The parallel architecture utilizes multiple adders and multipliers, based on the size of the FIR filter, in contrast to single adder and multiplier used in the sequential architecture design. Fig. 2.2 illustrates the parallel architecture of the microprogrammed FIR filter [8]. For example, the datapath micro architecture of 4-tap parallel FIR filter consists of the following sub-modules:

- Four 8-bit data registers
- One 2-to-4 decoder
- Four 8-bit coefficient registers
- Four multipliers (8×8)
- Three 16-bit adders
- One 16-bit register for latching the output

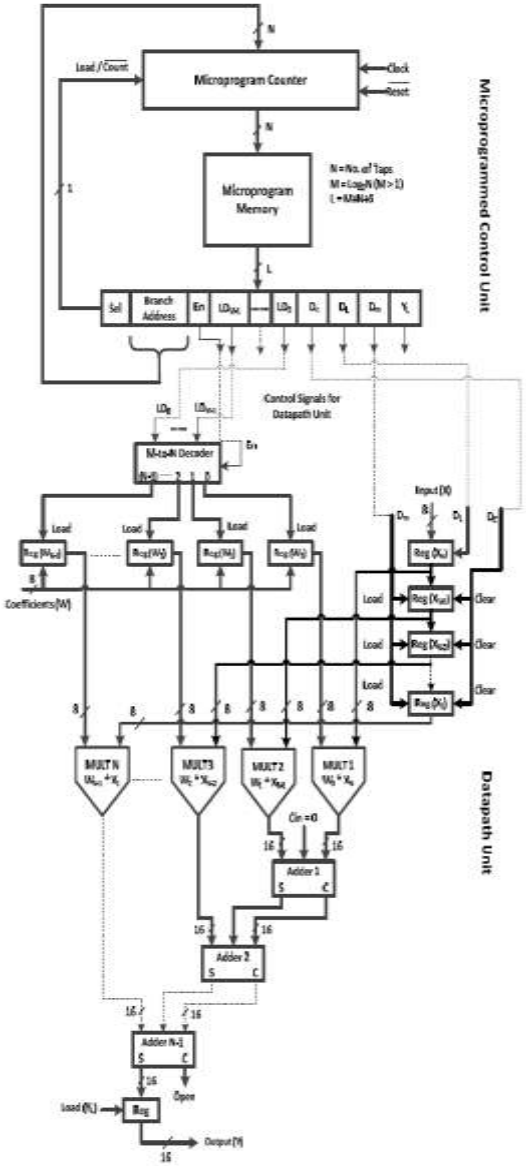


Fig. 2.2 Architecture of Parallel microprogrammed FIR filter

III. DESIGN OF WALLACE TREE MULTIPLIER

3.1 Wallace Tree Multiplier Design

A method for fast multiplication was originally proposed by Wallace. Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Using this method, a three step process is employed to multiply two integer numbers. The first step is to multiply each bit of one of the arguments, by each bit of the other, yielding *n2* results. Based on the position of the multiplied bits, the wires carry different weights. The second step is to reduce the number of partial products to two by layers of full and half adders. The third step is to group the wires in two and then add them using conventional adder. In this paper, two different architectures of Wallace tree multiplier are presented. First one is designed using only half adder and full adder, while the second one uses a more sophisticated carry skip adder (CSA).

3.2 Wallace Tree Multiplier using Full and Half Adders

The Wallace tree method reduces the number of adders by minimizing the number of half adders in any multiplier. In 8×8 multiplier, the first partial product is the least significant bit in the output of the multiplier result. After that, moving to the next column of the partial product if there are any adders from the previous product, the full adder is used otherwise a half adder is used and so on. The Following figures show how the algorithm is implemented.

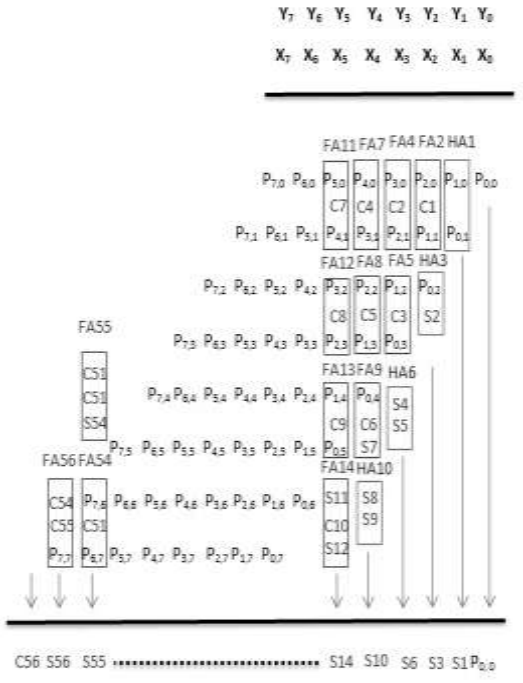


Fig. 3.1 Wallace Tree partial product addition using half and full adders.

3.3 Wallace Tree Multiplier using Carry Skip Adder

A carry-skip adder consists of a simple ripple carry-adder (RSA) with a special speed up carry chain called a skip chain. The purpose of using the CSA is to improve the worst case path delay. In this work, we used a 4-bit CSA for implementing the Wallace tree multiplier.

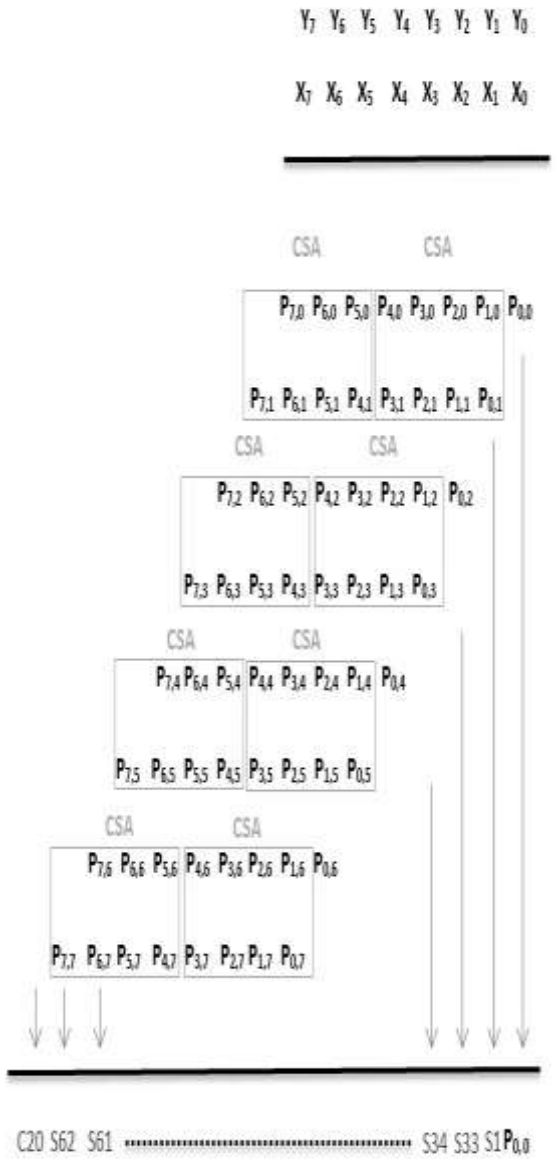


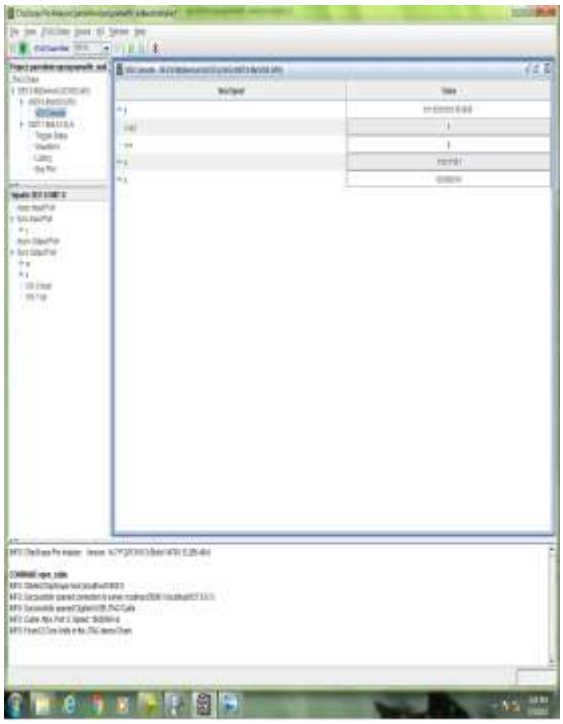
Fig. 3.2. Wallace tree partial product addition using carry skip adder.

In this design, 4-bit carry skip is used for the addition of partial products. Four bits from one row is being added with the next row as shown in Fig. 3.2 and the carry output from the first addition is the carry input for the second addition. The main advantage of using CSA is to improve the speed.

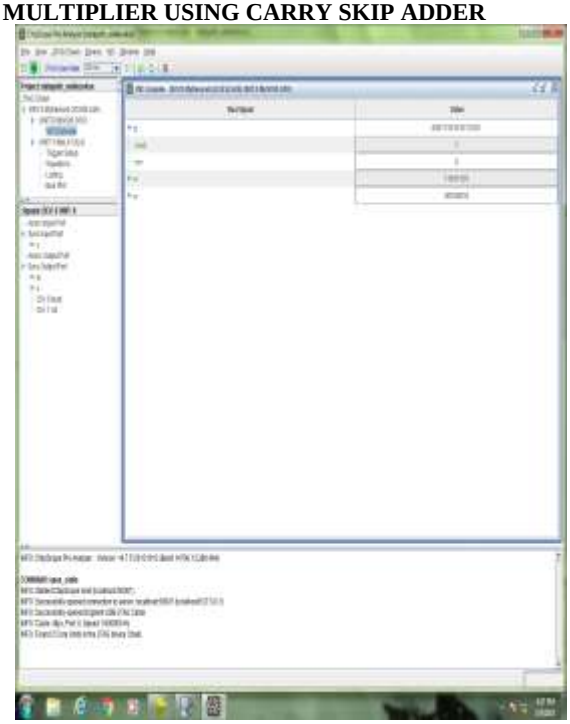
IV. SIMULATION RESULTS

4.1 PARALLEL MICROPROGRAMMED FIR FILTER ARCHITECTURE BY WALLACE TREE MULTIPLIER USING CARRY SKIP ADDER

4.2 PARALLEL MICROPROGRAMMED FIR FILTER ARCHITECTURE BY WALLACE TREE MULTIPLIER USING HALF AND FULL ADDER



4.3 SEQUENTIAL MICROPROGRAMMED FIR FILTER ARCHITECTURE BY WALLACE TREE MULTIPLIER USING CARRY SKIP ADDER



4.4 SEQUENTIALMICROPROGRAMMED FIR FILTER ARCHITECTURE BY WALLACE TREE MULTIPLIER USING HALF AND FULL ADDER

V. CONCLUSION

FPGAs have emerged as a platform of choice for faster and efficient realization of computer-intensive applications. Finite impulse response (FIR) filter is the core of any DSP and communication system. Wallace multiplier used in this project for the implementation of sequential and parallel microprogrammed FIR filter architectures. Hence the designs are realized using Xilinx Spartan-6 FPGA.

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