RESEARCH ARTICLE OPEN ACCESS

Performance Evaluation of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology

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ABSTRACT
This paper reviews study of symmetrical and asymmetrical cascaded H-bridge multilevel inverter. Here symmetrical, binary asymmetrical and ternary asymmetrical structure formed by cascading two H-bridge cells are compared in order to find an optimum arrangement with high quality output voltage. Performance of these structures is verified through computer simulation using MATLAB/Simulink.
***Index Terms**:* symmetrical, asymmetrical, Cascaded H Bridge, multilevel inverter, Total harmonic distortion (THD).

Date of Submission: 17 -07-2017 Date of acceptance: 31-07-2017

I. INTRODUCTION

The elementary concept of multilevel inverter (MLI) is to attain higher power by using number of power switches with several low voltage dc sources. It can synthesize output voltage waveform in steps closer to sine wave and reduces total harmonic distortion. Recently multilevel inverters have been used in various industrial applications like distributed generation ,adjustable speed drives, flexible ac transmission system, HVDC, electrical vehicles etc. due to prominent advantages like high quality output voltage using low switching frequency, low harmonic contents, low electromagnetic interference, less voltage stress on power switches, more efficiency and low dv/dt stress on load [1]-[6].

Enhancement in these advantages is possible by increasing number of levels of output voltage waveform but it requires large number of switches that makes circuit complex. It also raises cost and size of the circuit.

There are three main multilevel inverter topologies-neutral point clamped (NPC) [7], flying capacitor (FC) [8] and cascaded H bridge (CHB). CHB has become famous because of its modular design, simple control, reliability, availability and the absence of capacitor imbalance problem [9].

In this paper we are focusing on CHB topology which is series connection of several H-Bridge cells with equal and un-equal magnitude of dc sources called as symmetrical and asymmetrical structures.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The cascaded H-bridge multilevel inverter is an arrangement of several units of single-phase H-bridge power cells. The H bridge cells are connected in series on their ac side to attain medium voltage operation and low harmonic distortion. Each H-bridge power cell which is the building block for the cascaded H-bridge inverter is supplied by an isolated dc source on the dc side. Batteries, fuel cells or ultra-capacitors are used as isolated dc sources [10]. Fig. 1 shows single-phase structure of a cascade inverter with two H-bridges supplied by isolated dc voltage sources. An output voltage waveform is obtained by summing the output voltage of both the cells connected in series.

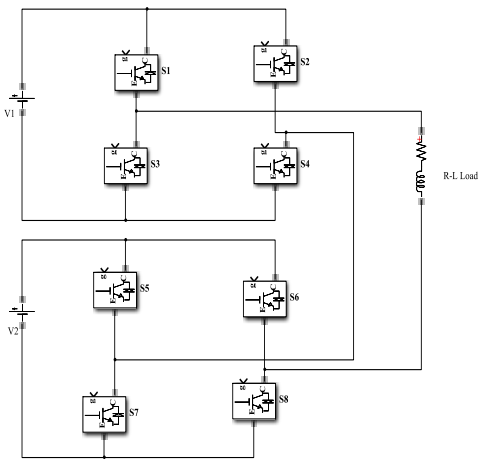

Fig. 1. Single phase structure of CHB inverter

If *n* number of cells is connected in series then total voltage across the load terminal is

$$(V_L)_T = (V_L)_1 + (V_L)_2 + \ldots\ldots\ldots + (V_L)_n$$

$$(V_L)_T = \sum_{k=1}^{n} (V_L)_n \quad (1)$$

A. Symmetrical Cascaded H-Bridge Multilevel Inverter

If all the dc voltage sources of CHB- MLI are of equal magnitude then it is called as a symmetrical MLI. Following equations can be written for this configuration,

$$V_k = E \quad (2)$$

$$k = 1, 2, \ldots\ldots\ldots n.$$

Means $V_1 = V_2 = \ldots\ldots = V_n = E$

The effective number of output voltage levels *m* in symmetric multilevel inverter is given by

$$m = 2n + 1 \quad (3)$$

$$V_M = n\,E \quad (4)$$

Where *n* is number of power cells used for cascade structure and V_M is maximum voltage generated.
For example, if *n=2* as shown in Fig. 1 it generates 5 level voltage with maximum voltage *2E*.

B. Asymmetric Cascaded H-Bridge Multilevel Inverter

In order to generate large number of output levels without increasing the number of cells, asymmetric multilevel inverters can be used. The magnitude of dc voltages sources can be selected according to a geometric progression with a factor of 2 or 3 [11].
If dc voltage sources are in the ratio of 1:2, then the inverter is known as binary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 2^{(k-1)} E$$

$$k = 1, 2, \ldots\ldots\ldots n. \quad (5)$$

The effective number of output voltage levels *m* and maximum voltage generated can be expressed as

$$m = 2^{(n+1)} - 1 \quad (6)$$

$$V_M = (2^n - 1)E \quad (7)$$

For two H-bridge cascaded topology this configuration generates 7 levels with maximum value *3E*.
If dc voltage sources are in the ratio of 1:3, then the inverter is known as ternary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 3^{(k-1)} E$$

$$k = 1, 2, \ldots\ldots\ldots n. \quad (8)$$

In this case number of voltage levels and maximum voltage generated can be calculated as

$$m = 3^n \quad (9)$$

$$V_M = \frac{(3^n - 1)}{2} E \quad (10)$$

Now, this configuration generates 9 levels with maximum voltage *4E* for Two H Bridge cascaded topology.

III. COMPARISON BETWEEN SYMMETRIC AND ASYMMETRIC CONFIGURATION OF CASCADED H-BRIDGE MULTILEVEL INVERTER

From above discussion it is clear that ternary asymmetrical multilevel inverter can generate more voltage levels and higher maximum output voltage with the same number of bridges as compared to symmetrical and binary asymmetrical configuration. Table I presents comparison based on the number of levels *(m)*, number of switches *(Nsw)*, dc sources *(Ndc)* maximum output voltages (V_M)and number of different voltage magnitudes *(Nv)* total voltage blocked by switches (V_{bt})when *n* number of cells are connected in series.

Fig. 2 compares number of switches required to generate specific number of output voltage levels and Fig. 3 shows number of dc sources required for the three configurations. It is clear that ternary asymmetric configuration needs less components.

TABLE I
COMPARISON OF SYMMETRIC AND ASYMMETRIC CHB-MLI

Parameters	Symmetric configuration	Asymmetric configuration	
		Binary	Ternary
m	$2n+1$	$2^{(n+1)}-1$	3^n
Nsw	$4n$	$4n$	$4n$
Ndc	n	n	n
V_M	nE	$(2^n-1)E$	$\frac{(3^n-1)}{2}E$
Nv	1	n	n
V_{bt}	$4nE$	$4(2^n-1)E$	$2(3^n-1)E$

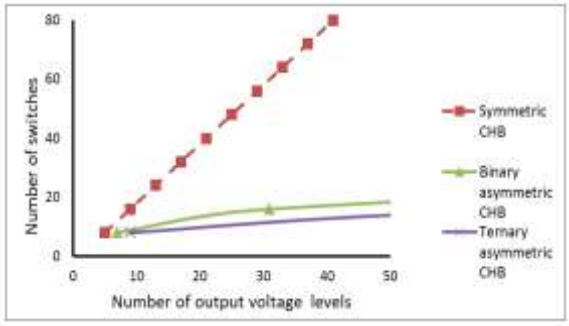

Fig. 2. Number of switches versus number of output voltage levels

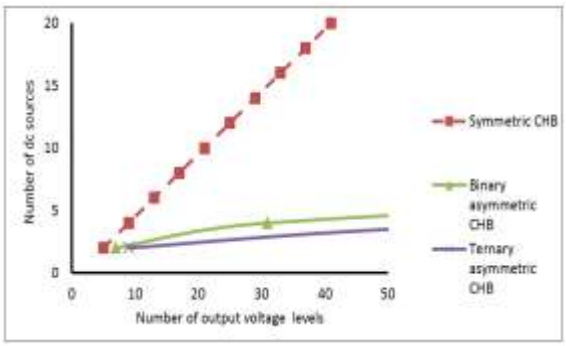

Fig. 3. Number of dc sources versus number of output voltage levels

IV. MODULATION TECHNIQUE

The objective of modulation scheme used to control inverter is to obtain quality waveform (voltage/current) with minimum losses. Several modulation strategies have been developed for multilevel inverters. Among the commonly used modulation techniques, Pulse Width Modulation (PWM) is simple and gives high performance and therefore the most successful technique. The conventional sinusoidal PWM technique can be applied to multilevel inverter topologies by using multiple carriers. Therefore it is known as multi-carrier PWM technique. A sinusoidal reference waveform of fundamental frequency is compared with high frequency carrier waveforms having same amplitude. For *m* level inverter $(m-1)$ carriers are required [12]. The output of comparator is high if the triangular carrier is greater than the reference signal and low otherwise. The sum of the different comparisons represents signal for output voltage level.

A multicarrier level shifted phase disposition PWM scheme is used in this paper to generate pulses for the switches of CHB-MLI.

V. SIMULATION RESULTS

In this paper, simulation models for five level symmetrical, seven level binary asymmetrical and nine level ternary asymmetrical CHB-MLI are developed in MATLAB/Simulink environment. For each configuration two H –bridges are used, so that number of switches and number of dc sources in all the models are same. The switches used in the simulations are assumed to be ideal. Separate dc sources are used in the simulation studies. In practice these dc voltage sources are available via distributed energy resources like photovoltaic panels, fuel cells and ultra- capacitors. If the available source is an ac source then the required dc voltage sources can be obtained by using rectifiers. Simulation parameters used are given in Table II and results are shown from Fig. 4 to Fig. 9. Comparison is given in Table III.

TABLE II
SIMULATION PARAMETERS

Description	Parameter	Value
Symmetrical inverter	V_1	120 volts
	V_2	120 volts
Binary asymmetrical inverter	V_1	160 volts
	V_2	80 volts
Ternary asymmetrical inverter	V_1	180 volts
	V_2	60 volts
Load	Resistance	100 ohms
	Inductance	10 mH

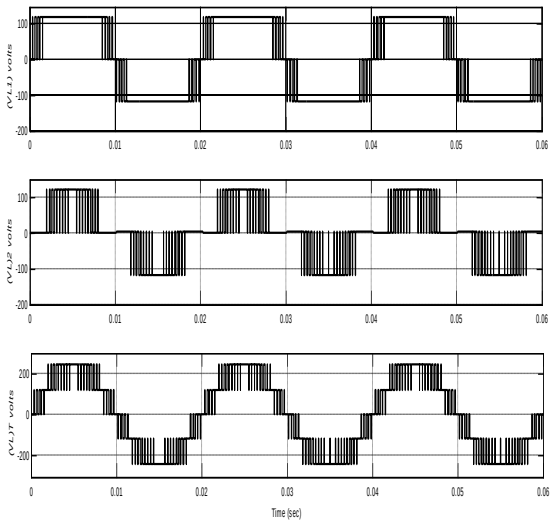

Fig.4. 5-level output voltage synthesis of symmetric CHB inverter

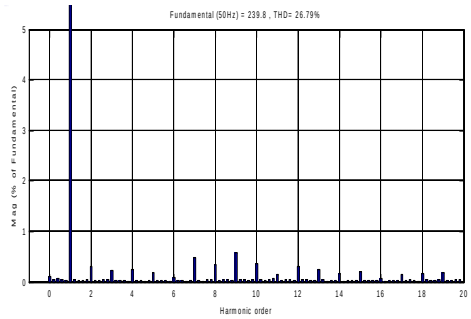

Fig.5. FFT analysis of output voltage of five level symmetric CHB inverter

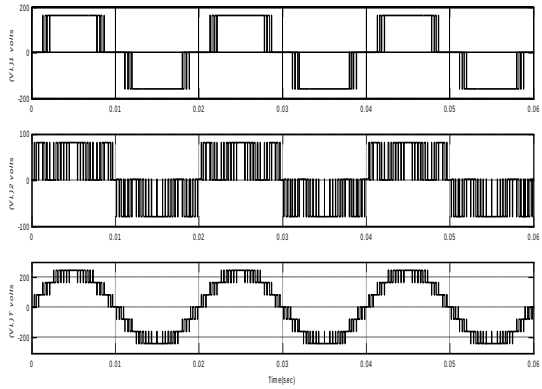

Fig.6. 7-level output voltage synthesis of binary asymmetric CHB inverter

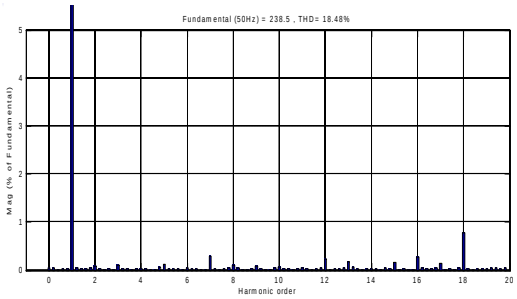

Fig.7. FFT analysis of output voltage of seven level binary asymmetric CHB inverter

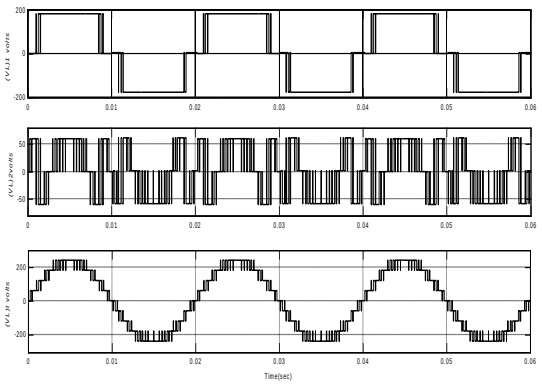

Fig.8. 9-level output voltage synthesis of ternary asymmetric CHB inverter

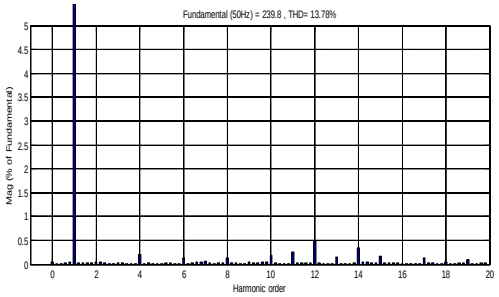

Fig.9. FFT analysis of output voltage of nine level ternary asymmetric CHB inverter

TABLE III
COMPARISON OF PERFORMANCE PARAMETERS OF SYMMETRICAL AND ASYMMETRICAL CHB INVERTER

Parameters	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
Number of dc sources	2	2	2
Number of switches	8	8	8
Fundamental Frequency	50 Hz	50 Hz	50 Hz
Carrier frequency	3 kHz	3 kHz	3 kHz
Voltage levels	5	7	9
V_L (volts)	239.8	238.5	239.8
Voltage THD (%)	26.79	18.48	13.78

VI. CONCLUSIONS

This paper presents comparison of symmetrical, binary asymmetrical and ternary asymmetrical CHB-MLI with two H-bridges in series. MATLAB/Simulink models are developed for all the three topologies. Using PD-PWM a pulse generation circuit is designed. From simulation results it is observed that the generated voltage spectrum is very much improved for nine level inverter topology. Among three configurations ternary- CHB inverter requires least number of switches and dc sources and generates high quality voltage with minimum harmonics.

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Aparna Prayag. "Performance Evaluation of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology ." International Journal of Engineering Research and Applications (IJERA) 7.7 (2017): 20-24.