RESEARCH ARTICLE OPEN ACCESS

Cascaded H-Bridge Multilevel Inverter Using SPWM and MSPWM Strategies

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ABSTRACT
Nowadays, the multilevel inverter is growing hugely in medium voltage-high power applications. It produces staircase output voltage near sinusoidal waveform. The multilevel inverter is as compared to a two level inverter has high output voltage at high switching frequency , less EMI (electro-magnetic interference), lower THD (total harmonics distortion), low voltage stress (dv/dt) and it reduces the size of the filter components. In this paper various techniques cascaded H-bridges inverter are designed and implemented. Single phase sinusoidal pulse width modulation (SPWM) and modified sinusoidal pulse width modulation (MSPWM) topologies of (three, five and seven) levels inverters are designed and implemented. The results in percentage value of THD before and after filter are compared. The simulink/matlab and proteus are used to simulate the systems and finally, result are obtained experimentally using microcontroller (arduino mega 2560). When the number of levels is increased using SPWM technique the THD reduced, THD improves in MSPWM technique too, and comparison table II illustrated that.

Keywords **:** SPWM, MSPWM, THD, FFT, cascaded H-bridge

I. INTRODUCTION

Renewable energy supplies are feeding into the grid enormously with higher accuracy and fewer power losses. Photovoltaic cells are a distributed energy source that could be installed on each consumer place like on the surface of a house, these photovoltaic transports the power using a converter to produce ac voltage from dc voltage of cells [1-3]. The two levels inverter has high harmonics and power losses. Multilevel inverter is a modern structure of inverter consists of dc sources and switches which attract the researchers and industries. It synthesize a desired ac voltage which closer to sine wave. Consequently it has lower total harmonics distortion (THD) and minimum power losses [4-6]. Various multilevel inverters types have been presented while several of them established their methods to the industries [7،8]. Cascaded H-bridges inverter is such as common topology that extensively manufactured by companies and used as useful power conversion [9]. SPWM or MSPWM technique is applied on cascaded H-bridges converter switches to obtain synthesize voltage waveform. These techniques have higher switching frequency and lower harmonics.

Kureve D. Teryima et al. [11] proposed a five level cascaded H-bridge inverter using overlapping carrier based on SPWM technique, the carrier frequency is equal to 5 KHz and fundamental frequency of 50Hz, the THD of output voltage is high.

Tejas M. Panchal et al. [12] presented modified cascaded H-bridge inverter for three-phase asynchronous motor, the zero harmonic spectrum (dc) is high value that caused damage in inductive, transformer and other components because of the heat problem, this heat is due to existence of dc component.

K. Rachel et al. [13] proposed a seven level cascaded H-bridge inverter using carrier overlapping SPWM and implemented in two H-bridge for PD, POD and APOD topology, the THD result is very high in output voltage.

Vinayaka B.C et al. [14] presented the design of five level cascaded H-bridge inverter with dc/dc converter, the output voltage with filter has distortion and it does not closer to ideal sinusoidal thus the THD is high.

In this paper three, five and seven levels cascaded H-bridges design and implemented using SPWM and MSPWM techniques. The resulted THD before and after filter are compared with the above papers [11-14].

Principle of operation of the multilevel inverter is presented in section II. SPWM and MSPWM techniques used to control the output are introduced in section III and section IV respectively. Proteus and hardware realization is explained in section V. Section VI presents the software algorithm. Conclusion is given in section VII.

II. MULTILEVEL INVERTER

Principally, inverter is a technique that converts power from dc to ac. The industries required high power with fewer harmonic for high power applications, therefore the multilevel inverter idea is presented to obtain ac output voltage with reduce harmonics. The cascaded H-bridge type of multilevel inverter is more popular than diode clamped and flying capacitors because it does not require any voltage balancing capacitors or clamping diodes. The output terminals of H-bridge are connected in series with other output terminals of another H-bridge to produce an ac voltage via summation of the output H-bridges as shown in fig. 1. The structure of the H- bridge consists of four switches and separated dc source, it has several three levels (positive voltage (+Vdc), zero (0) and negative voltage (Vdc)) [9،10], when s1, s4 are turned on and s2, s3 are turned off the positive voltage is obtained during the first half cycle. When s2, s3 are turned on and s1, s4 are turned off the negative voltage is obtained during the second half cycle. If (s1 and s2) or (s3 and s4) are turned off the zero voltage is generated. This paper discusses the cascaded H- bridges inverter with separated dc sources. Different techniques SPWM and MSPWM are used to control the switches. These techniques are implemented by simulation and practically design. The block diagram of the system is shown in fig. 2.

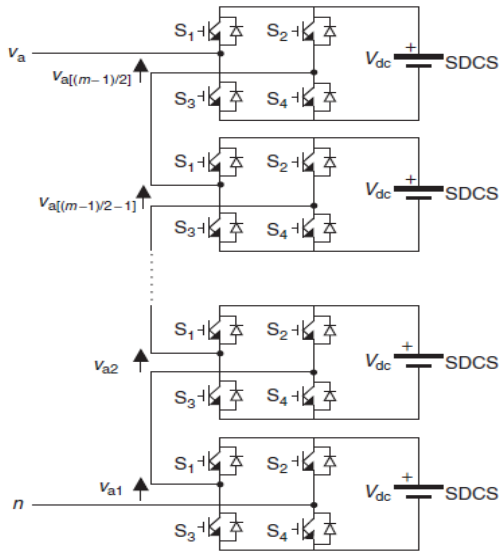


Fig. 1. General design of cascaded inverter [15]

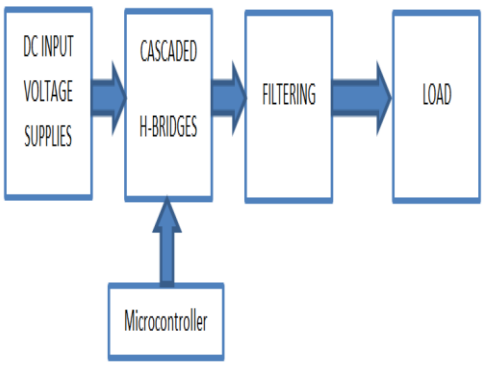
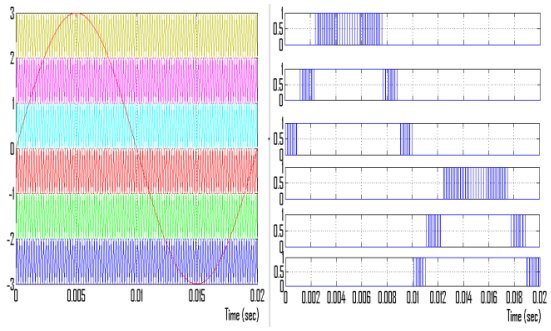


Fig. 2. The block diagram of proposed system

III. SPWM TECHNIQUE

The SPWM strategy is considered the most proper control used by searchers during the literature survey for multilevel inverter. In case of multilevel converter control, there should be one sine reference signal and multicarrier saw tooth waveforms. If number of levels is equal to (n), then the number of triangular waves is equal to (n-1). The pulsing signals are produced by comparing reference signal (sinusoidal waveform) with triangular carrier signals of frequency fc. Each triangular carrier wave is compared with sine reference signal. The power switch device is ON when a sinusoidal signal is larger than a triangular carrier wave attached with that switch. The frequency of a saw tooth waves identifies the switching frequency of the H-bridge converter and the harmonics in the output of multilevel converter [16]. The frequency of a sine modulation wave identifies the required fundamental frequency at the output of cascaded multilevel converter. The amplitude of sinusoidal signal varies the modulation index [17]. In this technique the amplitude of reference signal Ar is equal or less than the amplitude of triangular signals Ac as shown in fig. (3-a). The lowest order harmonics (LOH) and distortion factor (DF) are reduced in this technique. The pulses of seven levels are shown in fig. (3-b). The produced pulses for three, five and seven level are same. The pulses widths are varied to control ac voltage of inverter [18]. Full bridge (H-bridge) consists of four switches and dc supply, the comparison in term of number of switch and number of dc source for three, five and seven level is illustrated in table I. The output voltage before filter has high order harmonics but when converted to sinusoidal using discrete second orders filter the THD reduced significantly. The frequency of reference and carrier signal is 50Hz, 5KHz respectively. The system design of seven levels inverter is shown in fig. 4. The ac voltage and FFT spectrum for (three, five and seven levels) without and with filter are shown in (fig. 5, fig. 6 and fig. 7) respectively.



(a) (b)

Fig. 3. (a) The comparison between sine signal and triangle signals; (b) The produced pulses of SPWM technique seven levels inverter

TABLE I. The comparison between switches and dc sources for different level inverter

Number of levels	No. of dc sources	No. of switches
3	1	4
5	2	8
7	3	12

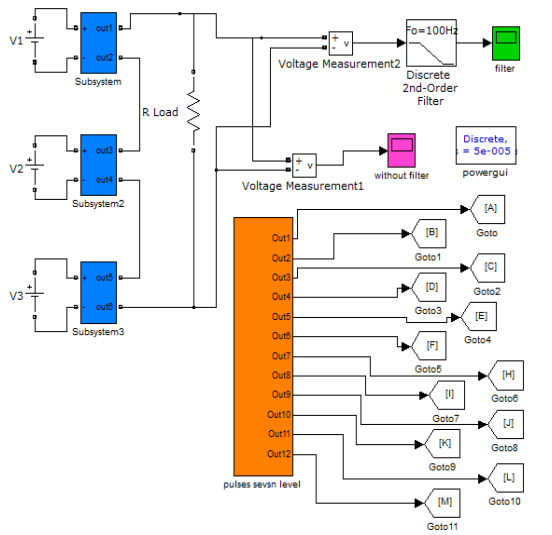
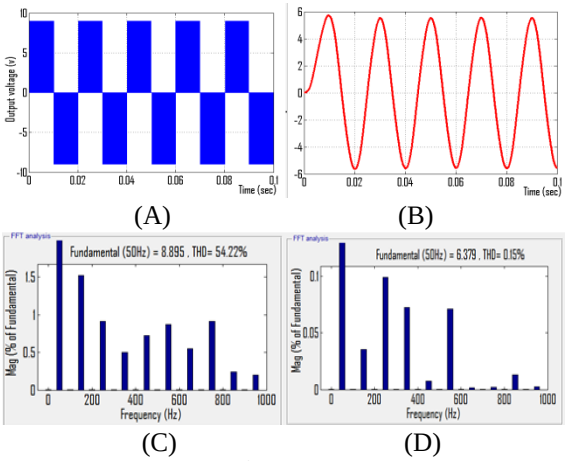


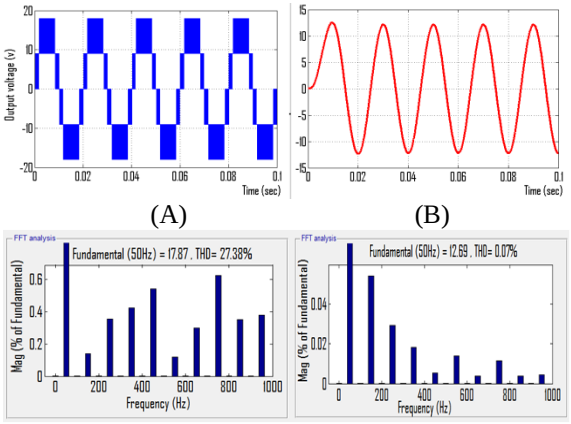
Fig. 4. The design of single phase seven level inverter



(A) (B)

(C) (D)

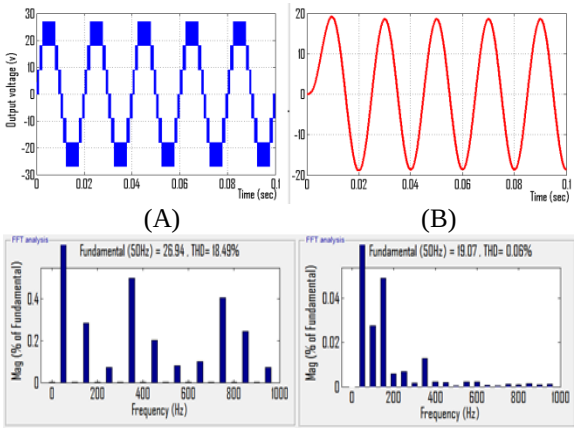
Fig. 5. AC voltage of SPWM three levels inverter in simulink/matlab: (A) without filter; (B) with filter; FFT analysis: (C) before filter (D) after filter



(A) (B)

(C) (D)

Fig. 6. AC voltage of SPWM five levels inverter in simulink/matlab: (A) without filter; (B) with filter; FFT analysis: (C) before filter (D) after filter



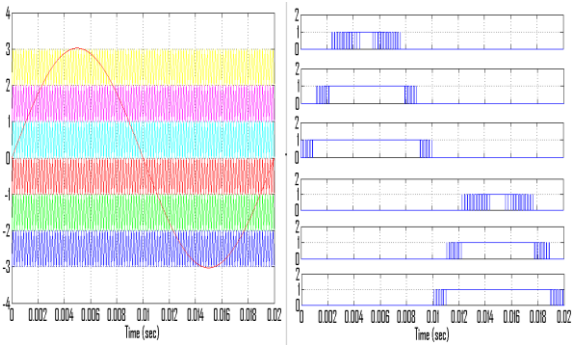
(A) (B)

Fig. 7. AC voltage of SPWM seven levels inverter in simulink/matlab: (A) without filter; (B) with filter; FFT analysis: (C) before filter (D) after filter

IV. MSPWM TECHNIQUE

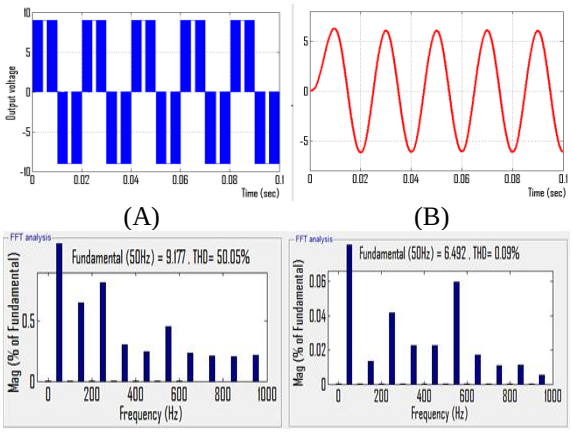
In SPWM technique, as the peak of sinusoidal signal arrives the amplitude of triangular signals the pulses widths do not vary significantly, because the amplitude of sine wave is equal or less than the amplitude of triangular signals, but in MSPWM technique the amplitude of sine wave is larger than the amplitude of multicarrier as shown in fig. (8-a). Each triangular signal is compared with sinusoidal wave. The semiconductor power switch is turn ON when sinusoidal reference wave is greater than triangular wave interconnected with that switch device and vice versa. The pulses are generated at output of converter depending on the amplitude and frequency of both triangular multicarrier waveforms and sine reference signal. The carrier frequency f_c of triangular signal is higher than the frequency f_r of sinusoidal reference wave. In this paper the frequency of saw tooth multicarrier waveforms and sine reference signal are (5KHz, 50Hz) respectively. The produced pulses of seven levels inverter are

shown in fig. (8-b). These gates pulses are applied for each bridge. The design used in this technique is same as design in SPWM which applied by simulink/matlab. For three, five and seven the output voltage and FFT spectrum before and after filter are shown in (fig. 9, fig. 10 and fig. 11) respectively. The fundamental frequency of output voltage converter is same of frequency of sine reference wave.



(A) (B)

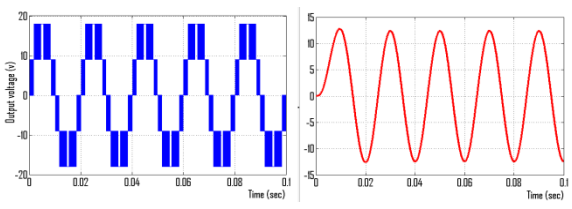
Fig. 8. (A) The comparison between sine signal and carrier signals; (B) The produced pulses of MSPWM technique seven levels inverter



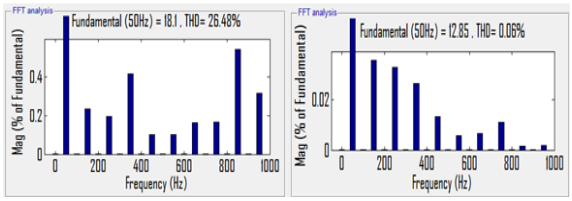
(A) (B)

(C) (D)

Fig. 9. The output voltage of MSPWM three levels inverter in simulink/matlab: (A) without filter; (B) with filter; the FFT analysis: (C) before filter (D) after filter

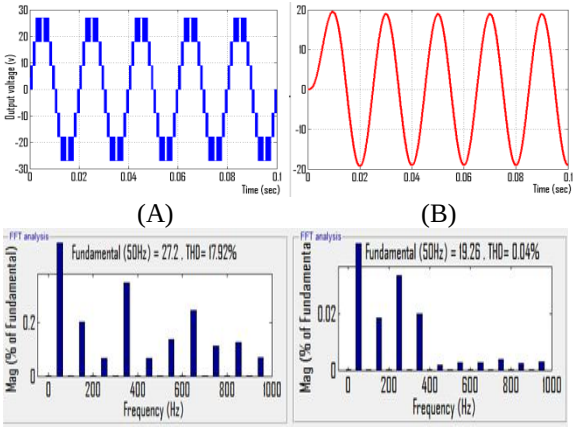


(A) (B)



(C) (D)

Fig. 10. The output voltage of MSPWM five levels inverter in simulink/matlab: (A) without filter; (B) with filter; the FFT analysis: (C) before filter (D) after filter



(A) (B)

(C) (D)

Fig. 11. The output voltage of MSPWM seven levels inverter in simulink/matlab: (A) without filter; (B) with filter; the FFT analysis: (C) before filter (D) after filter

V. PROTEUS AND HARDWARE

Proteus software application is introduced by developers of LABCENTER ELECTRONICS company, it is schematic circuit with ability to simulate not only normal digital and analog parameters, but also it can be implemented the programmable parameters like LCD displays and microcontrollers. It is very helpful tool in design presentations and PCB layout operation. In this paper the system consists of microcontroller (arduino mega), optocoupler, H-bridges drive (L298) and low pass filter. The simulated system in proteus is shown in fig. 12. The program is written in arduino software and compiles the program to hexadecimal then the hexadecimal file is sent to arduino board in proteus simulation design. Microcontroller can generate the high frequency PWM. The pulses produced by microcontroller are applied on zigzag side of each H-bridge for positive half cycle and turn it off for the negative half cycle and vice versa. The optocoupler used to separate the ground of arduino from the ground of L298 drive. Which the pulses applied for each bridge switches, are produced by microcontroller as shown in fig. 13. A second order passive filter is used in the output of cascaded H-bridges to convert the staircase PWM to

sine wave and eliminate harmonics. The equations used to calculate the inductance and capacitance for low pass filter is as following [19]:

$$L = \frac{R}{\pi f c} \quad (1)$$

$$c = \frac{1}{\pi f c R} \quad (2)$$

Where
L= inductance (H)
R= resistance (Ω)
C= capacitance (F)
f_c= cut-off frequency (HZ)

The complete circuit of hardware is shown in fig. 14. The output for seven levels implemented by proteus in SPWM and MSPWM strategies is shown in fig. 15. The experimental results using SPWM and MSPWM strategies are shown in (fig. 16, fig. 17) respectively

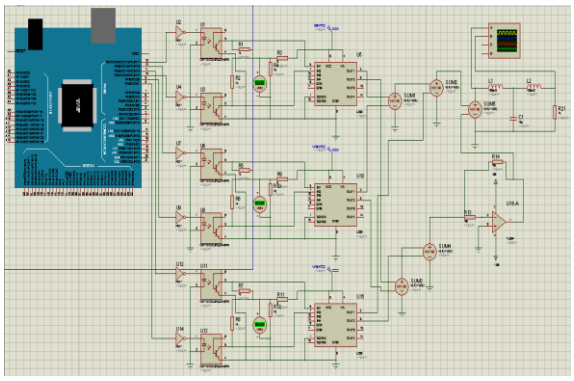
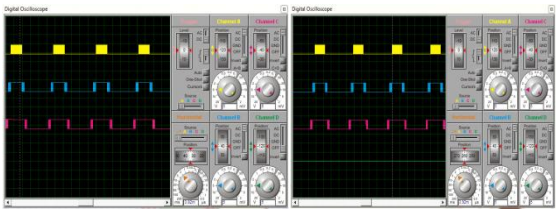


Fig. 12. The schematic of the system in proteus



(A) (B)

Fig. 13. The pulses produced: (A) positive half cycle; (B) negative half cycle

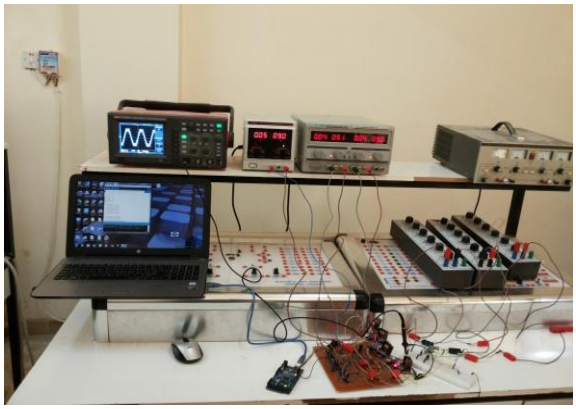
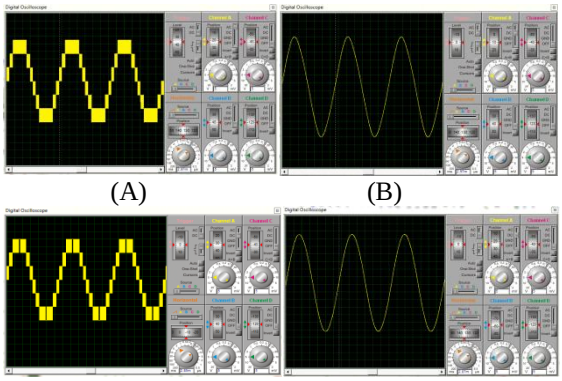


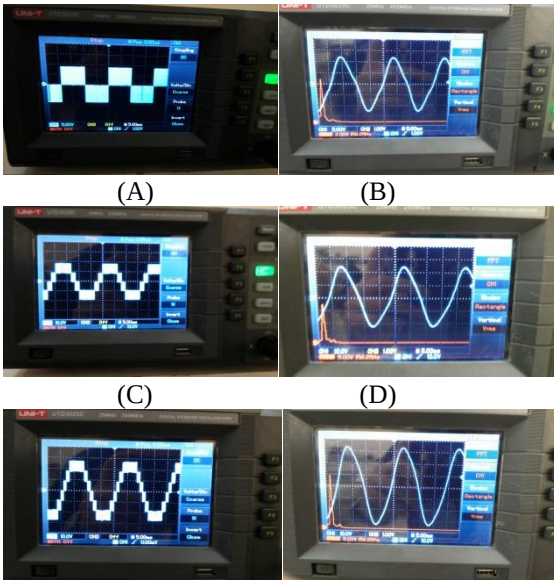
Fig. 14. The hardware proposed system



(A) (B)

(C) (D)

Fig. 15. The output voltage for seven levels by proteus: SPWM (A) without filter; (B) with filter; MSPWM (C) without filter (D) with filter

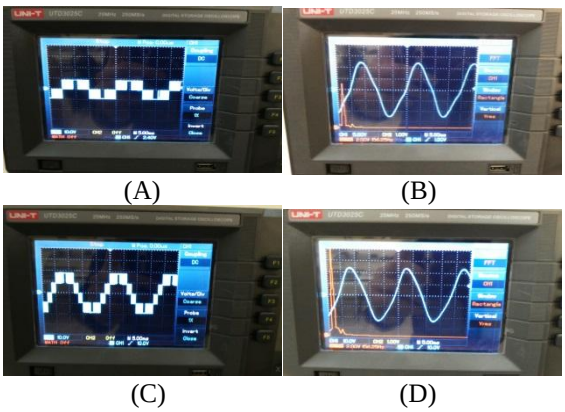


(A) (B)

(C) (D)

(E) (F)

Fig. 16. The hardware output voltage using SPWM: three level (A) without filter; (B) with filter and harmonics spectrum; five level (C) without filter; (D) with filter and harmonics spectrum; seven level (E) without filter; (F) with filter and harmonics spectrum



(A) (B)

(C) (D)

(E) (F)

Fig. 17. The hardware output voltage using MSPWM: three level (A) without filter; (B) with filter and harmonics spectrum; five level (C) without filter; (D) with filter and harmonics spectrum; seven level (E) without filter; (F) with filter and harmonics spectrum

VI. THE SOFTWARE ALGORITHM

The basic circuit of this system is an arduino microcontroller which is programmed for three, five and seven levels of SPWM and MSPWM to produce the required output voltage and reduce THD. The flowchart of the system is shown in fig. 18.

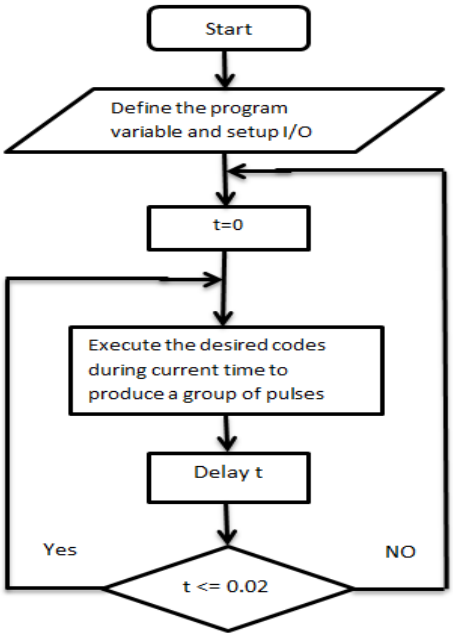


Fig. 18. The flowchart of the system

The algorithm contains the following steps:
1) Define the program variables and setup I/O
2) Read t=0
3) Execute the desired codes during current time to produce a group of pulses
4) Delay t
5) If t<= 0.02 then returns to step 3 else return to step2

TABLE II. The percentage values of THD before and after filter for different techniques used shown in below table:

Number of levels	SPWM technique		MSPWM technique	
	THD without filter	THD with filter	THD without filter	THD with filter
3	54.22%	0.15%	50.05%	0.09%
5	27.38%	0.07%	26.48%	0.06%
7	18.49%	0.06%	17.92%	0.04%

VII. CONCLUSION

The cascaded H-bridges inverter is design and implemented for three, five, seven levels using SPWM and MSPWM techniques. The results in term of THD before and after filter are compared as shown in table II. MSPWM technique as it clears from table II produces THD lower than SPWM. As the number of levels increases the THD is reduced for both techniques as it clears from the table II. The hardware achievement of both methods are designed and implemented practically.

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