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Minimum Mismatch of Current in Fully Differential Charge Pump for Integer N- DPLL

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ABSTRACT
Fully Differential ended charge pump (FDCP) are proven to have advantages over single ended charge pump at the cost of complexity and required more power for implementation for digital phase locked loop(DPLL). Wide swing cascodebias voltage with the rail to rail operational amplifier(opamp) as common mode feedback(CMFB) provides efficient solutions for current mismatch due to its non-idealities. The FDCP is simulated across process corners using 65nm technology with tsmc foundry for10Ghz DPLL. The power consumption of FDCP is 23mW with 100uA as Charge Pump (CP) current.
Key words: Fully Differential Charge Pump, Common mode feedback, rail to rail opamp, Digital Phase locked Loop, cascode bias

I. INTRODUCTION

Term lock signifies output frequency is same as input reference frequency with divider. Phase Frequency Detector (PFD) is primary block of DPLL which detects the edges of input and reference frequency and it results the two pulses UP and DN. The width of UP and DN decides amount of charging and discharging resulting the output voltage. For same width of UP and DN, amount of charge and discharge should be same. Series ON and OFF of the switches leads to charge in actual output voltage and also nonlinearity exists. In the entire DPLL loop output voltage of CP precisely generates corresponding frequency signal which is responsible for locking frequency. The deviation in the CP output voltage leads phase noise in the DPLL loop. Thus, design of CP is prominent. There are different situations through which the output voltage of CP can deviate from actual value. They are Unequal UP and DN currents, Charge sharing due to channel charge during switch ON to OFF and non-idealities because of continuous switching and timing of UP and DN. Proposed architecture is designed to achieve reduced mismatch current with less power consumption.

Different types of FDCP are discussed in literature [1]–[5].Replica charge pump is being adopted in literature [1] and Charge sharing is supressed in charge pump by current steering technique. Switch near to output voltage can't efficiently remove charge sharing even though voltage buffer is used. Rail to rail opamp is employed in literature [2] to give flexible swing of output voltage of charge pump. Constant gm is required in Rail to rail opamp to ensure stability in loop. Here author adopts replica technique to avoid channel length modulation. Current compensation and mismatch cancellation circuit is implemented in literature [3] to gain minimum current mismatch and its variation across output voltage range. Differential cross coupled current steering is employed in literature [4] which ensures high working speed with less current mismatch. Separate techniques for mismatch suppression and variation suppression are implemented in literature [5] to have same current for output voltage variations.

In this paper, fully differential charge pump is proposed for 10GhZ speed high performance digital phase locked loop. Section II explains being charge pump differential in nature, still current mismatch predominates the whole DPLL performance. Section III discussesthe proposed architecture of FDCEP. Section IV shows the results discussing across different factors. Section V For this work draws the conclusions.

II. FULLY DIFFERENTIAL CHARGE PUMP

The CP can be implemented either single ended and differential ended. In single ended block output voltage is measured with respect to ground where as in differential ended output is measured with respect to common mode voltage(V_{CM}).Differential ended architecture brings advantage of common mode noise voltage and increase in output voltage swing. Increased voltage range increases the VCO tuning range too[10]. Additionally, differential operation of CP ends the necessity to match between PMOS and NMOS networks. If they match between their networks that ensures the current matching in Differential CP. Also delay offset due to UP,UPB and DN,DNB will not major cause for jitter because of its fully symmetric architecture. The fully

differential DPLL requires two ON chip LPF in turn which will provide improved immunity to power and substrate noise.Disadvantage of fully differential CP is increased complexity and ensuring stability of two loop simulation for varying bandwidth till it locks to input frequency. General block diagram of fully differential block diagram is shown in Figure 1.

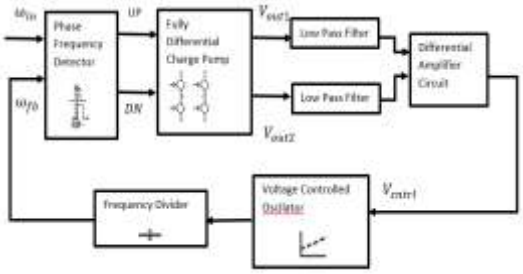

Figure 1. General block diagram of Fully differential DPLL

Implementation of fully differential charge pump is significant in high performance DPLL. The traditional implantation of FDCP is shown in Figure 2.

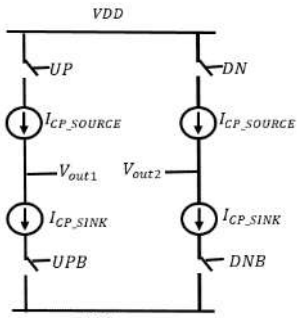

Figure 2. Functional block diagram of FDCP

The FDCP has complimentary input signals UP, UPBAR(UPB) and DN, DNBAR(DNB) corresponding for sink and source currents. It also has two output voltages which are equal and opposite in magnitude as V_{CP}^{+} and V_{CP}^{-}.Thus,the charge pump output voltages V_{CP}^{+} and V_{CP}^{-} is defined as equation 1.

$$V_{CP}^{+} = V_{CM} + \Delta V \quad \text{and} \quad V_{CP}^{-} = V_{CM} - \Delta V \qquad (1)$$

If V_{CM} changes, V_{CP}^{+} and V_{CP}^{-} also affected. So, any fully differential operation requires feedback to maintains same V_{CM} for both V_{CP}^{+} and V_{CP}^{-}. Mainly charge pump implementation has switches and current source. The PFD output signals are digital in nature. UP and DN pulses operate N and P type switches in charge pump such that V_{CP}^{+} and V_{CP}^{-} either charge/discharge or discharge/charge as in equation 2.

$$V_{CP} = \frac{Q}{C} \qquad (2)$$

The amount of charge/discharge is proportional to phase difference of reference and feedback signal from divider. Correspondingly locking time depends how accurate is this charge /discharge. The width of UP and DN pulses decides the amount of charge/discharge as shown in equations 3 and 4.

$$Q_{charge} = Q_{initial} + \int_0^{T_{UP}} I_{CP\_source}\,(t)dt \qquad (3)$$

$$Q_{discharge} = Q_{initial} + \int_0^{T_{DN}} I_{CP\_sink}\,dt \qquad (4)$$

Any variations of charge pump current I_{CP} for change in output voltage should be very minimal. Improper function of current in FDCP results increase in settling time or sometime it may become infinite loop to lock the input reference frequency. During DPLL lock, non- zero phase zero may lead to change charge pump output voltage means FDCP still suffers from non-idealities. It is very essential to have equations 5 and 6.

If $I_{UP1} = I_{UP2} = I_{CP\_source}$
and $I_{DN1} = I_{DN2} = I_{CP\_sink}$ (5)
Then $I_{CP\_source} = I_{CP\_sink} = I_{CP}$ (6)

Then any current mismatch in FDCP behaves as common mode offset. Thus, FDCP has great performance to produce less jitter in DPLL loop.

The FDCP performance is still made flexible by using rail to rail opamp. Rail to rail common mode range can be achieved by using P and N input differential pair.The implementation stages of rail to rail opamp is shown in Figure 3. Thus, the operation overlaps for mid voltage range. It changes the gm in circuit [7,9]. The stability of opamp depends on gm. P input differential pair works for initial voltages and N input differential pair works for later part of voltage. The mid-range of power supply voltage both differential pair works. For this range, it doubles the current in turn gm also. As change in gm directly effects the change in pole location, rail to rail opampshould be compensated by gm variations. Here in this paper maximum selection circuit method is adopted. It works on maximum/minimum current selection [7].

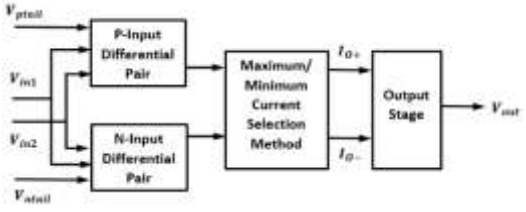

Figure 3.Implementation stages of rail to rail opamp

In this paper, architecture incorporates self-bias cascode design and efficient CMFB. Self-bias cascode design benefits to overcome the effects of channel length modulation and also stabilizes bias voltage in less time. Any changes in V_{CM}will be taken care by efficient CMFB.

III. PROPOSED FULLY DIFFERENTIAL CHARGE PUMP

The architecture of fully differential charge pump exhibits in three parts. Such as DCP1 and DCP2, wide swing cascode current source with start-upand constant gm compensated rail to rail opamp[9]. Figure 4 shows the schematic design of proposed FDCP.

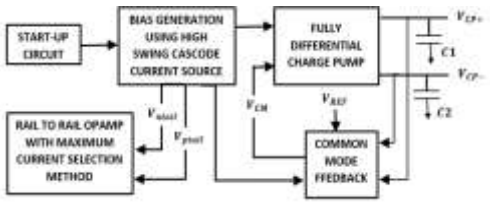

Figure 4. Implementation diagram of proposed FDCP

Minimum current mismatch can be achieved through replica current path, stabilized bias voltages and high output resistance of UP and DN current sources. Proposed FDCP is shown in Figure 5. Segments 1 and 2 are the replica branches for V_{CP}^{+} and V_{CP}^{-}. MS series transistors provide start up circuit for cascode bias as shown in Figure 7. Biasing is provided by MB series transistors. Single bias structure is adopted in FDCP where in required. This avoids error due to different settling time of bias voltages. The M5 – M8 are DN bias transistor. The UP bias is maintained through an output of opamp. When the switch UP is OFF, opamp A1 pulls V1 to have same gate voltage for UP Network. V_{CP}^{+}will not suffer from charge sharing and charge injection. DCP1 and DCP2 are supported by replica current branch. When switch turns ON to OFF or OFF to ON opamps A1 and A2 replicates the V_{CP}^{+} and V_{CP}^{-} through other path *V1 – VGP*. Incremental delta change reflects on replica branch. Switches MUP1, MUP2 and MDN1, MDN2 are place away from output point. It directly avoids charge sharing. The V_{CP}^{+} and V_{CP}^{-} either charges/discharges depending on UP and DN signals switching. The implementation of PFD is shown in Figure 6.

Same Common mode voltage for DCP1 and DCP2 is maintained by using CMFB circuit as shown in Figure 5 by resistor R1, R2 and opamp A3. The FDCP output voltages are compared with vref. CMFB output changes the current of DN network in main branch. Increase in VCM values it decreases DN current, in turn UP current. The design is simulated in cadence tool with 65nm technology and able to achieve 2% of current mismatch measured across corners.

IV. SIMULATION RESULTS

Maximum or constant gm is achieved in rail to rail opamp using maximum/minimum current selection method. The results are tabulated in table 2.The overlap region between NMOS and PMOS inputdifferential makes maximum 5% gm variation across the corners.

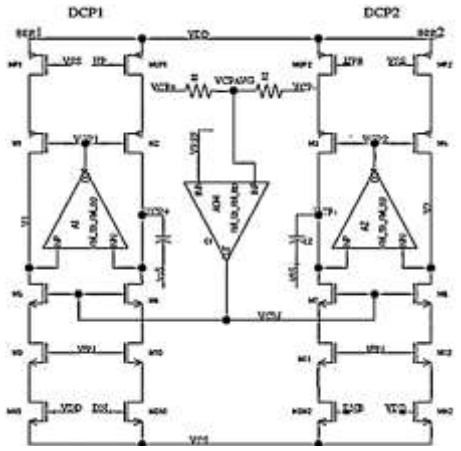

Figure 5. Proposed implementation of FDCP

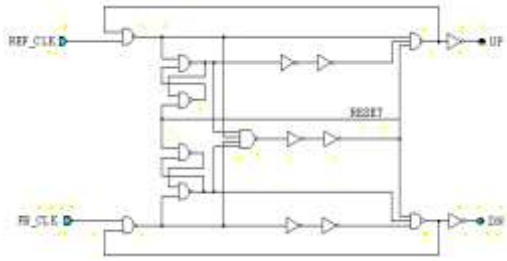

Figure 6. Schematic of PFD with reset delay

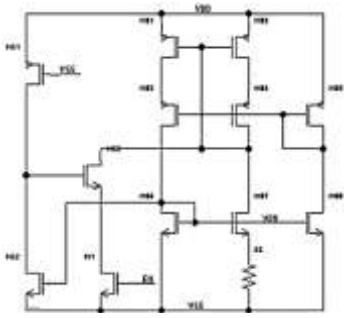

Figure 7. Wide swing cascode bias with start-up circuit

The rail to rail opamp output connects to PMOS, thus the careful simulation required to set the values of transistor. This impacts the clock feedthrough and

slew rate of opamp. The gain of opamp is 105dB is sufficient to reduce offset voltage.

Current mismatch of UP and DN current across out voltage variations are shown in Figure 9. Through this paper, it would be able achieve highest 2% of current variation with output voltage variations 0 to 1.8V across all corners.Fully differential CP is implemented in DPLL loop archives results is shown in Figure 10. It is observed the output voltage V_{cntrl} is varying for different width of UP and DN.When input frequency is equal to feedback frequency the width of UP and DN pulses are observed constant. While PLL clocked the width of pulses should be such that FDCP reacts, otherwise dead zone occurs between PFD and FDCP.Here it careful designed to avoid dead zone. Sufficient delay will be given in the reset path of PFD as shown in Figure 6.

Table1.Results of rail to rail opampwith level shift

Process	Tsmc 65nm
Power supply	1.8V
DC Gain	105dB
Gain Bandwidth Product	8 MHz
Phase Margin (PM)	85 deg
Input common mode range (CMR)	rail to rail
Power dissipation	< 1mW
Gm (µA/V)	±5%
Slew rate	15uV/s

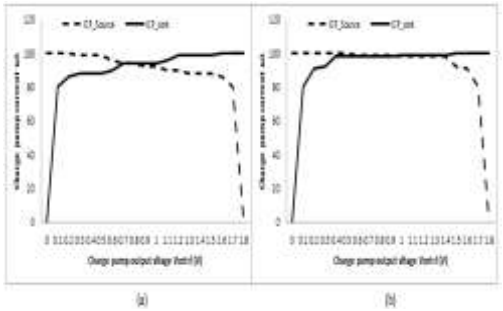

Figure 9. Charge pump current matching

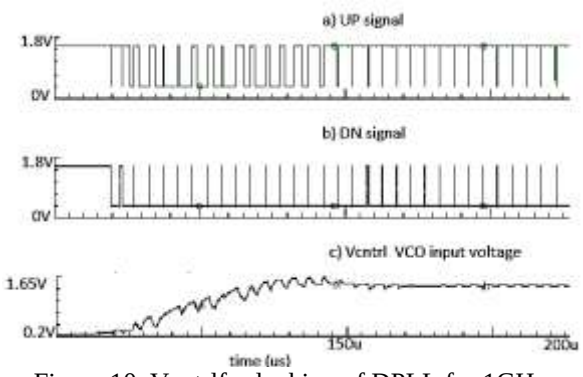

Figure 10. Vcntrlfor locking of DPLL for 1GHz

V. CONCLUSION

Fully differential CP has many advantages over single ended CP may be at the cost of increased complexity and area, more current. FDCP architecture is proposed and achieves 2% current mismatch with 100uA as CP current. It is simulated with tsmc 65nm, 1.8V across corners. Charge sharing, charge injection and Clock – feedthrough is efficiently taken care to reduce the jitter in Integer N DPLL loop. FDCP consumes 23mW as total power. Reducing dead zone range between PFD and FDCP and also with minimum current mismatch, the overall jitter in integer N DPLL can be reduced to great extent.

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