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An Optimal Design of UP-DOWN Counter as SAR Logic Based ADC using CMOS 45nm Technology

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ABSTRACT
In this paper an analog to digital converter architecture is introduced. The proposed design is based on Up-Down counter approach SAR type ADC. This design offers less design complexity which leads to low power consumption. Based on the proposed idea, a 4-bit ADC is simulated in Microwind 3.5 environment using 45nm CMOS technology with supply voltage of 1 V. The ADC is designed with control signal like Start of conversion (SOC) and End of conversion (EOC). The ADC design consumes 3.2mW of power. The proposed ADC design is optimized to area of 829.6µm2.

Keywords - Analog-digital conversion (ADC), SAR, Up-Down counter, Microwind 3.5

I. INTRODUCTION

ADC is an integral design block in modern digital communication system. With the continuous advancement of CMOS technology, the need for low complexity, low-power and high-speed analog-to-digital converters has increased [1].

Nowadays, VLSI designs are implemented with more and more functions on the chip. Along the same, with an increasing trend to a system-on-chip, in order to achieve low manufacturing cost, an ADC has to be implemented in a low-voltage submicron CMOS technology [2]. So we have proposed low power ADC. From different ADC architectures available SAR based ADC is having many advantages over the different types of ADC architecture [1]. SAR based ADC can be design in many ways. This paper proposed Up-Down counter as a SAR logic. This proposed structure also have various advantages over the regular SAR design methodologies. The Up-Down counter as a SAR logic is best suitable for low power application.

The paper is organized as follows. In section II, overview of SAR based ADC is described. Section III and IV describes proposed design of parts of ADC system and performance analysis. Finally section V concludes the paper.

II. PROPOSED ADC ARCHITECTURE

The SAR algorithm works by switching on a large voltage and comparing that to the input voltage. If the switched voltage proves higher than the input voltage then the algorithm turns off that voltage and turns on a voltage half that size and repeats. If the voltage comes up lower than the input voltage it keeps that voltage on and then adds a voltage that represents half the size of the first voltage and repeats. This then corresponds to a series of 1s and 0s. These values are known as bits with the first voltage that is turned on corresponding to the most significant bit (or MSB) and the last voltage corresponding to the least significant bit (or LSB). When the algorithm finishes the result is a binary code that corresponds to the input voltage. This process is referred to as successive approximation [3].

The architecture of a successive approximation ADC is shown in Figure 1. The SAR based ADC is basically based in the concept of a binary search algorithm to determine the closest digital code for an input signal. The analog input signal that to be converter is applied to the structure through the sample and hold circuit to the comparator. The comparator simply tells whether the input signal is greater or smaller than the DAC output and gives one digital bit at a time starting from the MSB [3].

The SAR stores the produced digital bit and uses the information to alter the DAC output for the next

comparison. In order to achieve N-bit resolutions, a successive approximation ADC needs N clock cycles. As the performance is limited by DAC linearity, the calibration of the DAC is required to gain high resolution [4].

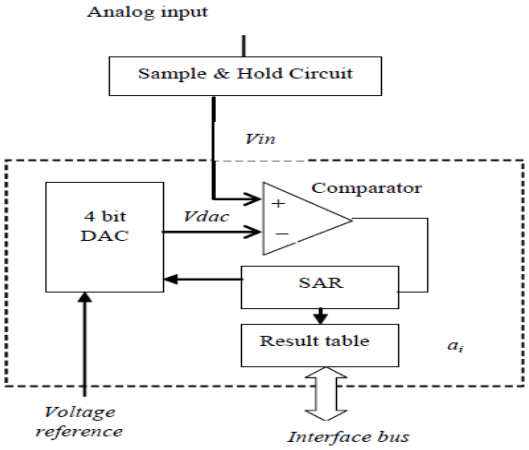

Figure 1: Architecture of SAR based ADC

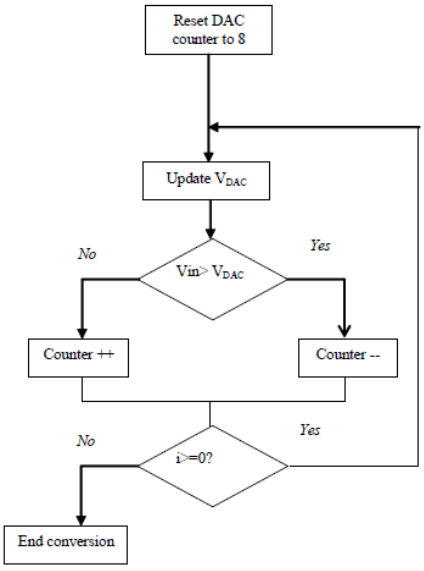

Figure 2: Iterative converter algorithm and a simple implementation with up/down counter

The complete process is faster than the iterative converter as only N comparisons are necessary. The algorithm is showed in detailed in figure 2.
The proposed Up-Down counter based SAR ADC is basically consists of four different parts as;

A. Sample and Hold circuit
B. Voltage Comparator
C. Up-Down counter as SAR logic
D. DAC

A. Sample and Hold circuit:

The input signal in the proposed ADC structure is provided to the sample and Hold circuit. It samples analog input signal & holds value between clock cycles. Sample and hold circuit provides the stable input which is the most important parameter for the ADC topology. The physical design of sample and hold circuit is as shown in figure 3.

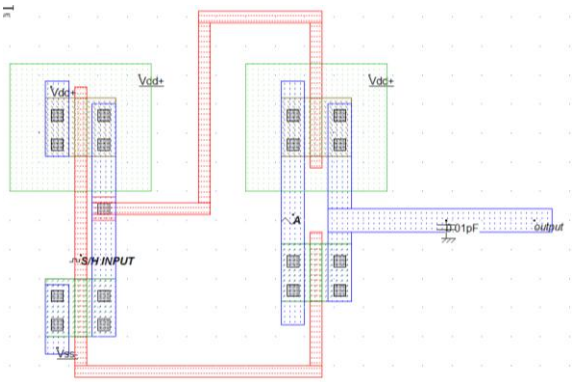

Figure 3: Physical layout design of SnH structure

The structure is designed with a combination of an inverter with transmission gate on the output side. The capacitor value have to be decided depending on the restoring logic of the input signal. The simulation result for the input as a sine wave is shown in figure below.

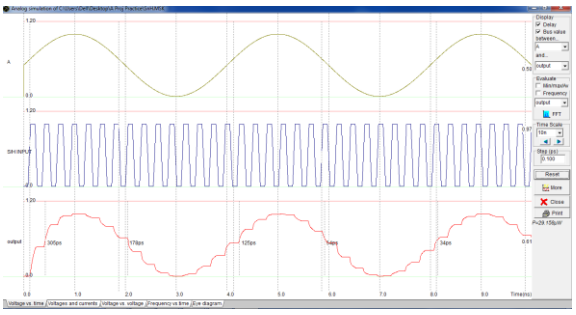

Figure 4: Simulation result of SnH cicuit

B. Digital Comparator
Comparator is the important design sub block of the ADC. The sampled output from the sample and hold circuit is provided to the comparator structure to determine the digital equivalent of the analog signal and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison.

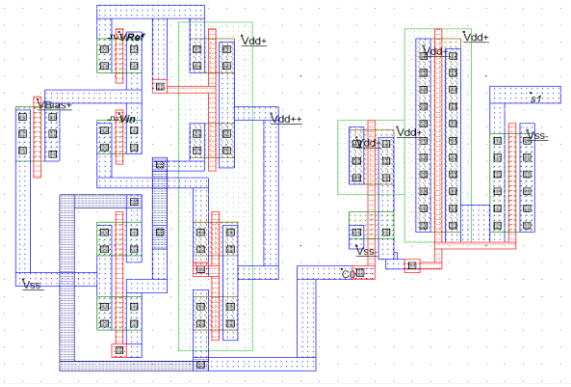

Figure 5: Physical design layout of Comparator

For a given design of the comparator, when
Vref > Vin ; the structure outs as logic 1 and for
Vref < Vin ; the structure outs as logic 0

The simulation result for the input Vref as input with some delayed clock and Vin as random clock is shown in figure below.

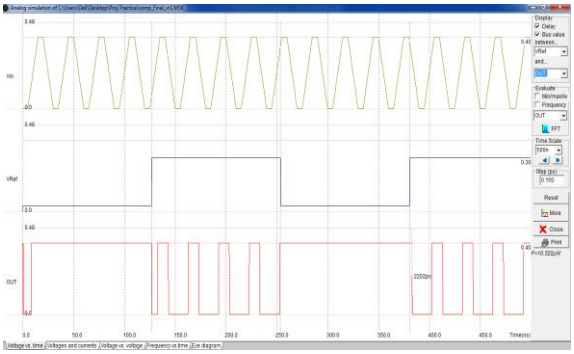

Figure 6: Simulation result of Comparator

C. Up-Dow Counter as SAR logic

The proposed work is basically focused on the construction of the SAR logic by designing the Up-Down counter. We design the SAR counter logic by simplest method, an Up/Down counter to control DAC o/p.

It works by starting by binary o/p 8(1000), and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments.

The counter o/p and Vin is compared using comparator which gives the value of that count directly. The comparison is performed for the next count, and so on until all count are checked for below or greater than value 8.

The conversion would start with SOC signal and cycle finishes after 8 clock cycles, with active low EOC output

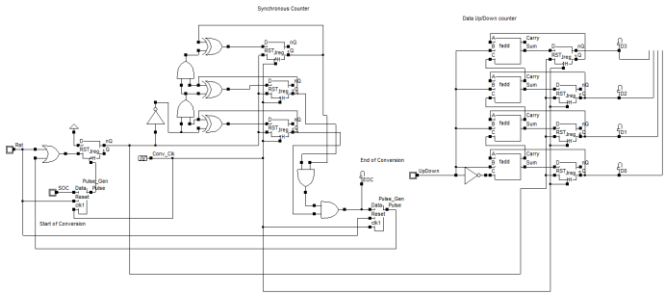

Figure 7: Logical Schematic design of SAR

The counter increments or decrements on the comparator input, it would start only with a pulse signal as Start of Conversion (SOC), lasting at least one clock cycle.

If the Comparator is '0', then the O/P would be 15 (1111), and if the comparator is '1' all the time then the o/p would be 1 (0001).

The conversion end with EOC (end of conversion) signal, going active low to indicate end of conversion and also load counter value to the o/p port.

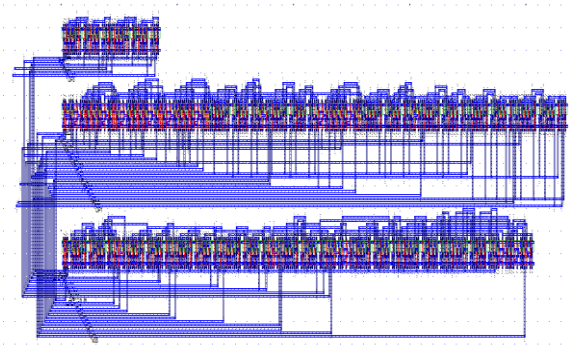

Figure 8: Physical design of SAR logic

D. Digital to analog converter

DAC is designed by using R-2R ladder network. The resolution of R-2R based DAC is based on the accuracy of the resistors and resistance of switches which must be low to minimize the voltage drop and associated non-linearity. 'Fig 9' shows MOS based layout of 4-bit R-2R DAC. Resistors are designed by using polysilicon material, due to it has high resistivity. The resistor R has a fixed value of 500 ohm.[5]

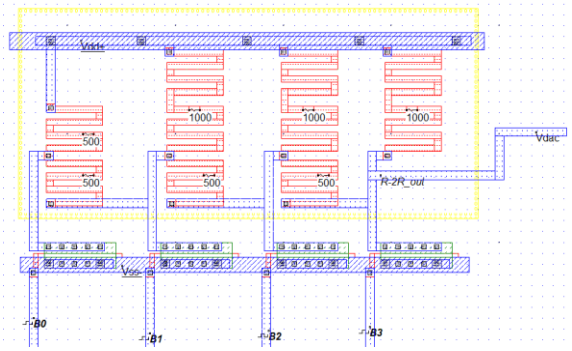

Figure 9: Physical design of DAC

The table below provided the analog output values that we are getting form the simulation v/s the theoretical values.

Table I: Analog output values for DAC

Digital Inputs				Analog Output Values	
B3	**B2**	**B1**	**B0**	**Theoretical**	**Practical**
0	0	0	0	1	1
0	0	0	1	0.9325	0.92
0	0	1	0	0.875	0.84
0	0	1	1	0.812	0.79
0	1	0	0	0.75	0.70
0	1	0	1	0.68	0.64
0	1	1	0	0.62	0.60
0	1	1	1	0.56	0.56
1	0	0	0	0.50	0.44
1	0	0	1	0.43	0.40
1	0	1	0	0.37	0.35
1	0	1	1	0.31	0.33
1	1	0	0	0.25	0.29
1	1	0	1	0.18	0.26
1	1	1	0	0.125	0.24
1	1	1	1	0.0625	0.23

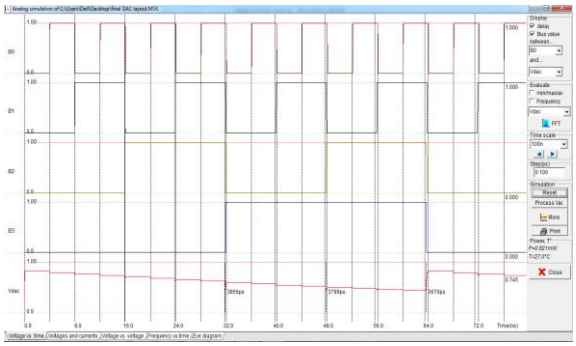

Figure10: Simulation result of DAC

III. IMPLEMENTATION OF ADC:

Physical layout of the proposed ADC architecture is done with the EDA tool microwind with 45 nm technology.

Now we are having layout design of all required four blocks that we need to design ADC. These four blocks we need to arrange as shown in “fig 11”.

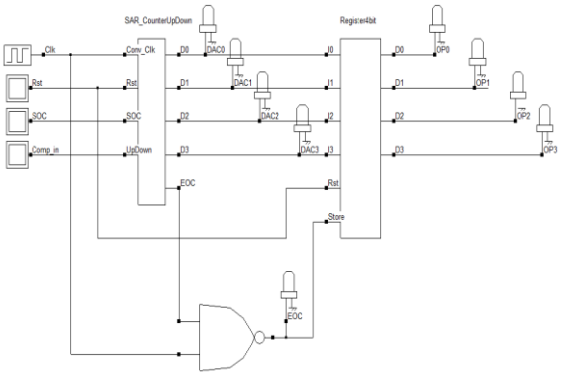

Figure 11: Schematic design of ADC

Figure 11, gives the overall view of SAR Based ADC when integrated together with different components of the block diagram for SAR ADC.

It integrates the building blocks like SAR counter and O/P register.
The counter increments or decrements on the comparator input, it would start only with a pulse signal as Start of Conversion (SOC), lasting atleast one clock cycle.

If the Comparator is ‘0’, then the O/P would be 15 (1111), and if the comparator is ‘1’ all the time then the o/p would be 1 (0001).

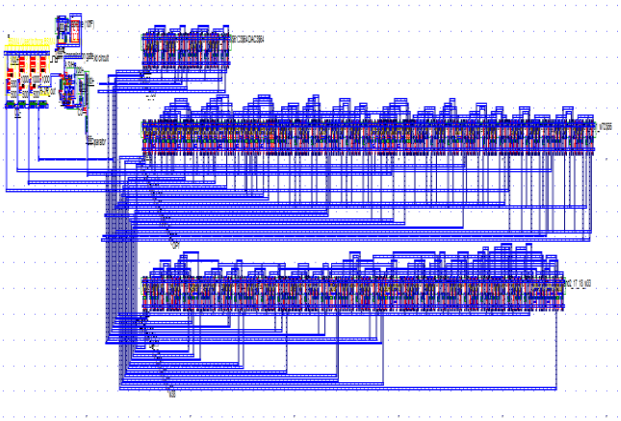

Figure 12: Physical design of SAR based ADC

Physical design parameters for ADC:
Width: 56.9µm
Height: 14.6µm
Surf: 829.6µm2
Electrical nodes: 234
NMOS devices: 235
PMOS devices: 198

IV. PERFORMANCE ANALYSIS

For simulation here are the details
Analog input signal (A_in) : sine wave with 1000 MHz of frequency.
SnH clock: logical delayed clock
System clock= 500 MHz
Vout= Output signal

TABLE II . ADC Output Table

Analog Vtg Input	ADC o/p	Decimal Values
0.0V	1111	15
0.1V	1111	15
0.2V	1111	15
0.25V	1101	13
0.32V	1011	11
0.4V	0111	7
0.5V	0100	4
0.6V	0011	3
0.7V	0010	2
0.75V	0011	2
0.8V	0001	1
0.87V	0001	1
0.9V	0001	1
1.0V	0001	1

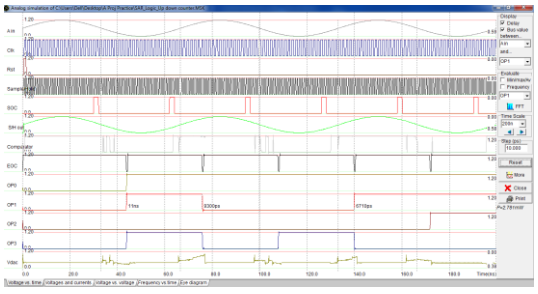

Figure 13: Simulation result of ADC

V. CONCLUSION

This paper presents the physical design implementation and simulation of ADC system. In this paper, low power and high speed SAR ADC is proposed and designed in 45 nm CMOS technology. We presented high speed/performance and typically low power consumption design of Successive Approximation Logic for ADC and by using the same we designed ADC architecture whose speed of operation is nearly doubled with more output stability.
At last, we club up all the working modules of the SAR based ADC is designed in 45nm CMOS technology with 4 bit resolution. It consumes different power values for the various range of input variations, as for triangular waveform as input, it consumes, 3.2mW of power for running simulation for 200nsec.

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