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Design and Implementation of Area Optimized, Low Complexity CMOS 32nm Technology Based NCO

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ABSTRACT
A numerically controlled oscillator (NCO) is a digital signal generator which is a very important block in many Digital Communication Systems such as Software Defined Radios, Digital Radio set and Modems, Down/Up converters for Cellular and PCS base stations etc. NCO creates a synchronous, discrete-time, discrete-valued representation of a sinusoidal waveform. This paper implements the development and design of CMOS look up Table based numerically controlled oscillator which improves the performance, reduces the power & area requirement. The design is implemented with CMOS 32 nm Technology with Microwind 3.8 software tool. In addition, it can be used for analog circuit also enables the integration of complete system on chip. This paper also describes the design of a NCO which is of contemporary nature with reasonable speed, resolution and linearity with lower power, low area. For all about Pre Layout simulation has been realized using 32nm CMOS process Technology.

***Keywords* :** Numerically Controlled Oscillator, LUT, Microwind 3.8

I. INTRODUCTION

In VLSI design, more and more functions are get added while designing a chip. To achieve the highest working parameters, the number of transistor are increases which increase the complexity and hence the die size required for the system also get increases [1]. For generating the real valued sinusoidal waveforms, the common method is to design the NCO with look up table based scheme. In LUT based scheme, signal generator such as NCO, generated signal through a unique memory access and clocking mechanism. LUT based NCO stores a large number of points for single cycle of periodic waveform in memory [2].

The proposed NCO have the option works for the two operating frequency of the output sine wave and we can set the Frequency select word as per the requirement of the output frequency.

The paper is organized as follows. In section II, overview of LUT based NCO is described. Section III and IV describes implementation of parts of NCO system and simulation result. And finally section V concludes the paper.

II. NCO OVERVIEW

A. NCO architecture

Simply, NCO is constructed by designing LUT with sample of sine values are stored in it. "Figure 1" shows the logic schematic of NCO. The NCO system has two inputs, frequency select word (FSW) and system clock. The value of FSW determines the sine wave frequency produced by NCO. The frequency of output signal produced by N-bit NCO is given by;

$$Fout = K * \frac{Fclk}{2^N}$$

Where K is the FSW, N is number of bits and FCLK is system clock [3].

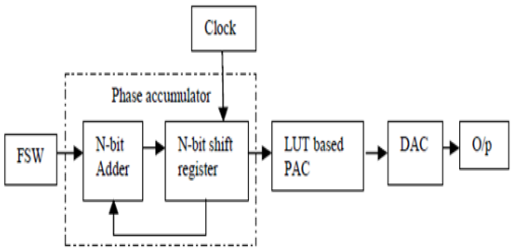

Figure 1: Logic schematic of NCO

Basically as per as the block diagram of the NCO design, it typically consist of a phase accumulator, phase-to-amplitude converter and Digital to analog converter [3].

A. Phase Accumulator which adds to the value held at its output a frequency control value at each clock sample [3].

B. A phase-to-amplitude converter, which uses the phase accumulator output word (phase word) as an index into a waveform look-up table to provide a corresponding amplitude sample [3].

C. Digital to analog converter, which converts discrete time, discrete value output of PAC into equivalent analog waveform [4].

A. Phase Accumulator:

A phase accumulator circuit is the basic building block of NCO which adds to the value held at its output a frequency control value at each clock sample.

In a simple word, it is a digital circuit which is act as counter. Output of phase accumulator is act as pointer, which index into waveform lookup table to provide corresponding output sample. Phase accumulator is collection of components that allows NCO to output at precise frequencies. A binary phase accumulator consists of an N-bit binary adder and N-bit register connected as shown in "Figure [2]". At each clock cycle phase accumulator produces a new N-bit output which consist of addition of the previous output obtained from the register with the digital input provided as frequency select word (FCW) which is constant for a given output frequency.

B. Phase to amplitude converter

PAC uses the phase accumulator output word (phase word) as an index into a waveform look-up table to provide a corresponding amplitude sample.

PAC is based on the lookup table. The PAC can be a simple read only memory containing contiguous samples of the desired output waveform which typically is a sinusoid. For the expected output waveform, the output of the phase accumulator points to the needed waveform sample address in the lookup table [2]. The lookup table then provides the digital word at the provided memory address, which is the digital word of the correct amplitude and phase for the DAC to produce.

C. Digital to analog converter

DAC converts discrete time, discrete value output of PAC into equivalent analog waveform [4].

III. IMPLEMENTATION OF NCO:

Physical layout of the proposed NCO architecture is done with the EDA tool microwind with 32 nm Technology.

A. Phase accumulator

4-bit phase accumulator contains back to back connection of 4-bit adder and shift register as shown in "Figure [2]". 4-bit adder is designed by cascading four, 1-bit full adder. 1-bit full adder is designed by using NAND gates. Same like, 4-bit shift register is designed by connecting four, 1-bit shift register. 1-bit shift register is designed by using one D flip-flop. Such 4 D flip-flops are connected in parallel in parallel out (PIPO) configuration [3]. These four D flip-flops are synchronized by clock and reset.

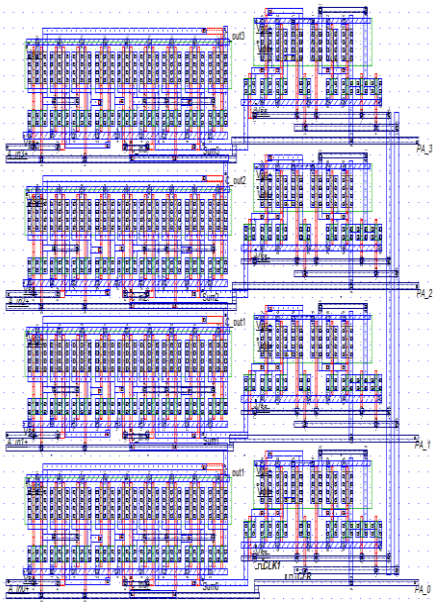

Figure 2: Physical design of the phase accumulator

Physical Parameter:
Width: 4.6µm (253 lambda)
Height: 6.5µm (361 lambda)
Surf: 29.6µm2 (0.0 mm2)

B. Phase to Amplitude Converter:

NCO system is of 4-bit, so PAC can be designed such that it can store 16 samples. PAC can be designed by connecting four, 4x1 LUTs. " One 4x1 LUT is designed by connecting 16-bit shift register and 16:1 multiplexer in series, as shown in Figure[3].

Here, 16-bit shift register is operating in serial in-parallel out (SIPO) mode. This shift register is act as memory element which stores 16 samples of sine wave. The values stored in these 16 memory location is accessed by using 16:1 multiplexer.

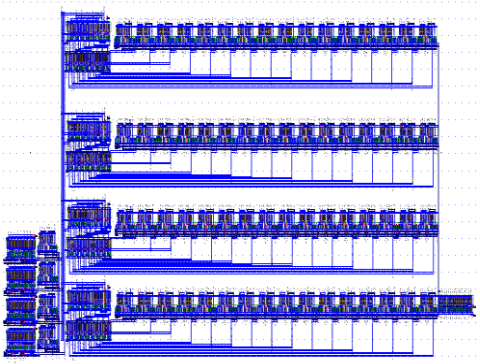

Figure 3: Physical design of 4X4 LUT based PAC

Physical Parameter:
Width: 61.8µm (3434 lambda)
Height: 18.3µm (1019 lambda)
Surf:1133.8µm2 (0.0 mm2)

C. Digital to Analog Converter:

DAC is designed by using R-2R ladder network. The resolution of R-2R based DAC is based on the accuracy of the resistors and resistance of switches which must be low to minimize the voltage drop and associated non-linearity. Resistors are designed by using polysilicon material, due to it has high resistivity. The resistor R has a fixed value of 500 ohm [4]. Physical layout design shown in Figure [4].

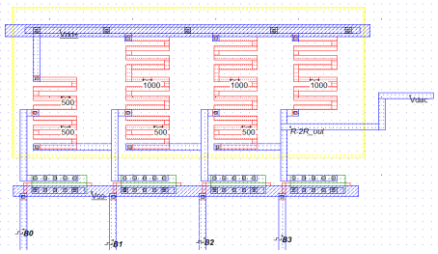

Figure 4: Physical design of DAC

Physical Parameter:
Width: 4.6µm (258 lambda)
Height: 3.2µm (176 lambda)
Surf: 14.7µm2 (0.0 mm2)

D. NCO (Numerically controlled oscillator)

Now we are having layout design of all required three blocks that we need to design NCO. These three blocks are arranged as shown in "Figure [5]" for realization of NCO. "Figure [6]" shows MOS base layout of NCO system.

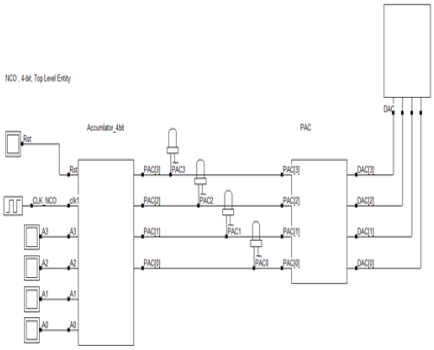

Figure 5: Schematic design of NCO

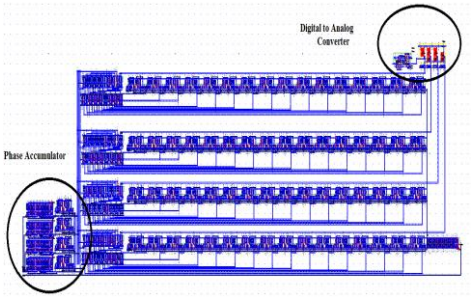

Figure 6: Physical design of NCO

Physical layout design parameter of NCO
Width: 62.1µm (3450 lambda)
Height: 21.1µm (1172 lambda)
Surf:1310.1µm2 (0.0 mm2)
No.of Electrical nodes: 728
NMOS devices: 765
PMOS devices: 625
Power dissipation: 1.409 mW

IV. SIMULATION AND RESULT

For simulation here are the details
System clock= 500 MHz
FSW input= 1 for 100ns & 2 for next 100ns
N=4
V_out= Output signal
By using (1) output frequency can be calculated

1. For FSW= 1

Fout (theoretical) = (FSW*FCLK)/ 2N
= (1*500MHz)/16
= 31.25 MHz

2. For FSW= 2

Fout (theoretical) = (FSW*FCLK)/ 2N
= (2*500MHz)/16
= 62.25MHz

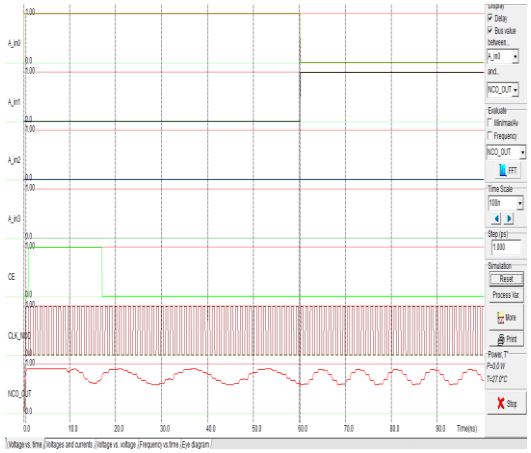

Figure 7: Simulation result of NCO

"Table [1]" shows the simulated output signal using simulation tool Microwind 3.8. In simulation we have two output frequencies 31MHz for FSW=1 and 62MHz for FSW=2 which are measured using cursor. "TABLE I" compares theoretical and simulated output frequencies.

TABLE I. Comparison of theoretical and practical output frequencies

Sr No.	FSW input (A3-A0)	Theoretical output frequency	Practical output frequency
1	1 (0001)	31.25MHz	31MHz
2	2(0010)	62.25MHz	62MHz

V. CONCLUSION

This paper presents the physical design implementation and simulation of NCO system. The designed system provides the sinusoidal wave as output. The output amplitude and frequency is dependent on the FSW provided and the number of

bit the system is designed for. The proposed design provides the optimized parameters like area, power and speed. Here 4-bit NCO is implemented which generates two output frequencies for two different FSW inputs.

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