

## Dynamic Power Reduction of Digital Circuits by Clock Gating

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### ABSTRACT

In this paper we have presented clock gating process for low power VLSI (very large scale integration) circuit design. Clock gating is one of the most quite often used systems in RTL to shrink dynamic power consumption without affecting the performance of the design. One process involves inserting gating requisites in the RTL, which the synthesis tool translates to clock gating cells in the clock-path of a register bank. This helps to diminish the switching activity on the clock network, thereby decreasing dynamic power consumption within the design. Due to the fact the translation accomplished via the synthesis tool is solely combinational; it is referred to as combinational clock gating. This transformation does not alter the behavior of the register being gated.

**Keywords:** Clock Gating, Low Power Design, MUX

### I. INTRODUCTION

Reducing power consumption in very large scale integrated circuits (VLSI) design has become an interesting research area. Most of the movable devices available in the market are battery driven. Battery operating devices impose tight constraint on the power dissipation. Reducing power consumption in such devices improves battery life significantly. Due to lesser development in battery technology, low power design has become more interesting research area. Power consumed in a digital circuit is of two types. Static and dynamic power. Static power appear in circuit due to leakage of currents whereas dynamic power consists of short circuit power and capacitive switching power. In VLSI circuit clock signal is used for the synchronization of active components. Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power consumption is a substantial component of total power dissipation in a digital circuit [4]. Clock-gating is a well-known technique to reduce clock power in give circuit. In a sequential circuit individual blocks usage depends on application, not all the blocks are used simultaneously, giving rise to dynamic power reduction opportunity. By clock gating technique, clock to a non idle portion of circuit is enable, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [3]. Local clocks that are enabled using conditionally are called gated clocks, because a signal from the environment is used to

gate the global clock signal [2]. Average power dissipated in a digital circuit is given as

$$P_{\text{average}} = P_{\text{dynamic}} + P_{\text{short-circuit}} + P_{\text{leakage}} + P_{\text{static}}$$

$P_{\text{average}}$  is the average power dissipation,  $P_{\text{dynamic}}$  is the dynamic power dissipation due to switching of transistors,  $P_{\text{short-circuit}}$  is the short-circuit current power dissipation when there is a direct current path from power supply down to ground,  $P_{\text{leakage}}$  is the power dissipation due to leakage currents,  $P_{\text{static}}$  and is the static power dissipation.

**Power consumed in digital circuits is given below.**

1. Static power
2. Dynamic power.

#### 1. Static Power

Static power is the power dissipated by a gate when it is inactive or idle. Ideally, CMOS (Complementary Metal Oxide Semiconductor) circuits dissipate no power since in the steady state there is no direct path from Vdd to ground.

#### 2. Dynamic Power

Dynamic power is the power dissipated during active state due to switching activity of input signal. In other words, dynamic power dissipation is caused by the charging and discharging. Dynamic power dissipation in a circuit is given as

$$PD = \alpha C_L VDD^2 f$$

Where  $\alpha$  is the switching activity,  $f$  is the operation frequency,  $C_L$  is the load capacitance,  $VDD$  is the supply voltage.

## II. CLOCK GATING TECHNIQUE

Clock-Gating [8] is the most common register transfer level (RTL) optimization for reducing dynamic power. In clock gating method, clock is applied only to those modules that are working at that instant. Clock-gating support adds additional logic to the existing synchronous circuit [9] to prune the clock tree, thus disabling the portions of the circuitry that are not in use. By adopting the clock-gating approach, power dissipation can be reduced significantly, lowering not only the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network. Here the clock gating [10] is implemented using AND gates. Fig. 1 shows the schematic of a latch element. A significant amount of power is consumed during charge/discharge cycle of the cumulative gate capacitance  $C_g$  [11] of the latch when the clock is fed directly (Fig. 1(a)) and there is no change in the clock cycle. Fig. 1(b) shows the latch with gated clock. By gating the clock, charge/discharge of  $C_g$  can be affected only when there is change in the clock cycle thus saving power.

## PROBLEMS IN PREVIOUS TECHNIQUES

- In AND gate clock gating we have output correctness problem due to glitches and hazards.
- In NOR gate clock gating we have output correctness problem due to glitches and hazards.
- In Latch based AND gate clock gating design hazards problem is removed but glitches problem still exists.
- In Latch based NOR gate clock gating hazards problem is removed but glitches problem still exists.
- In MUX based clock gating requires an expensive MUX per bit and consumes more power and hardware.

## III. MUX BASED CLOCK GATING

In MUX based clock gating [11] we use multiplexer to close and open a feedback loop around a basic D-type flip-flop under control of enable signal as shown. As the resulting circuit is simple, robust, and compliant with the rules of synchronous design this is a safe and often also a reasonable choice. one negative side of this approach it takes one fairly expensive multiplexer consume more power per bit and consumes more

power. This is because any toggling of the clock input of a disabled flip-flop amounts to wasting of energy in discharging and recharging the associated node capacitances for nothing. In Figure waveform of Negative Edge triggered Counter is shown and in Positive edge triggered. When En turns ON then at each Negative and Positive Edge of the clock respectively counter increments and when En goes Low counter holds its state.

## APPLICATIONS OF GATED CLOCK

- 1- All sequential circuit.
- 2- Memory processing
- 3- Registers & counters.
- 4- Data processing.
- 5- Arithmetic and logic units.

## IV. RESULT

The dynamic power reduction by clock gating technique using MUX is verified on 16x1 MUX. The results shows that a significant change in dynamic power. Figure 2 shows the input voltage, current drawn; dynamic and static power drawn and total power drawn for 16x1 MUX without clock gating applied. Figure 3 shows same result using clock gating.

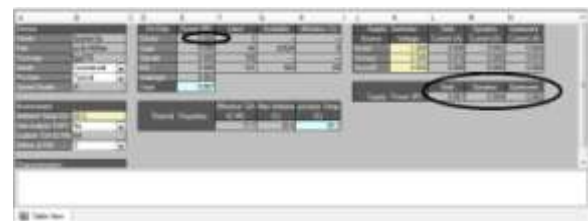


Fig 2 16x1 MUX without clock gating



Fig 3 16x1 MUX with clock gating

## V. CONCLUSION

From above result we can conclude that with gating technique we can reduce dynamic power of any digital circuit dynamic power of 16x1 MUX without gating is 0.04 where it is dynamic power of same MUX with gating is around 0.02. We have reduce the clock or dynamic power of circuit by 0.02.

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