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A 0.6-V 2-nA CMOS Current Reference Circuit

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ABSTRACT
This paper proposes a 0.6-V current reference circuit for use in ultra-low-power applications. In a conventional resistorlessbeta-multiplier current reference circuit, a MOSFET that operates in the strong inversion and triode regions is used as a resistor. Our proposed circuit provides a forward body-biasing for the MOSFET to lower its threshold voltage and make it operate in its strong inversion region even at a very low supply voltage of 0.6 V.We ran simulations using BSIM3v3 SPICE parameters for a 0.18-µm standard CMOS process. At a supply voltage of 0.6V, the reference current was 2nA. The chip area of the proposed current reference circuit was 0.022 mm^2.

Keywords: Analog integrated circuits, CMOS current reference circuit, forward body-biasing,low-voltage design, 0.18-µm standard CMOS process.

I. INTRODUCTION

Current reference circuitsare one of the most important building blocks in analog and mixed-mode circuit systems. These circuits generate a reference current and are used in op-amps, oscillators, phase-locked loops, andA/D and D/A converters[1–3]. As the demand for efficient low-power circuits has significantly increased in recent times owing to the demand for long-lasting batteries in handheld devices, low-voltage current reference circuits have been investigated [1–17]. Some of these circuits operate at a supply voltage greater than 1 V [1–11], whereas others have been found to operate at a supply voltage lower than 1 V [12–17]. Circuits with reference currents of only several nano-amperes have also been reported [6, 11, 12].

In this paper we propose a circuit that provides a reference current of 2 nA and operates at a supply voltage of 0.6 V. Section II describes conventional current reference circuits. Section III presents the proposed current reference circuit and in Section IV simulation results are shown. Finally, conclusions are described in Section V.

II. CONVENTIONALCURRENT REFERENCE CIRCUIT

A beta-multiplier current reference circuit is shown in Fig. 1 [1]; it is an example of a conventional current reference circuit. In this figure, the PMOS transistors M1 and M2 are used to form a current mirror. When the NMOS transistors M3 and M4 operate in their weak inversion regions, the source voltage of M3 is given by the following equation:

$$V_{SM3} = U_T \ln \left(\frac{S_{M3} S_N}{S_{M4} S_N} \right) \qquad (1)$$

where U_T = kT/q is the thermal voltage, and S_{M1}–$S_{M4}$are the aspect ratios of M1–M4, respectively [1]. V_{SM3} is equal to the voltage difference across the resistor R. The reference current I_{REF} is therefore given by the following equation:

$$I_{REF} = \frac{U_T}{R} \ln \left(\frac{S_{M3} S_{M2}}{S_{M4} S_{M1}} \right)$$
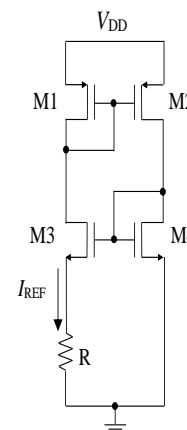
(2)

Fig. 1. Beta-multiplier current reference circuit [1].

The drawback of this beta-multiplier current reference circuit is that it requires a large chip area for its resistor R. Oguey and Aebischer have proposed a circuit in which a resistor is replaced by a MOS transistor as shown in Fig. 2 [2]. The resistor R in Fig. 1 is replaced by an NMOStransistor M5 operating in the strong inversion and triode regions; this enables the chip area to be smaller than that in the beta-multiplier current reference circuit shown in Fig. 1.

However, at a supply voltage of 0.6 V, NMOS transistor M5 operates in its weak inversion

region, unless a special process with a low threshold voltage is used. The resistance linearity of this NMOS transistor then becomes worse than in the strong inversion region.
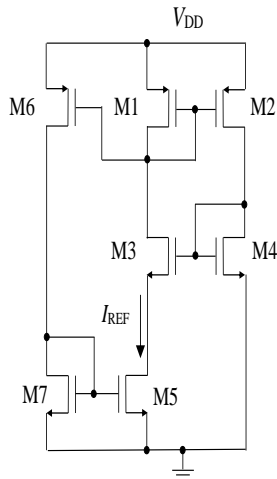

Fig. 2. Resistorless current referencecircuit [2].

In the weak inversion region, the drain current of the NMOS transistor M5 is given by the following equation:

$$I_D = I_0 \frac{W}{L} exp\left\{\frac{(V_{GS} - V_T)}{nU_T}\right\}\left\{1 - exp\left(\frac{-V_{DS}}{U_T}\right)\right\} \quad (3)$$

where I_0 is the process-dependent parameter, and n is the slope factor. The drain conductance is given as follows:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{U_T} I_0 \frac{W}{L} exp\left\{\frac{(V_{GS} - V_T - nV_{DS})}{nU_T}\right\} \quad (4)$$

Therefore, the MOSFET drain resistance canbe expressed as following:

$$R = \frac{\partial V_{DS}}{\partial I_D} = U_T \frac{1}{I_0} \frac{L}{W} exp\left\{\frac{-(V_{GS} - V_T - nV_{DS})}{nU_T}\right\} \quad (5)$$

From Eqs. (1) and (5), the reference current I_{REF} can be given by the following equation:

$$I_{REF} = I_0 \frac{W}{L} \ln\left(\frac{S_{M3}S_{M2}}{S_{M4}S_{M1}}\right) exp\left\{\frac{V_{GS} - V_T - nV_E}{nU_T}\right\} \quad (6)$$

In Eq (6), the exponential term contains a thermal voltage $U_T = kT/q$, and thereforethe reference current I_{REF} depends on the temperature when the NMOS transistor M5 operates in the weak inversion region.

III. PROPOSEDLOW-VOLTAGE CURRENT REFERENCE CIRCUIT

Figure 3 shows our proposed current reference circuit.The body terminal of M5 is now connected to its gate terminal, which is enabled by a deep n-well, electrically separating the p-well of M5 from the p-type substrate. By applying a forward bias voltage between the body and source terminals of M5, the threshold voltage of M5 can be reduced. Hence, M5 can operate in the strong inversion region at ultra-low supply voltages such as 0.6 V.

Since the reference current is in the order of nano-amperes, the gate lengths of MOSFETs M5 and M7 have to be several hundred micrometers.
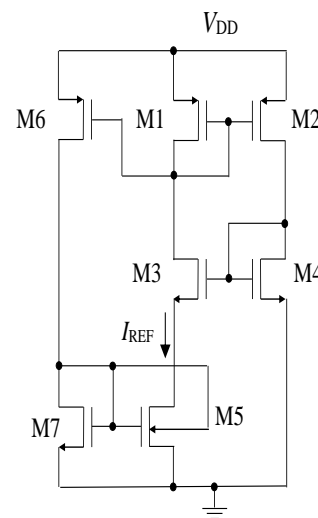

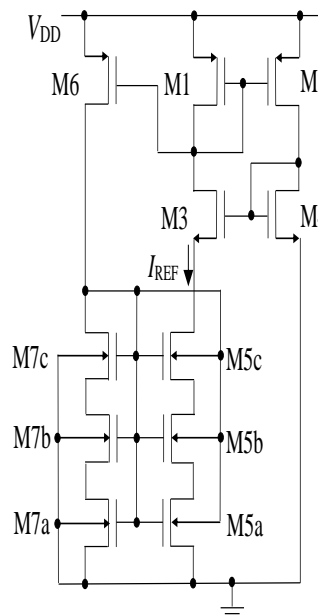**Fig. 3.** Proposed current reference circuit.

Fig. 4. Proposed current reference circuit using the self-cascode structure.

Furthermore, in the proposed circuit, the threshold voltage of M5 can be reduced by body-biasing; hence, its gate length can be a few times larger than that in the conventional circuit shown in Fig. 2. Therefore, we adopted the self-cascode structure for M5 and M7 as shown in Fig. 4 to reduce the gate lengths and make the layout compact.

IV. SIMULATION RESULTS

To verify the effectiveness of the proposed circuit, we ran HSPICE simulations using BSIM3v3 SPICE parameters for a standard 0.18-μm CMOS process. The sum of the threshold voltages, $V_{TN} + |V_{TP}|$, was approximately 0.85 V. Figure 5 shows the

supply voltage dependence of the reference current of the proposed circuit shown in Fig. 4. The minimum supply voltage for the proposed circuit was 0.6 V and the reference current was 1.96 nA. The total power consumption is 3.5 nW at a supply voltage of 0.6 V.

The layout of the proposed current reference circuit is shown in Fig. 6, and its area is 0.022 mm^2. Table I summarizes the simulation results of the proposed circuit and those of the previously reported low-voltage current reference circuits. The minimum supply voltage of our proposed circuit was 0.6 V, which was 0.2 V lower than those of previously reported circuits. Note that the minimum supply voltage of our proposed circuit was 0.25 V lower than the sum of the threshold voltages, $V_{TN} + | V_{TP} |$.
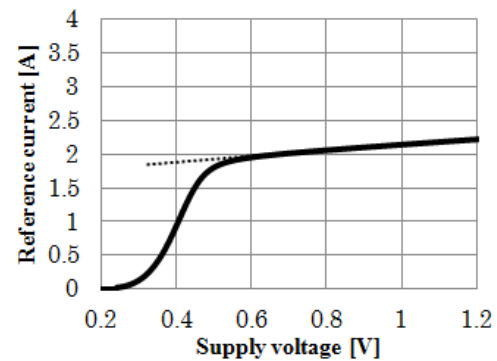

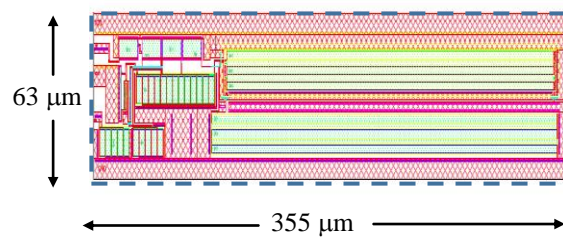**Fig. 5.** Supply voltage dependence of the reference current.

Fig. 6. Layout of the proposed current reference circuit (Fig. 4).

Table I.SUMMARY OF THE SIMULATION/EXPERIMENTAL RESULTS AS COMPARED TO PREVIOUSLY REPORTED CIRCUITS

	Proposed circuit **	[4]*	[6]*	[12]**	[13]*	[16] **
Minimum supply voltage [V]	**0.6**	1.25	1.3	0.85	0.8	0.8
Technology [μm]	**0.18**	0.18	0.35	0.18	0.18	0.18
$V_{TN} + | V_{TP} |$ [V]	**0.85**	-	-	0.87	-	-
Reference current I$_{REF}$ [nA]	**2.0**	92.3	9.95	2.05	54.1	20
Total power consumption [nW]	**3.5 @0.6V**	670 @1.8V	88.5 @1.3V	5.1 @0.85	289 @1V	120 @0.8V
Temperature (°C)	**□40 to 80**	−40 to 85	−20 to 80	-	0 to 80	−40 to 65
TC (ppm/°C)	**26,015**	177	1,190	91	63	-
Line regulation [%/V]	**18.3**	7.5	0.046	1.35	0.21	-
Chip area [mm^2]	**0.022**	0.001	0.12	-	0.245	-
Year	**2017**	2016	2010	2010	2013	2016

*experimental results, **simulation results.

The line regulation of the proposed current reference circuit was 18.3 %/V for a supply voltage ranging from 0.6 V to 1.2 V. It should be noted that the parasitic p–n diode current between the body and source of M5 was approximately 10% of the drain current of M5 (I_{REF}) at a supply voltage of 0.6 V.

One of the issues noted was that the temperature coefficient (TC) of the proposed circuit was much higher than those of the other circuits. The reason is surmised that NMOS transistor M5 in Fig. 3 (and M5a-c in Fig. 4) is in the moderate inversion region rather than completely in the strong inversion region, and the reference current is largely affected

by temperature. This is the issue that we intend to improve in future.

V. CONCLUSION

In this paper, an ultra-low-voltage current reference circuit with no resistor was proposed.This circuit provides a reference current of 2 nA at a supply voltage of 0.6 V without using a special low-threshold CMOS process.To reduce the threshold voltage ofthe NMOS transistor acting as a resistor and make it operate in the strong inversion region, we connect itsbody terminal with the gate terminal. HSPICE simulation results show that the minimum

supply voltage is 0.6 V, which is 0.2 V lower than those of previously reported circuits. The total power consumption is 3.5 nW at a supply voltage of 0.6 V. Thechip area is found to be 0.022mm^2.

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