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Design Discrete Wavelet Transform using Canonic Signed Digit Technique

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ABSTRACT
Conventional distributed arithmetic (DA) is popular in field programmable gate array (FPGA) design, and it features on-chip ROM to achieve high speed and regularity. In this paper, we describe high speed area efficient 2-D discrete wavelet transform (DWT) using 9/7 filter based canonic signed digit (CSD) Technique. Being area efficient architecture free of ROM, multiplication, and subtraction, CSD can also expose the redundancy existing in the adder array consisting of entries of 0 and 1. This architecture supports any size of image pixel value and any level of decomposition. The parallel structure has 100% hardware utilization efficiency.
Keywords: - 2-D Discrete Wavelet Transform (DWT), CSD, Low Pass Filter, High Pass Filter, Xilinx Simulation.

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I. INTRODUCTION

Discrete wavelet transform (DWT) is a mathematical technique that provides a new method for signal processing and decomposes a discrete signal in the time domain by using dilated / contracted and translated versions of a single basis function, named as prototype wavelet [Mallat (1989a) ; Mallat (1989b) ; Daubachies (1992) ; Meyer (1993) ; Vetterli and Kovacevic (1995)]. DWT offers wide variety of useful features over other unitary transforms like discrete Fourier transforms (DFT), discrete cosine transform (DCT) and discrete sine transform (DST). Some of these features are; adaptive time-frequency windows, lower aliasing distortion for signal processing applications, efficient computational complexity and inherent scalability [Grzesczak et al. (1996)]. Due to these features one dimensional (1-D) DWT and two dimensional (2-D) DWT are applied in various application such as numerical analysis [Beylkin et al. (1992)], signal analysis [Akanshu and Haddad (1992)], image coding [Sodagar et al. (1999); Taubman (2000)], pattern recognition [Kronland et al. (1987)], statistics [Stoksik et al. (1994)] and biomedicine [Senhadji et al. (1994)]. Several algorithms and computation schemes have been suggested during last three decades for efficient hardware implementation of 1-D DWT and 2-D DWT.

The DWT is computationally intensive and most of its application demand real-time processing. One way of achieving high speed performance is to use fast computational algorithm in a general purpose computers. Another way is to exploit the parallelism inherent in the computation for concurrent processing by a set of parallel processor. But, it is not cost effective to use a general purpose computer for a specific application. Also, general purpose computer used for their implementation required more space, large power and more computation time. With the development of very large scale integration (VLSI) technology it facilitates to digital signal processing (DSP) system designer to design a high performance, low cost and low power system in a single chip. The characteristic of VLSI system are that they offer greater potential for large amount of concurrency and offer an enormous amount of computing power within a small area [Weste and Eshraghian (1993)]. The computation is very cheap as the hardware is not an obstacle for VLSI system. But, the non-localized global communication is not only expensive but demands high power dissipation. Thus, a high degree of parallelism and a nearest neighbor communication are crucial for realization of high performance VLSI system [Kung (1982)]. Keeping this in view, high performance application specific VLSI systems are rapidly evolving in recent years. The special purpose VLSI systems maximize processing concurrency by parallel / pipeline processing and provides cost effective alternative for real- time application. Therefore, 2-D DWT is currently implemented in a VLSI system to meet the temporal requirement of real-time application. Keeping this fact in view, several design schemes have been suggested in the last two decades for efficient implementation of 2-D DWT in a VLSI system. Researchers have adopted different algorithm formulation, mapping scheme,

and architectural design methods to reduce the computational time, arithmetic complexity or memory complexity of 2-D DWT structures. However, the area-delay performance of the existing structures changes marginally. This is mainly due to the memory complexity, which forms a major hardware component of folded 2-D DWT structure. A detail study of the existing design methods and a complexity analysis is made in Chapter 2 to find an appropriate design strategy to improve the area-delay performance of 2-D DWT structures.

II. LITERATURE REVIEW

Mamatha I et al. [1], when working with the line-primarily based wavelet transform, JPEG2000 wishes to buffer many sub-band lines for future block coding. This coding buffer occupies most people of the reminiscence utilization in a JPEG2000 gadget. On this paper, its first use the multilevel block-primarily based wavelet remodel, after which make use of the multilevel stripe-based wavelet remodel to recognize JPEG2000 coding. The system schemes of the multilevel block-based totally wavelet remodel and the multilevel stripe-based totally wavelet transform for JPEG2000 are provided. The proposed schemes can effectively control the wavelet coefficient output sample, and thus lessen the reminiscence usage of JPEG2000 coding buffer. Compared with the line-based totally wavelet remodel, the proposed schemes reduce greater than 50% reminiscence usage of the JPEG2000 system and slightly decrease the memory bandwidth. Via preserving the blocks/stripes in on-chip memory, which do no longer depend upon the photo length, the reminiscence bandwidth of the JPEG2000 system can be in addition significantly decreased. The gain of the stripe-based wavelet remodel over the block based wavelet remodel lies in that it occupies an awful lot much less inner memory.

R. Praisline Jasmi et al. [2], photograph compression is one of the positive strategies in exceptional varieties of multi-media services. Picture Compression method have been emerged as one of the most vital and successful programs in image evaluation. in this paper the notion of photograph compression the usage of easy coding strategies referred to as Huffman; Discrete Wavelet transform (DWT) coding and fractal algorithm is achieved. These strategies are easy implementation and make use of much less memory. Huffman coding approach includes in reducing the redundant facts in input images. DWT can be able to enhance the quality of compressed picture. Fractal algorithm entails encoding technique and offers better compression ratio. by the usage of the above algorithms the calculation of height signal to noise ratio(PSNR), suggest rectangular errors(MSE) and compression ratio(CR) and Bits in step with pixel(BPP) of the compressed image via giving 512×512 input pictures and also the comparison of performance analysis of the parameters with that above algorithms is finished. The result really explains that Fractal set of rules affords higher Compression ratio (CR) and top signal to noise ratio (PSNR).

Ms. Rashmi Patil et al. [3], this paper provides an implementation of 1-D Discrete wavelet transform DWT the usage of systolic array structure. It plays calculations of low skip and excessive pass coefficients by the use of best one multiplier. This architecture has been carried out and simulated using VLSI. The systolic nature of this architecture corresponds to a clock velocity of 19.27 MHz for Coiflets1 wavelet and occasional electricity of 88.9 mW for Haar wavelet. It has advantage for optimizing region and time. The structure is modular and cascadable for one or multi-dimensional DWT.

Rashmita Sahoo et al. [4], in present day generation memory storing area is not a completely big deal. however when it comes to a transportable gadget i.e. a digital with net in addition to communication facility, then the bandwidth for communique as well as storage are of serious issue. Huge beneficial statistics must be stored and retrieved efficaciously for realistic functions. The Haar wavelet, which is the handiest of all of the 2d DWT, in conjunction with thresholding has been carried out on a JPEG photo. After that Run duration Entropy Coding has been adopted. That is the novel method that authors have proposed for compression of image the usage of parameter CR (Compression Ratio) without dropping the parameter PSNR, the first-class of picture, the use of less bandwidth.

Ms. S. Manjui et al. [5], Carry Select adder (CSLA) is known not the quickest snake among the Conventional snake structures. This work utilizes a productive Carry select viper by sharing the Common Boolean Logic (CLB) term. After a rationale rearrangements, we just need one OR entryway and one inverter door for convey and summation operation. Through the multiplexer, we can choose the right yield as indicated by the rationale conditions of the convey in sign. In view of this adjustment Square root CSLA (SQRT CSLA) construction modeling have been created and contrasted and the standard and Modified SQRT CSLA structural planning. The Modified CSLA structural engineering has been created utilizing Binary to Excess –I Converter (BEC). This paper proposes a proficient strategy which replaces a BEC utilizing regular Boolean rationale. The outcome examination demonstrates that the proposed structural planning accomplishes the three collapsed focal points regarding region, defer and power.

B. Ramkumar et al. [6], convey Select Adder (CSLA) is one of the quickest adders utilized as a part of numerous information handling processors to

perform quick number juggling capacities. From the structure of the CSLA, it is clear that there is extension for diminishing the zone and force utilization in the CSLA. This work utilizes a straightforward and proficient entryway level change to altogether diminish the range and force of the CSLA. In light of this change 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) structural engineering have been produced and contrasted and the general SQRT CSLA structural planning. The proposed outline has diminished territory and force as contrasted and the standard SQRT CSLA with just a slight increment in the deferral. This work assesses the execution of the proposed outlines regarding deferral, region, power, and their items by hand with legitimate exertion and through specially craft and format in 0.18-m CMOS process innovation. The outcomes investigation demonstrates that the proposed CSLA structure is superior to the normal SQRT CSLA.

Gaurav Tewari et al. [7], have proposed a High-Speed & Memory Efficient 2-D DWT on Xilinx Spartan3A DSP using scalable Poly phase Structure with DA for JPEG2000 Standard in 2011. In this paper, they describe an efficient XilinxSpartan3A DSP implementation of 2D DWT (Discrete Wavelet Transforms) using poly phase filter bank architecture with Distributed Arithmetic (DA) to speedup wavelet computation. Results show that the distributed arithmetic formulation results in a considerable performance gain while reducing the consumption of logic resources significantly. This architecture supports any size of Image and any level of decomposition. With minor changes this core can be implemented on any FPGA device.

III. MULTILEVEL DISCRETE WAVELET TRANSFORM

Multiresolution analysis (MRA) is a characteristic feature of SB and it is used for better spectral representation of the signal. In MRA, the signal is decomposed for more than one DWT level known as multilevel DWT. It means the low-pass output of first DWT level is further decomposed in a similar manner in order to get the second level of DWT decomposition and the process is repeated for higher DWT levels. Few algorithms have been suggested for computation of multilevel DWT. One of the most important algorithm are pyramid algorithm (PA), this algorithm are proposed Mallet (1989a) for parallel computation of multilevel DWT. PA for 1-D DWT is given by

$$Y_l^{\,j}(n) = \sum_{i=0}^{k-1} h(i) Y_l^{\,j-1}(2n-i) \quad (1)$$

$$Y_h^{\,j}(n) = \sum_{i=0}^{k-1} g(i) Y_h^{\,j-1}(2n-i) \quad (2)$$

Where $Y_l^{\,j}(n)$ is the n-th low-pass sub band component of the j-th DWT level and $Y_h^{\,j}(n)$ is the n-th high-pass sub band component of the j-th DWT level. Two-dimensional signal, such as images, are analyzed using the 2-D DWT. Currently 2-D DWT is applied in many image processing applications such as image compression and reconstruction [Lewis and Knowles (1992)], pattern recognition [Kronland *et al*. (1987)], biomedicine [Senhadji *et al*. (1994)] and computer graphics [Meyer (1993)]. The 2-D DWT is a mathematical technique that decomposes an input image in the multiresolution frequency space. The 2-D DWT decomposes an input image into four sub bands known as low-low (LL), low-high (LH), high-low (HL) and high-high (HH) sub band.

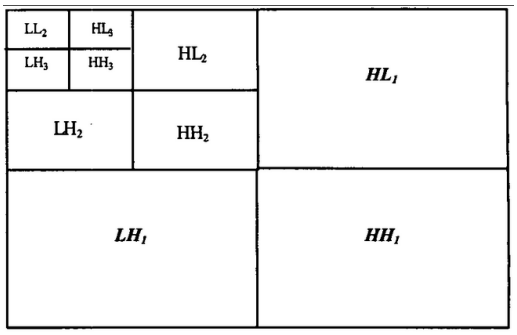

Figure 1: Three Level Diagram of 2-D Sub-band Wavelet Transform

IV. PROPOSED ARCHITECTURE

On this paper, the original signal X[n] has N- sample points, is exceeded thru 1×2 demultipler. Whilst pick out line is 0 then we get even pattern and whilst choose line is 1 then we get abnormal sample. After that we've got handed those samples through CSD based totally low-skip filter out, equal method with high-skip filter. Now we get N/2 sample s at the primary decomposition level output of CSD primarily based high-skip (Y_H) and low-pass filter out (Y_L). At the second decomposition level, the output of CSD based totally low-skip and high-bypass clear out handed through a sign in unit. Now the output of sign up unit surpassed via mux. Whilst the pick line 0, we get CSD primarily based low-skip filter out output and while the choose line 1, we get CSD primarily based high-skip filter out. Now we've surpassed mux output via CSD primarily based low-pass filter out then we get Y_LL &Y_LH output now equal method implemented with the CSD based high-skip filter out we get Y_HL & Y_HH. on the 0.33 decomposition degree, the time period is doubled and frequency can be 1/2, and the output of

CSD primarily based low-pass and excessive-skip filter out is passed through a check in unit. Now the output of check in unit is surpassed via mux. when the choose line is 00. Now finally we have passed mux output through CSD based low pass filter and high pass filter we get Y_{LLL},Y_{LHL}, Y_{HLL}, Y_{HHL} and Y_{LLH}, Y_{LHH}, Y_{HLH}, Y_{HHH}.

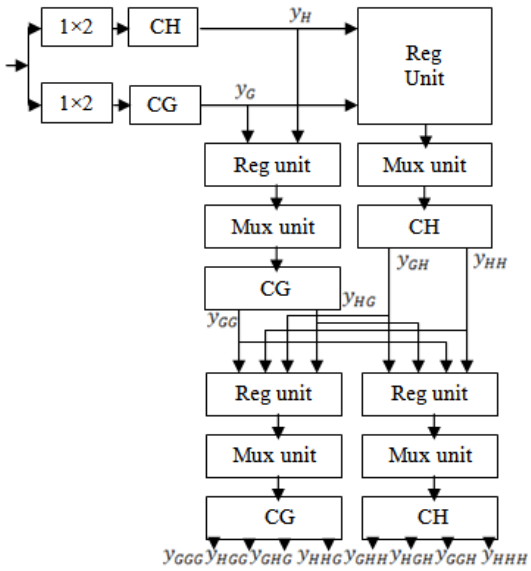

Figure 2: 3-Level CSD design based DWPT, CG and CH means the CBL design based low & high-pass filter.

SIMULATION RESULT

We have implemented multiplier based (MB) architecture and common Boolean logic based (CBL) architecture for DWT by different approaches. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter (AOI), each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

V. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 6.2i updated version. Xilinx 6.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 6.2i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-2 FX and Virtex-E LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing.

We functionally 2-D sub-band WT verified presented in this paper including all low pass filter and high pass filter. We have been found from the results shown in table 1, that number of slices, number of slices LUTs and maximum combinational path delay used in different types of device family. RTL (resister transistor logic) view is 1-D sub-band tree structure in shown in figure 3.

All of the designing and test concerning algorithm that referred to in this paper is being developed on Xilinx 14.1i up to date version. Xilinx 14.1i has couple of the striking functions inclusive of low reminiscence requirement, fast debugging, and occasional price. By means of the aid of that software program we debug the program without problems.

A. Result and Analysis

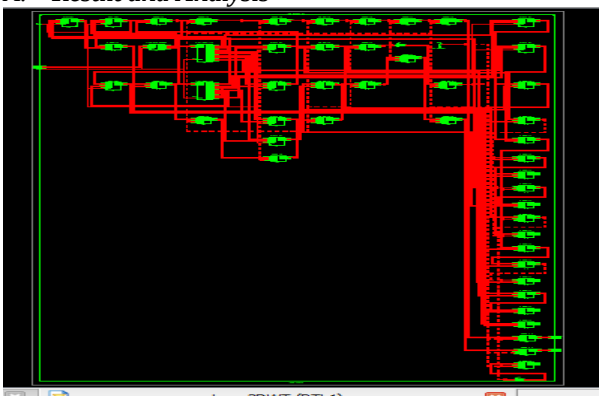

Figure 3: RTL View of 1-D DWT using Canonic Signed Digit

Table 1: First Level DWT using CSD Technique

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	35	301440	0%
Number of Slice LUTs	213	150720	0%
Number of fully used LUT-FF pairs	10	238	4%
Number of bonded IOBs	29	400	7%
Number of BUFG/BUFGCTRLs	1	32	3%

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 1.380ns (Maximum Frequency: 724.638MHz)
   Minimum input arrival time before clock: 0.471ns
   Maximum output required time after clock: 11.542ns
   Maximum combinational path delay: 10.949ns
```

We functionally 2-D sub-band WT verified presented in this paper including all low pass filter and high pass filter. We have been found from the results shown in table 1, that number of slices, number of slices LUTs and maximum combinational path delay used in different types of device family. RTL (resister transfer level) view is 2-D sub-band tree structure in shown in Figure 4.

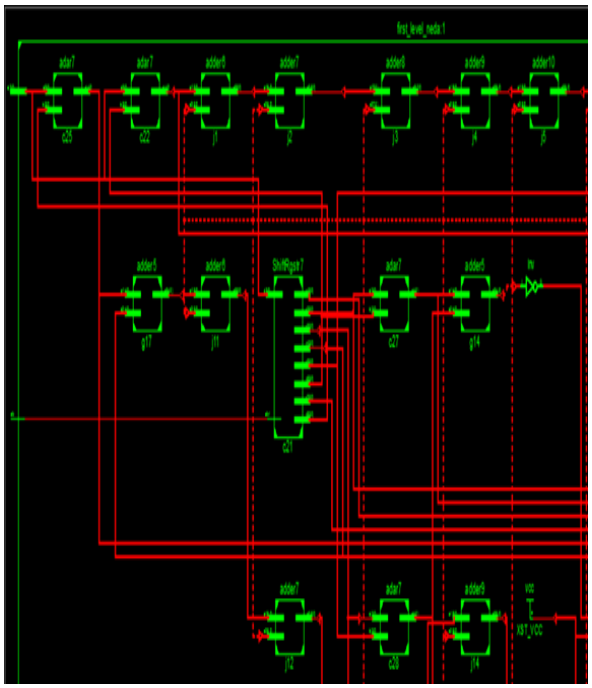

Figure 4: RTL View of 2-D DWT using Canonic Signed Digit

Table 2: Second Level DWT using CSD Technique

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	228	301440	0%
Number of Slice LUTs	728	150720	0%
Number of fully used LUT-FF pairs	134	822	16%
Number of bonded IOBs	44	400	11%
Number of BUFG/BUFGCTRLs	1	32	3%

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 6.911ns (Maximum Frequency: 144.703MHz)
   Minimum input arrival time before clock: 6.836ns
   Maximum output required time after clock: 13.172ns
   Maximum combinational path delay: 13.097ns
```

Table 3: Comparison result of existing algorithm and proposed algorithm

Design	No. of Slice Registers	No. of Slice LUTs	LUT Flip Flop pair	Bonded IOBs	Maximum Frequency (MHz)
Mamatha I, Shikha [11]	139	417	71	358	633.43
Proposed Design	35	213	10	29	724.638

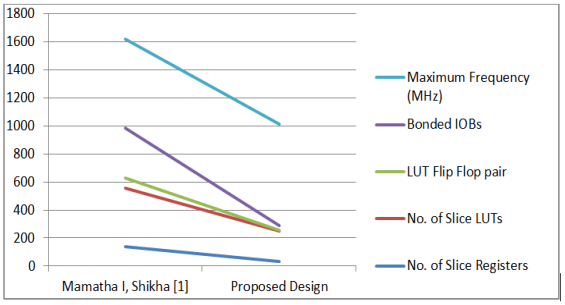

Figure 5: Shows the Bar Graph of the Previous Algorithm and Implemented Algorithm

VI. CONCLUSION

2-D sub-band wavelet transform standardize two basic blocks for representing the image compression namely, low pass filter and high pass filter. Wavelet transforms a vast application in many areas like image compression, signal processing and VLSI design. We propose a 2-D sub-band novel distributed arithmetic paradigm named CSD structure for VLSI implementation of digital signal processing (DSP) algorithms involving inner product of vectors and vector-matrix multiplication. We demonstrate that CSD is a very efficient architecture with adders as the main component and free of ROM (free memory), multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary.

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