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Low power and Area Efficient MDC based FFT for Twin Data Streams

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ABSTRACT
Fast Fourier transform (FFT) has become multivariate in many industrial environments. FFT is one of the most employed architecture in multipurpose communication and signal processing systems. The main intent of this paper is to design an efficient Twin Data Streams FFT processor for numerous applications. The FFT architecture used in the Multipath Delay Commutator will process an N / 2 point decimation in time FFT and an N / 2 point decimation in frequency FFT operations of odd and even samples of two Data streams separately to reduce the area and improve throughput. By using the bit reversal operation in the architecture the number of registers will be decreased. Multipath Delay Commutator (MDC) with FFT parallelized architecture is used to achieve high throughput. Modified booth multiplier is used to reduce number of partial products and complexity of the system when compared to serial multiplier.

Keywords: Decimation in Time (DIT), Decimation in Frequency (DIF), bit reorder, Multipath Delay Commutator (MDC), Pipelining, Radix-2.

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I. INTRODUCTION

FFT is one of the most efficient algorithms used in wireless communications to increase the transmission rate of the system. Generally FFT is a crucial block in OFDM systems. To overcome, the difficulties of large area, low throughput and power consumption, pipelined FFT architectures are introduced. Pipelined FFT architectures which reduces the area, power consumption and gives the high throughput. There are two types of pipelined FFT architectures Delay feedback(DF), Delay Commutator (DC), according to the number of input data stream paths, the two pipelined FFT architecture can be classified into Single Path Delay Commutator (SDC) , Multipath Delay Commutator (MDC), single path delay feedback(SDF), Multipath delay feedback (MDF) [1]. Using SDC, SDF, MDC pipeline techniques are observed. Whenever the multiple inputs are given the multiple output data is not available [2-3].

To reorder the bits FFT output into normal order, the Bit Reversal circuits are used [4-5]. In the pipelined FFT architecture the bit reversal operation is done by data scheduling registers. In this registers are used to recover the inverted samples. When the even samples of the input are given the bit reversal operation is done after the Butterfly operation, when the odd samples of the input are given the bit reversal operation is done before the Butterfly operation [6-7]. Serial multiplier multiplies any two input bits and is designed with half adder and full adder [8-9]. The advantage of Modified Booth algorithm is it can be easily implemented but the drawback of serial multiplier is circuit complexity increases as the number of partial products are increased[10-11], to overcome this draw back Booth multiplication algorithm is proposed which reduces partial products, increases the throughput and finally leads to reduction of power consumption[12-14].

In this paper the architecture is based on Multipath Delay Commutator (MDC) technique to parallel pipelined FFT architecture is implemented. In this architecture both N/2 point DIT FFT and N/2 point DIF FFT works simultaneously. For bit reversing scheduling registers are used these registers are used delay the sample to perform the butterfly operation. And Booth multiplier is used instead of serial. As a result the implemented architecture as the advantages of less number of registers, high throughput and power reduction.

In the below Fig.1 there are 6 levels, which are named as L_1, L2, L3, M_1, M_2, and M3. The registers L1 and M_1 levels changes the odd input

data and reorder the bits, L_3 and M_3 changes the even input data and reorder the bits. There are two switches SW_1, SW_2 which plays an important role to control the operation of radix-2 MDC FFT architecture. In SW_1, SW_2 there are two modes of operation one is normal mode and another one is swap mode which have two dissimilar modes of operation for N/2 cycles. In normal mode the input data u_1 u_2 u_3 u_4 is applied and the output v_1 v_2 v_3 v_4 is obtained. When coming to the swap mode the output obtained is v_3 v_4 v_1 v_2.

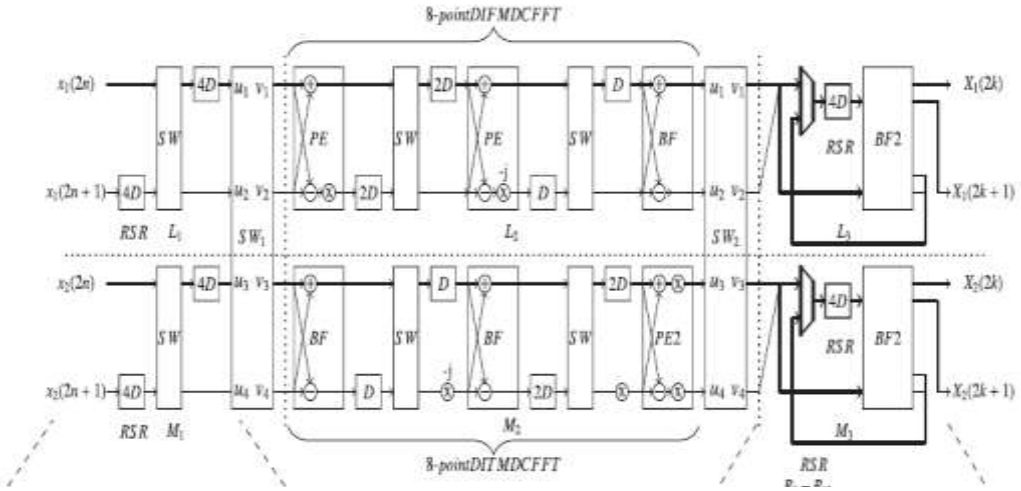

Fig.1. Radix-2 Pipelined FFT Architecture.

The even data occurs at the 8-point DIFMDC FFT to undergo the DIF operation and produce the data and forwarded to L_3 and perform bit reversal operation. At the last stage butterfly operation is performed then the outputs will be obtained in normal order. After performing DIF change the switch mode operation the odd data is passed to M_2 and the DIT is performed after M_2 is forwarded to M_3, at the last stage butterfly operation is performed.

The rest of the paper is structured as follows: In section II, the proposed Modified Booth Algorithm for pipelined FFT architecture is presented. The following section III explains experimental results, performance comparisons are discussed. And finally conclusion of this paper is shown in section IV.

II. MODIFIED BOOTH ALGORITHM FOR PIPELINED FFT ARCHITECTURE

Multiplication is mostly used in digital system signal processing, graphics and scientific computation. Different techniques are used to design multipliers to achieve high speed, low power consumption, less area and cost reduction for the system. The proposed method shown in Fig.2 is used for designing and simulation of radix-8 Booth encoder multiplier for signed- unsigned numbers.

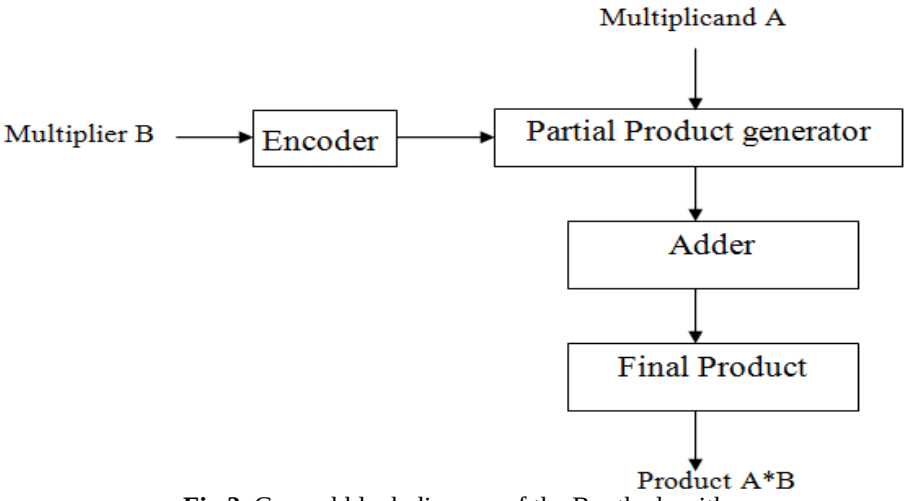

Fig.2. General block diagram of the Booth algorithm.

n/3 partial products are produced by the radix- 8 Booth encoder circuit in parallel. In the Fig.3 modified Booth encoder circuit with Carry Save Adder (CSA) and Ripple Carry Adder (RCA) are used to speed up the multiplier operations. This multiplier performs signed and unsigned multiplication. The radix-8 Booth recoding algorithm is same for the radix-4. In radix-4 three multiplier bits are grouped, but in radix-8 four multiplier bits are grouped.

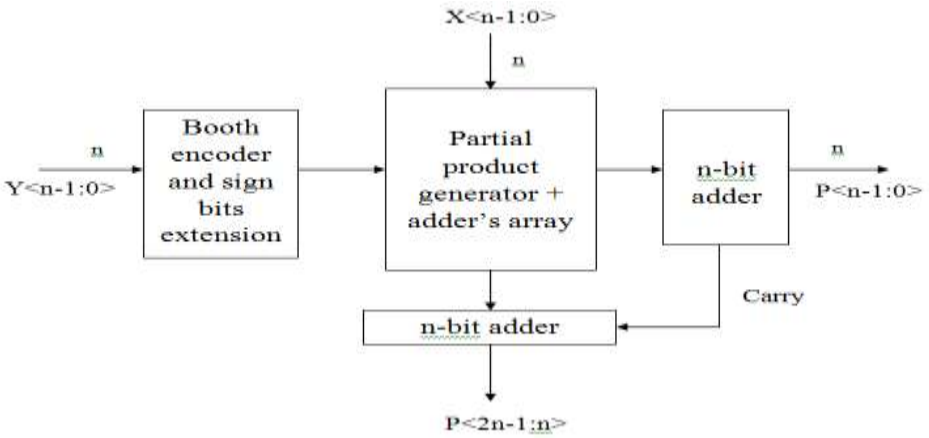

Fig.3. Block diagram of Modified Booth algorithm.

Multiplier bits grouping is mainly based on radix Modified Booth algorithm, which reduces the partial products by half when compared with other architectures. By using the radix number, multiplier is divided into overlapping groups of n-bits. Appending '0' to LSB and grouping 4 bits to multiplier. Appending with two zeros to the MSB if n is even, and appending with one zero to the MSB if n is odd. In radix8 four bits are grouped together with one Overlapping bit. Booth's recoding method does not propagate the carry to subsequent stages. Each of the recoded digits can be obtained independently. Colon is used to represent concatenation of bits. Booth multiplier provides high speed and low power consumption.

Table.1. Partial product generator of Encoding table for radix-8 modified Booth multiplier

Group of multiplier bits	Operation to be perform on multiplicand
0000	0
0001	1xMultiplicand
0010	1xMultiplicand
0011	2xMultiplicand
0100	2xMultiplicand
0101	3xMultiplicand
0110	3xMultiplicand
0111	4xMultiplicand
1000	-4xMultiplicand
1001	-3xMultiplicand
1010	-3xMultiplicand
1011	-2xMultiplicand
1100	-2xMultiplicand
1101	-1xMultiplicand
1110	-1xMultiplicand
1111	0

From the Table 1 the product remains same as the multiplicand value when multiplying by 1, multiplicand is multiplied by 2 to perform shift left multiplicand value by one time. Multiply by -1 means the product is 2's complement of the multiplicand. Multiplicand is multiply by 3 perform both multiplicand is multiply by 1 and 2 operations. Multiplicand is multiply by 4 performs 2 times shift

left multiplicand value.

III. EXPERIMENTAL RESULTS

Table.2. Design summary of parallel pipelined MDC FFT with Modified Booth algorithm.

S.No	PARAMETERS	VALUE
1	Number of Slice LUTS (in %)	1
2	Number of occupied Slices (in %)	1
3	Number of bonded IOBs (in %)	12
4	Min clock period	28.821ns
5	Frequency	34.696MHz
6	Dynamic Power	0.167(W)
7	Quiescent Power	0.119(W)
8	Total Power	0.286(W)

The presented architectures have been implemented for the use in field programmable gate array (FPGA). The Simulation results for L_1 and M_1 levels are shown in the Fig.4. Here N/2 odd bits are reordered and even bits pass normally. The Simulation results for DIF (Decimation in frequency) are shown in Fig.5. In DIF 8 input data perform operation to get the corresponding output.

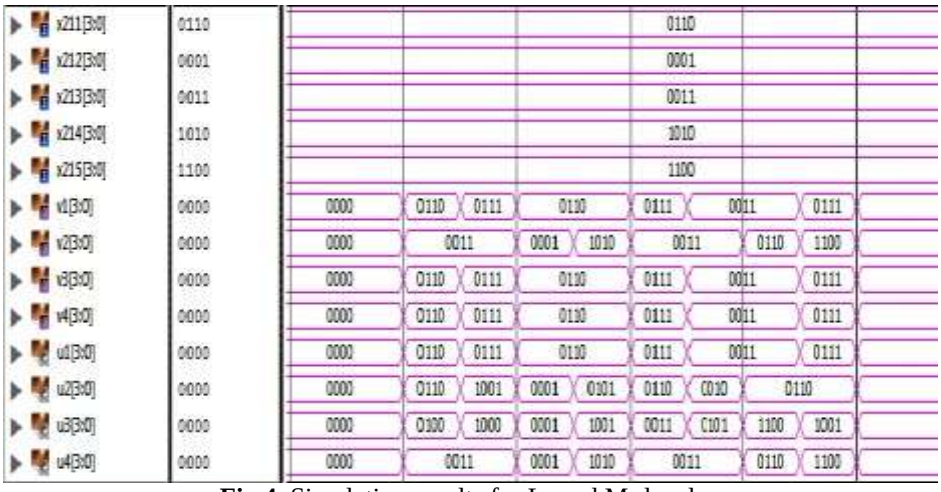

Fig.4. Simulation results for L_1 and M_1 levels.

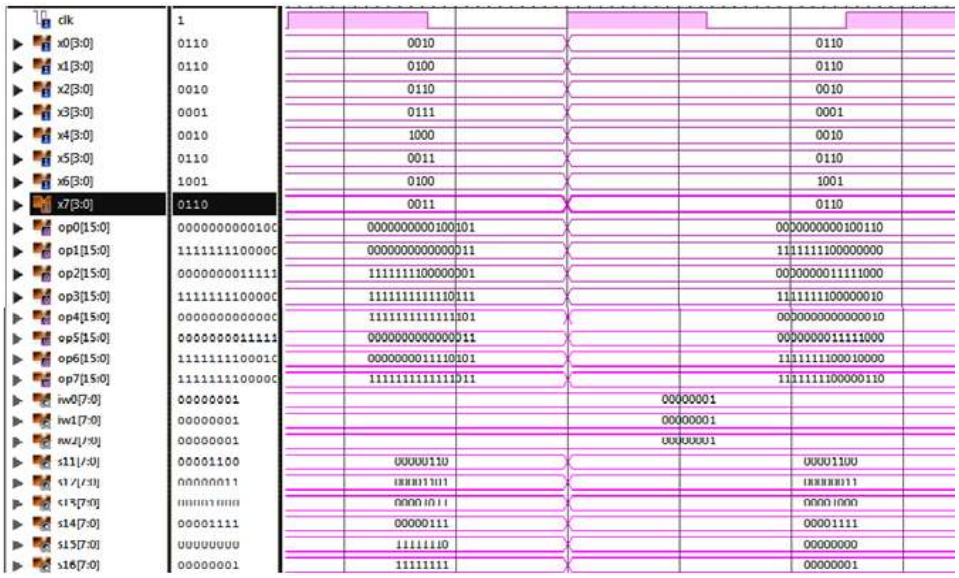

Fig.5. Simulation results for 8-point DIF (Decimation in frequency) MDC FFT.

Fig.6 Shows the Simulation results for DIT (Decimation in Time).here eight inputs are given, DIT operation is perform corresponding the output is appeared Fig.7 Shows the Simulation results for radix-2 MDC FFT Architecture, at the last stage all the operations including butterfly operation the corresponding output occurred in normal order. Fig.8. RTL Schematic of MDC FFT Architecture Fig.9. Simulation results for Modified Booth algorithm multiplier; whenever the two inputs are given the corresponding output is occurred.

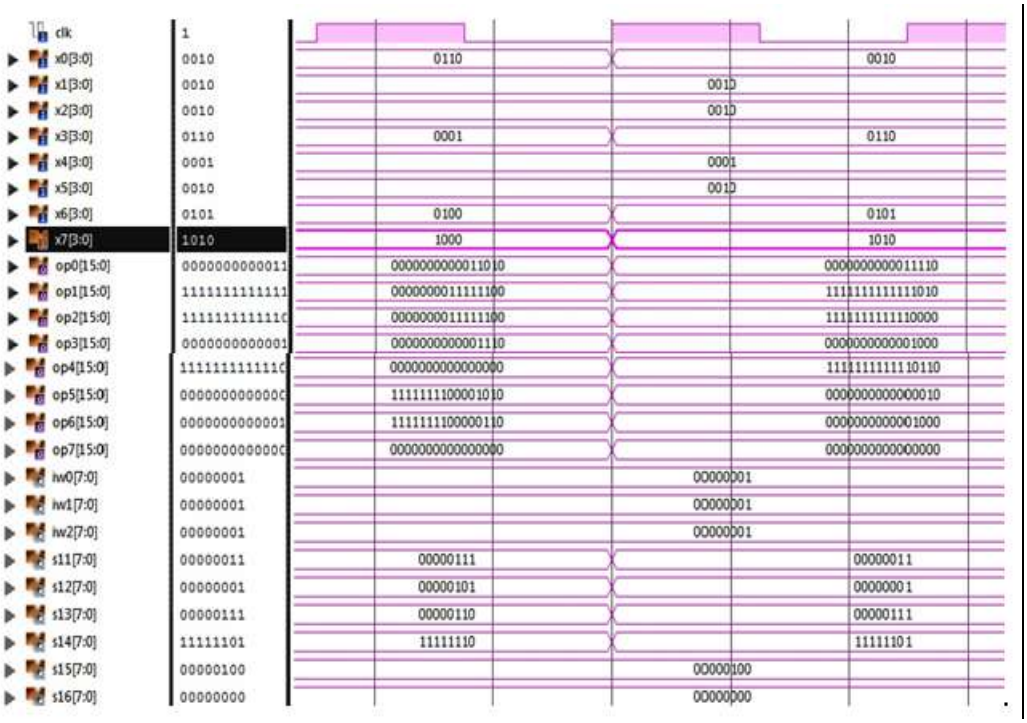

Fig.6. Simulation results for 8-point DIT (Decimation in Time) MDC FFT.

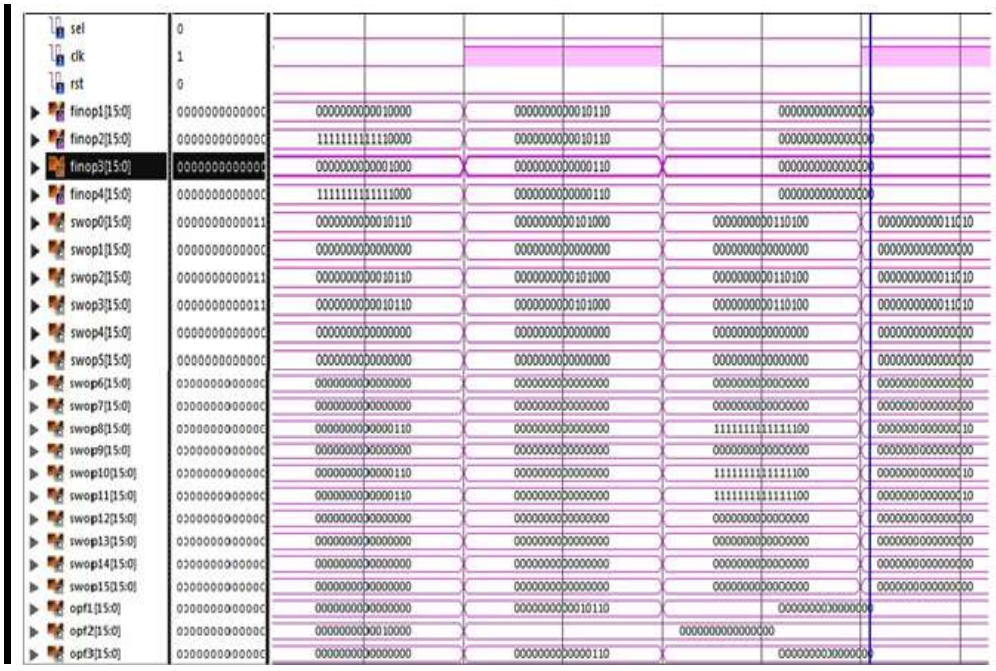

Fig.7. Simulation results for radix-2 Pipelined FFT Architecture.

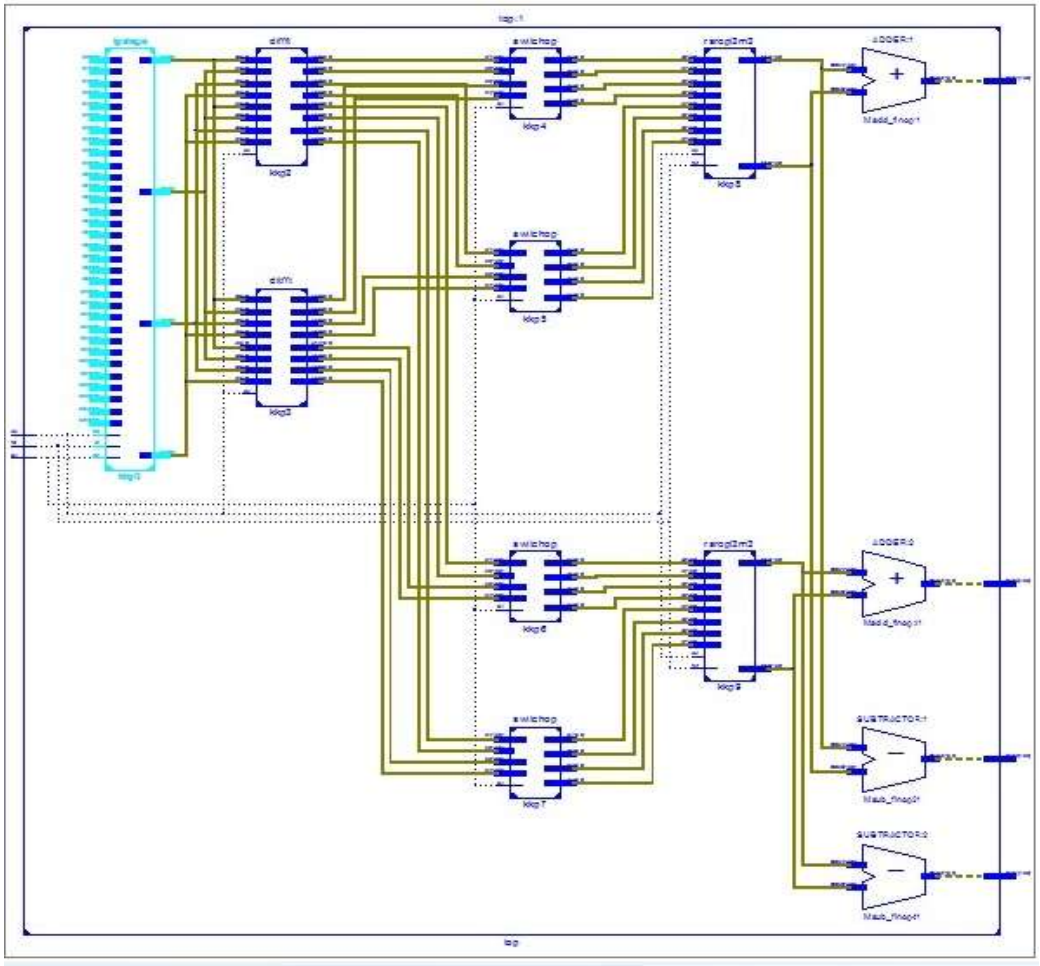

Fig.8. RTL Schematic of radix-2 Pipelined FFT Architecture.

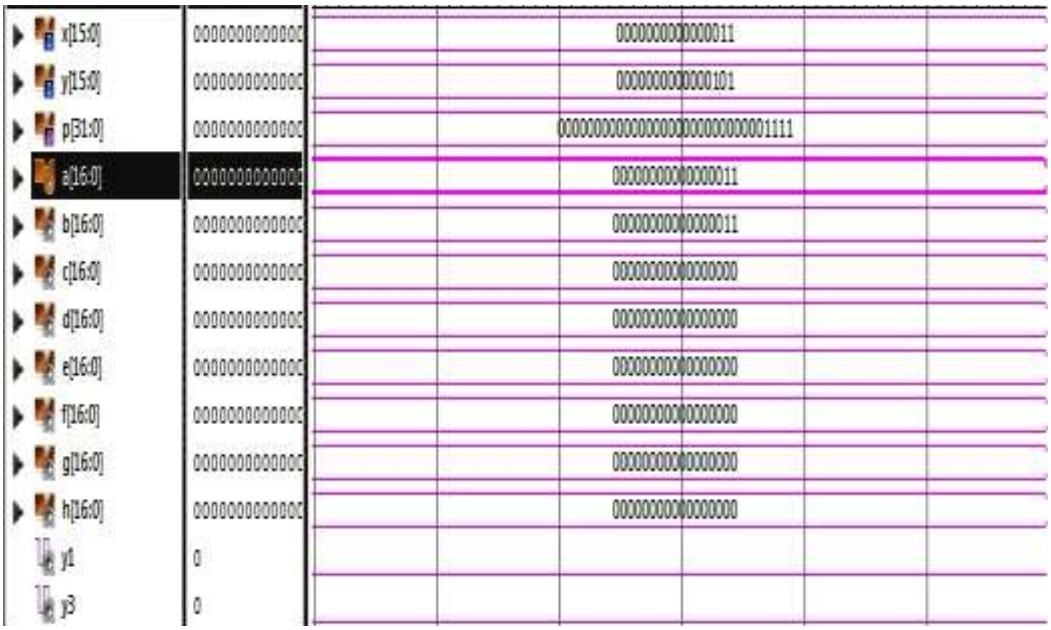

Fig.9. Simulation results for modified Booth algorithm.

Table.2. Power report comparison of existing and proposed Radix-2 MDC FFT architecture

Name of the system	Power (mw)
Radix-2 MDC FFT architecture power report	340
Proposed architecture	286

Proposed architecture reduces the 54mw power than existing architecture, so the performance of the system is increased.

Table.3. Comparison between MDC FFT Architecture with serial multiplier and MDC Architecture with modified Booth Algorithm

S.No.	Parameters	MDC FFT Architecture with serial multiplier	MDC FFT Architecture with modified Booth Algorithm
1	Number of Slice LUTS (in %)	1	1
2	Number of occupied Slices (in %)	2	1
3	Number of bonded IOBs (in %)	92	12
4	Dynamic Power	0.219(W)	0.167(W)
5	Quiescent Power	0.121(W)	0.119(W)
6	Total Power	0.340(W)	0.286(W)

MDC Architecture with modified Booth Algorithm is compared with MDC FFT Architecture with serial multiplier in various parameters like number of slice LUTs, number of occupied slices, number of bonded IOBs, dynamic power, Quiescent power, total power .The implementation results are almost give the same output but power ,area is less when compared to MDC FFT Architecture with serial multiplier.

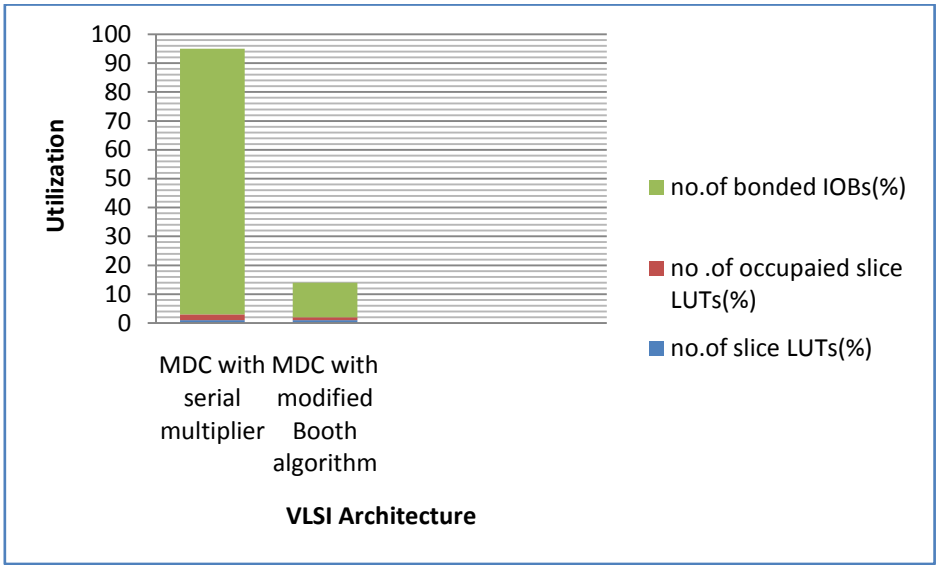

Fig.10. Comparison of area of VLSI architectures for MDC FFT Architecture with serial multiplier and modified Booth algorithm

Fig.10. states the Comparison of area of VLSI architectures for MDC FFT Architecture with serial multiplier and modified Booth algorithm. Finally absorbed MDC FFT Architecture with modified Booth algorithm occupies less area than serial multiplier MDC FFT Architecture.

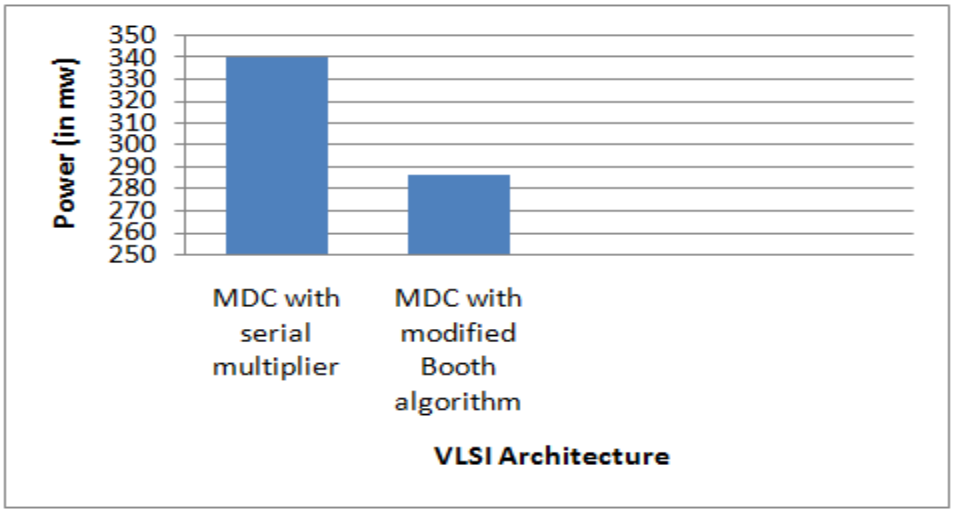

Fig.11. Comparison the power of VLSI architectures of radix-2 pipelined MDC FFT Architecture with serial multiplier and modified Booth algorithm

Fig.11. explain the power comparison between MDC Architecture with modified Booth Algorithm and compared with radix-2 pipelined MDC FFT Architecture with serial multiplier. Finally it states that the MDC FFT Architecture modified Booth Algorithm performance is increased.

IV. CONCLUSION

Radix 2 FFT architecture is designed and implemented using bit reversal circuits to reorder the bits for twin data streams and serial multiplier to process the data. In radix2 FFT architecture area of the circuit is increased and power consumption for the architecture is high. To overcome this disadvantage the serial multiplier in radix 2 FFT architecture is replaced by modified booth algorithm. Using the proposed architecture implementation the power consumption of the circuit is reduced from 340 mw in existing architecture to 286 mw in proposed architecture.

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