RESEARCH ARTICLE OPEN ACCESS

On the Construction of Ground Bounce Noise Reduction Using Three - Step Wake-Up Partitioning

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ABSTRACT
In low power nanotechnology, the sub-threshold leakage occurs and it can be controlled by power gating techniques which does not affect the performance of the circuit. But the transitions of mode in the power gating takes place along with the large inrush/discharge currents which causes inductive noise on the power supply and the ground rails. The above issue can be tackled by slowly turning on the sleeping transistor, but introduces a fixed lower bound on the delay overhead, independent of the duration of the sleep period. The effect of changes in the internal circuit nodes at the time of wakeup is not been taken into account in the conventional methods. Under the observation of the internal nodes during sleep-to-active transition, can be partitioned into three distinct stages. This serves as the motivation for taking three–step turn on scheme that limits current flow while the gated block is in the metastable state. It strongly reduces power gating noise along with reduced wakeup time. The simulation is performed using full adder in 0.13µm technology as circuit under test. The further modifications are done to reduce the power consumption

Keywords: Ground bounce noise, Inrush currents, Multimode Power gating, Power gating.

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I. INTRODUCTION

MTCMOS is considered as one of the efficient power gating technique, for reduction of leakage power during standby mode of the circuit. It allows High speed operation during the active mode in burst mode type circuits [8]. Controlling leakage with long idle time reduces battery lifetime 9]- .Effective reduction of sleep mode power consumption but Overheads occurs in performance, area, dynamic power dissipation . When sleep transistor is used as header contributes virtual power supply rail, also discharges to a steady-state value during long sleep period that is close to the ground.

Effectively suppresses the leakage currents due to zero difference voltage between supply and ground .But large inrush currents occurs due to the restoration of virtual power supply to the full swing .Wastage of energy and increased wake-up time also causes current surges leading to voltage fluctuations in the power/ground network, parasitic impedances of off-chip bonding wires and on-chip power rail. IR drop and Ldi/dt in the wake-up process is known as power gating noise (PGN).Separate power line bypasses the rush current In[10] includes overheads due to power rail and extra bypass switches The above considerations strongly focus on the internal nodes during the wake-up time and the inductive noise of power and ground rails including the overheads of time and energy.

This motivates to consider the reduction of inrush currents which can be achieved by dividing the wake-up transition into three stages thus introducing three step power gating–on scheme which reduces internal node noise. Supply voltage reduction only during metastable state which is sensitive to noise; suppress the power –gating noise and the wake-up time.

The multimodal power gating are used for reducing the power consumption further. The comparisons can be made to prove the efficiency of the current and enhanced work.

1.1 DESCRIPTION

This paper considers the behaviour of internal nodes is observed during the sleep-to-active mode transition and identified three distinct stages. This motivates a three-step turn-on scheme and an associated compact power-gating structure that limits the current flowing through the sleep transistor only while the gated block is metastable, but quickly boosts the power supply rail when there are no short-circuit current paths in the logic.The three-step wake-up partitioning technique consists of a control logic block which controls the sleeper transistors.

The power gating is achieved by usage of three sleeper transistors namely M1, M2, M3as denoted in the figure1(a).The sleep signal is given through the signals like S1,S2,S3 which controls the

gating cell through the control logic. Threshold detector is main part of the control logic which indicates the region in which noise minimization should be considered. Control logic consists of two detectors which indicate the starting and ending point of the particular noise limiting region according to the values of VVDD depending on the threshold voltage fixed with the sleeper transistors.

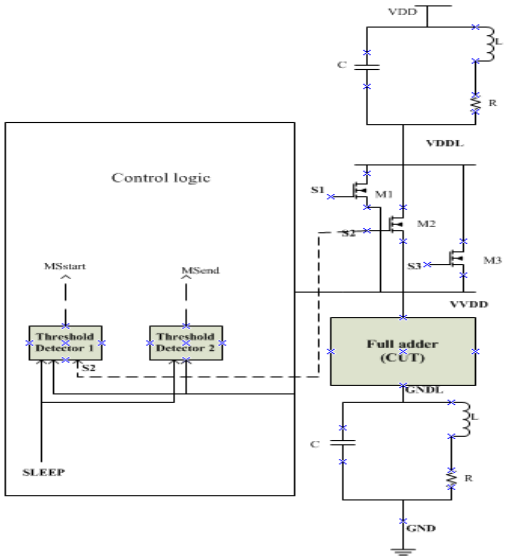

Fig.1 (a): Circuit for three-step wake-up scheme.

1.2 WORKING OF THREE-STEP SCHEME

This scheme mainly depends on the signals given to the sleeper transistors. Here PMOS transistors are used as the sleeper transistors and hence it becomes ON only when logic'0'is applied. Based on the value of S1,S2,S3 the various states of three-step are obtained .the various stages are as follows

1. Pre boosting stage(VVDD<Vtp)
2. Noise limiting stage (VVDD>Vtp)
3. Post boosting stage (VVDD>Vtp+Vtn)

These stages are occurred only when the logic circuit is in sleep mode i.e. SLEEP=0.Individual signals are applied to sleeper transistors to perform power gating operation.

There are three steps in normal operation of any power gating circuits ,they are

i. Active
ii. Sleep
iii. Wake-Up

The current work mainly focuses on the wake-up stage since there are likely chances for the occurrence of noise due to inrush current while transition of the logic circuit takes place. Thus they are partitioned as above stated .The operation is as follows ,when **S1=0,S2=1,S3=1** then the circuit goes to pre- boosting stage were the virtual VDD is slightly lesser than threshold voltage of PMOS transistor and the Threshold Detector 1detects the region of noise limiting stage by sending

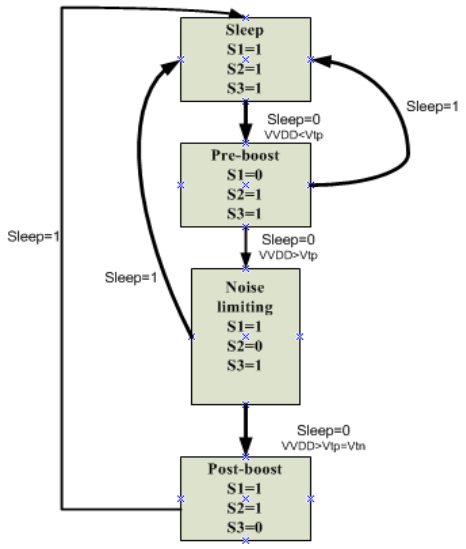

Fig.1 (b): Transition Diagram

MSstart signal to the control logic in which control has to be employed also the Threshold Detector 2 sends MSend at the end of the noise limiting stage this occurs when both 1 **S1=1,S2=0and S3=1**.when the signals are **S1=1,S2=1,S3=0** then it goes to post-boosting stage were virtual VDD is greater than the threshold voltage.

The operation of the three –step is well explained with the help of the fig1(b).The logic circuit1(c) of the control logic block clearly shows way of observing the noise limiting stage among all other region in the wake-up process of the logic block (full-adder) .the control logic block consists of three modules

1. Threshold detector 1
2. Threshold detector 2
3. Combinational logic

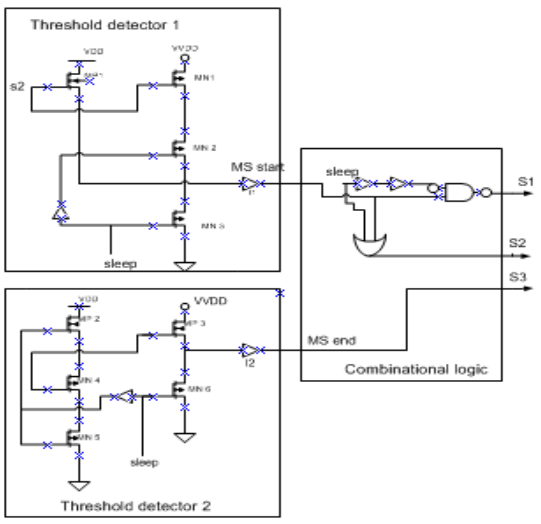

Fig.1(c): *Control logic block*

The signal S2 is sent feedback to the Threshold Detector 1 which closely determines whether the virtual voltage crosses the pre-determined value and send MSstart signal which indicates the noise limiting region. Threshold detector 1 consists of low skew inverter which generates high to low pulse and alarms the circuit. Similarly Threshold detector 2 send MSend signal by monitoring the voltage value and along with the combinational logic circuit it generates sleep signals S1, S2, S3.

II. ENHANCEMENT AND MODIFICATION

The above work, though it proves to be efficient in conserving the power during the idle state of the logic circuit. It consumes more power due to increased number of transistors used in the control logic. So as an enhancement the same power gating can be employed with multimode techniques.

Single mode power gating is replaced by tri-mode power gating technique. It introduces drowsy state instead of wake-up state and hence the analysis is made with the help of simulation. It consists of sleep inverters and also external drowsy signal to control the logic block. Fig 2(a) and 2(b) shows the tri-mode technique. The simulation results are shown in the following chapter.

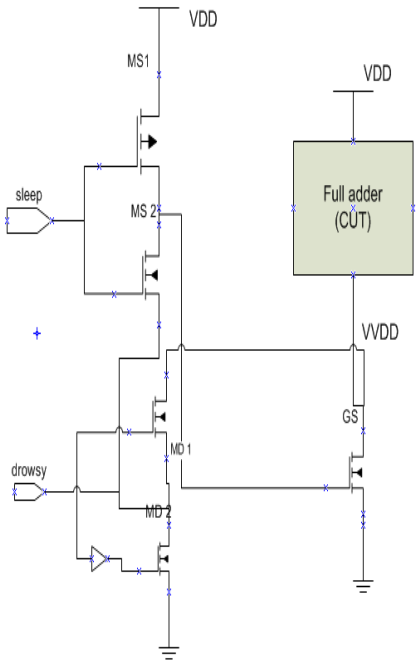

Fig.2: Circuit tri-mode footer technique

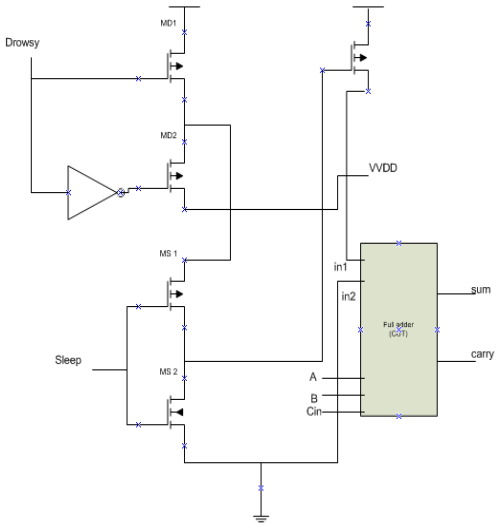

Fig.2: Circuit tri-mode header technique

The working of both header and footer is similar and it results in the power reduction of the entire circuit.

III. SIMULATION AND WAVEFORM RESULTS

The simulation is done using T-SPICE tool with.13µ technology and the various results are shown below

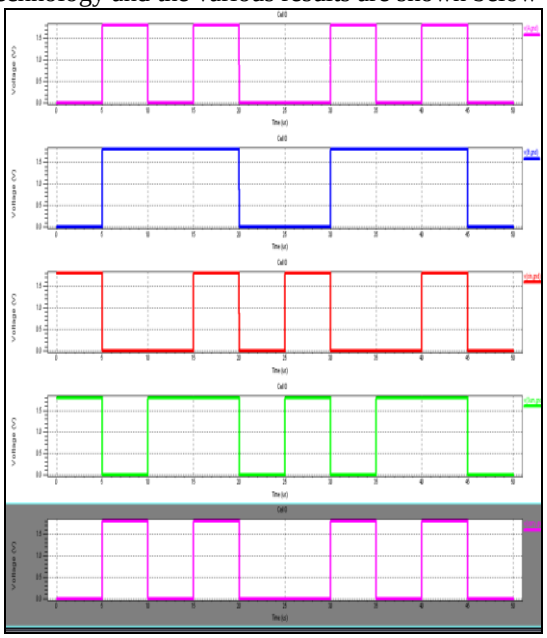

Fig.3 (a): Waveform of adder circuit

The above Fig. shows the perfect functioning of full adder.

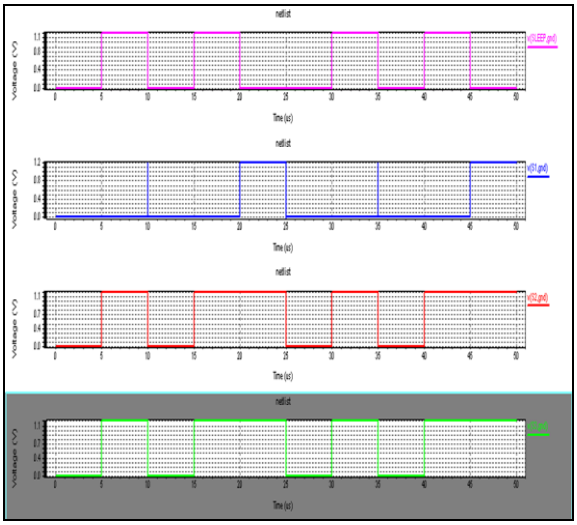

Fig.3 (b)*:* Control logic wave results

The waveform of overall circuit block is below

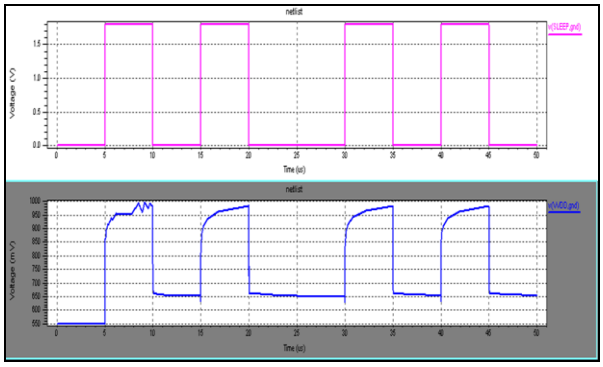

Fig.3(c): Overall circuit with virtual VDD

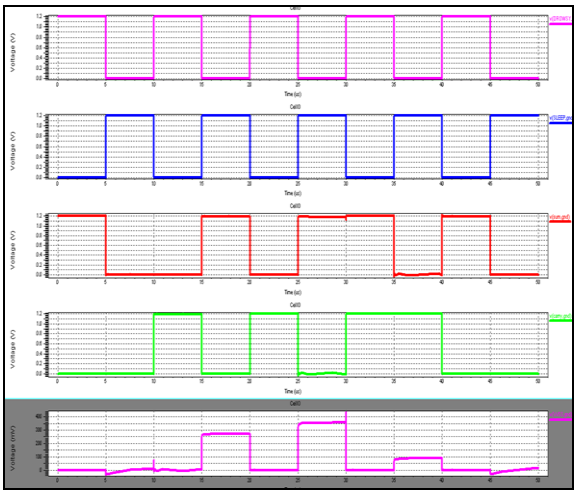

Fig.3 (d): Tri-mode footer power gating

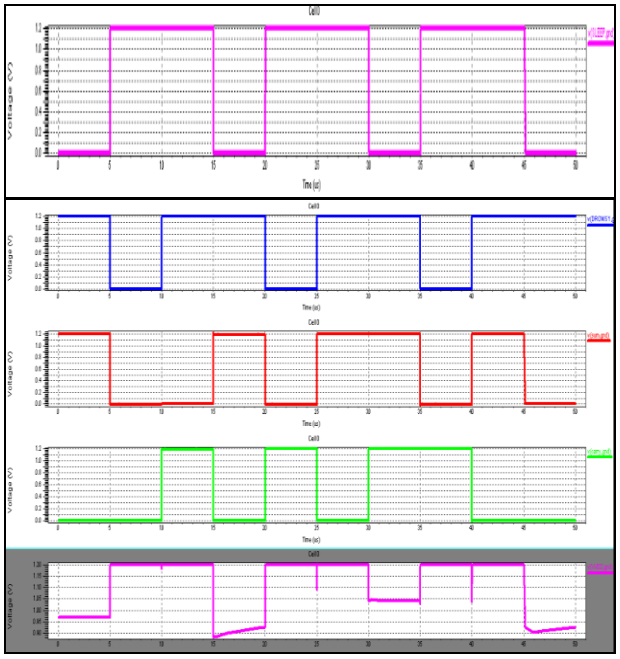

Fig.3 (e): Tri-mode header power gating

IV. POWER RESULTS

The power comparison is done with the simulation tool and the efficient technique is identified.

Scheme	Average power consumed (mW)	Minimum power consumed (µW)	Maximum power consumed (mW)
Three-step wake-up	11.329	614.795	54.625
Tri-mode footer	1.123	133.439	35.139

Table : Power Comparison

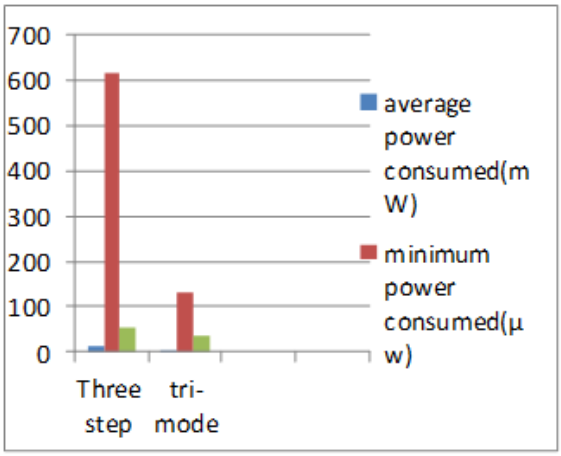

Fig.3 (f): Power Consumption graph

V. CONCLUSION

Thus the above results show that the power consumption gets reduced when tri-mode power gating circuits are used with lesser number of transistors and the future work includes the analysis with multi-mode following for the same and perform the comparisons to show the efficient techniques.

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