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RESEARCH ARTICLE OPEN

Frequency Stability Analysis of 9-stage Ring Oscillator in CMOS 45nm Technology using Cadence Tool

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ABSTRACT:
This proposed paper focuses on design and analysis of a nine stage Ring Oscillator in terms of frequency stability. For a ring oscillator, accuracy is very important. A 9-stage ring oscillator is designed and simulated using 45nm CMOS process technology. The input control voltage is varied from 0.5V to 1V to examine the frequency stability and power consumption of the circuit. The measured output frequency is 2.384 GHz and output power of 0.223µW.
Index Terms: *CMOS, Oscillator, frequency stability, Cadence Tool*

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I. INTRODUCTION

The main function of Oscillator is to generate clocks in digital systems. Ring oscillators are preferred over other oscillators because of its simple architecture, ease of implementation, capability of generating high frequency oscillators, integrated nature and compatibility with different standards. Periodic pulses, square and sine signals, oscillating signals can be generated using Oscillators. The ring oscillators do not have the complication of the on-chip inductors required for the LC oscillators and hence the chip area is reduced. The proposed is an inverter based ring oscillator and such inverter based oscillators are also known as single-ended ring oscillators. These oscillators consist of odd number of inverter stages connected in a loop and the output of the last inverter is fed back to the first stage of the loop. These intermediate stages and their corresponding time delays they produce are responsible for the output of the entire circuit. CMOS inverter is the combination of MOS transistors i.e. pmos and nmos, where pmos is called as pull-up network and nmos is called as pull-down network.

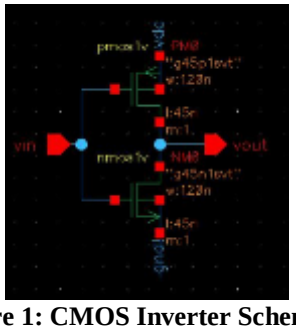


Figure 1: CMOS Inverter Schematic

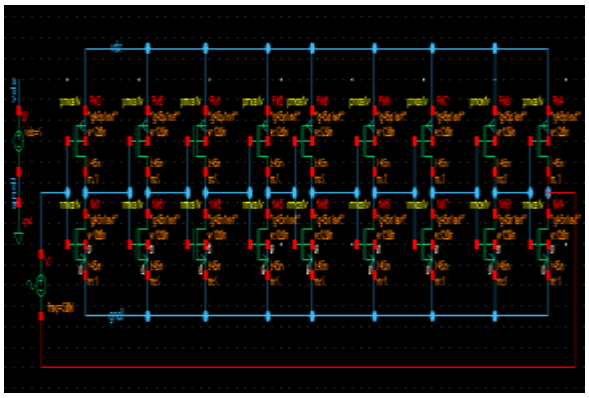
II. RING OSCILLATOR

Ring oscillator consists of a number of gain stages in a loop. The odd number of inverters in the circuit forms a closed loop with the positive feedback and is called a ring oscillator.

The oscillation occurs if the circuit contains multiple stages [2]. Search topology is considered undesirable because that leads to inadequate phase margin in opamps [3]. The architecture of 9 Stage ring oscillator is shown in figure 1. The oscillation frequency is given by

$$f_{osc} = 1/n(t_{PHL} + t_{PLH})$$

where t_{PHL} and t_{PLH} are the intrinsic propagation delays of the inverter. Assuming that the inverters are identical and n(odd) is the number of inverters in the ring oscillator [3]. The circuit exhibits positive feedback near zero frequency due to the signal inversion through each common-source stage which results in latch-up rather than oscillations [2]. Since the ring oscillator is self starting, it is often added to a test portion of a wafer to indicate the speed of a particular process run. The sum of the high-to-low and low-to-high delays is used to calculate the period of the oscillation because each inverter switches twice during a single oscillation period [3].



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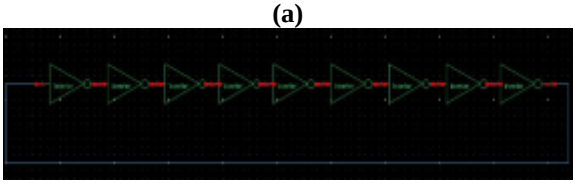


(b)

Figure 2: A 9-stage ring oscillator schematic

The circuit must satisfy the Barkhausen criteria in order to provide sustained oscillations, should provide unity voltage gain and must have a phase shift of 2π. The DC inversion provides a phase shift of π and the remaining π phase shift is divided equally among the stages in ring oscillator, so each delay gives phase delay of π/N, where N is number of stages in oscillator. The frequency of the N-stage ring oscillator is given by [1].

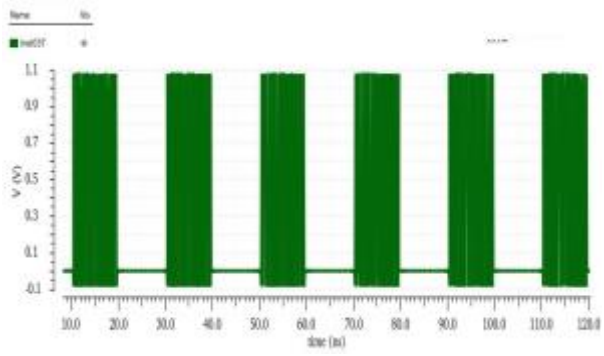
$$f = 1/ 2N_{td} \quad (1)$$

The delay is calculated using this equation and then the frequency of the ring oscillator is calculated with the help of the obtained results. Since identical inverters are used, the capacitance on the inverter's input or output is the sum of an inverter's input capacitance with the inverter's output capacitance as shown below

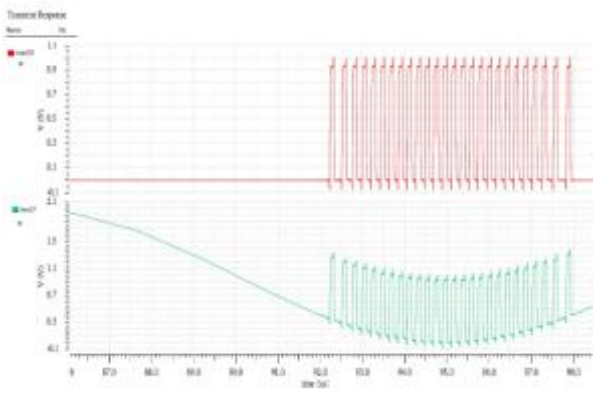
$$C_{out} = C_{oxp} + C_{oxn} + (3/2)\,(C_{oxp} + C_{oxn}) = (5/2)\,(C_{oxp} + C_{oxn})$$

III. SIMULATION RESULTS

For a ring oscillator, an input voltage of 0.7V is applied for a small period of time and the voltage is varied from 0.7 v to 1.3 volts and the results are observed. The transient analysis for the period zero to 200ns is performed with an input frequency of 50 MHz. The transient response of 9-stage ring oscillator during a period of 0 to 200ns is shown in figure 3.

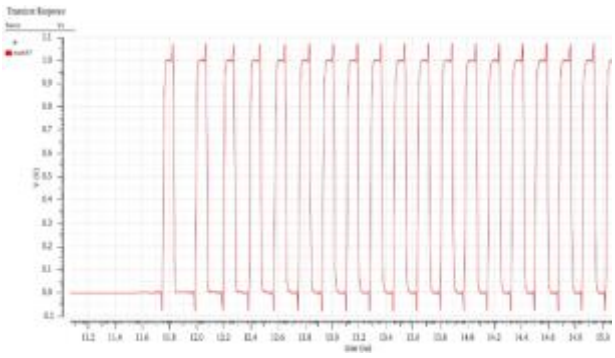


(a)



(b)

The oscillations produced by the ring oscillator with respect to sine signal of frequency 50Hz are observed here.



(c)

Figure 3: Transient Response of a 9-stage ring oscillator

The output of a 9-stage ring oscillator at every stage is also observed and the plotted simulation results are shown in figure 4.

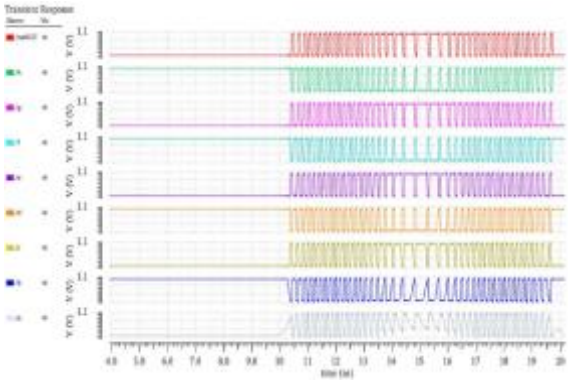


Figure 4: Transient Response at every inverter output of a 9-stage ring oscillator

The Variations observed in output parameters like frequency, power consumed, output current and bandwidth due to changes in input control voltage are tabulated as shown in the following table 1.

Control Voltage (V)	output freq (GHz)	output power (uW)	output current (uA)	Band Width (Hz)
0.5	2.267	0.545	0.545	10.03E-12
0.6	2.381	0.285	0.261	10.72E-12
0.7	2.384	0.223	0.209	36.90E-12
0.8	2.234	0.312	0.2935	37.17E-12
0.9	2.029	0.110	0.0994	37.74E-12
1.0	1.821	0.2325	0.2325	50.86E-12

Table 1: Variations observed in output parameters due to changes in input control voltage

The power consumed by the designed 9-stage ring oscillator is observed to be minimum at input control voltage of 0.7V from the analysis table with an output frequency of 2.384GHz..The power consumption is 0.223µW with an output current of 0.209µA. The bandwidth is observed to be 36.90E-12 for the same input control voltage of 0.7V.

IV. CONCLUSION

A 9-stage ring oscillator has been designed and analysis is performed using Cadence tool at 45nm CMOS process technology and simulation results in terms of transient response is also verified. The performance analysis based on output frequency, delay, and power consumption were measured. In a ring oscillator, the frequency and power consumption are in proportion with the supply voltage and the delay was inversely proportional. The power consumed by the designed 9-stage ring oscillator is observed to be minimum from the analysis in a certain frequency range.The power consumption is 0.223µW with a measured output frequency of 2.384 GHz.

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