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Design analysis of CNTFETs based Full Adder using CVSL

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ABSTRACT
In this paper, the design analysis, implementation and comparison of different types of full adders is done. The adders being a very important basic logic functional block are required in many complex and high end circuits. Also with the growing trend for nanotechnology, it has become mandatory to reduce the circuit size at every possible step. One such initiative is the adoption of the carbon nanotubes as these have size very small as compared to the Silicon based CMOS transistors. Also when these nanotubes are implemented along with the cascade voltage switch logic, the result is as desired. In this research work, full adder circuits are designed and implemented using different channel material and logics. The circuits designed are the Full Adder using CMOSFETs that use the Silicon substrate as the channel material and Carbon nanotubes based Full adder that uses the Carbon nanotubes field effect transistors. Both the circuits are implemented using the cascade voltage switch logic. These circuits are compared with the standard library Full adder using delay, power consumption, and transistor count as the parameters for comparison. It was found that the CNTFETs based Full adder using CVSL is more efficient with 50% less power consumption and 48.9% less delay when compared with CMOS based full adder that too using the CVSL.

Keywords **-** Circuit Simulation, CNTFETs, CVSL, Full Adder, time delay, power consumption.

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I. INTRODUCTION

The Adders are the very important logic circuit in the electronic world. These are considered as one of the most important building block for any type of circuit. The addition logic forms the basis for almost all the small or high end complex circuits that are used in the designing of the electronics circuits or devices [1]. Thus enhancement of this logic unit will help in enhancing the overall the performance of the arithmetic unit in the whole, which will give us a high performance circuits. The performance parameters that are most important in the designing of any electronic circuit are speed, power consumption, on chip area, delay, portability, reliability and many others. Power consumption and delay being the most important among all. Thus in designing of any circuit, the main focus is always on minimizing these two parameters. The full adder is basically the addition operation of three bits together [2]. This is different from half adder as it performs the operation of adding only two bits and does not have the concept of carry. This is the reason of it being called the full adder as it also adds the carry that is being generated in the previous addition. It adds two bits which are the inputs and the third bit being the carry of the last addition of two bits. The two outputs that are being generated are the sum and the carry. The sum here is the result of the addition of bits and carry will act as the third input bit for next addition operation. The basic logic diagram of the full adder is as shown below in the figure 1 [3].

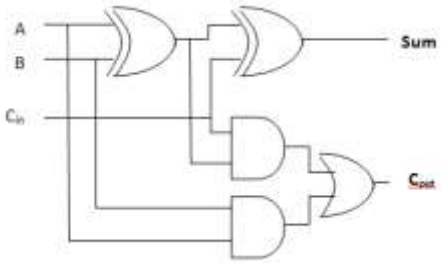

Figure 1: Full Adder

As is seen from the figure 1, A and B are the two input bits and C_{in} is the input carry that is forwarded from the last addition operation. The two outputs generated are the Sum and C_{out}. The circuit of full adder is performs operation in two parts, one generates the summed output and the other part takes forward the carry generated during this summing operation and take it forward towards the input for next cycle of addition. The Boolean expression for the sum and carry operations are as shown below in equation 1 and 2 respectively.

Sum = $A \oplus B \oplus C_{in}$ (1)

Carry (C_{out}) = $A.B + A.C_{in} + B.C_{in}$ (2)

The truth table for the full adder operation is as shown below in table 1 [4].

Table 1: Full Adder Truth Table

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. PROPOSED LOGIC

The logic that is used in this work for the implementation of the full adder is the cascade voltage switch logic. The short for this is CVSL. This is a very efficient type of differential logic. In this logic, both the true and complementary form of the inputs is required for the functionality [5]. The basic cascade voltage switch logic is as shown below in figure 2.

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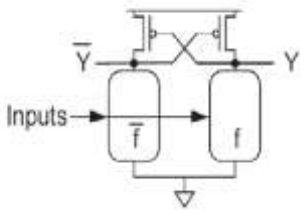

Figure 2: Basic CVSL

As is seen, the cross coupled network pair of pull up devices is connected to the NMOS structure. It has a pair of N pull down trees which are identical to each other. Here the pull down network is depicted by f, which evaluated the logic while the f bar evaluated the complement of the logic by making use of the inverted inputs applied [6]. The working logic is such that whenever the input is given, one of the two networks will be in ON state and other will be in OFF state. The active network will make the output to go to LOW level which in turn will make the PMOS transistor ON and will pull the second output to HIGH level. Similarly when the output of complementary network goes to HIGH state, the second PMOS network will got to OFF state. Thus at anytime, only one network will be ON, this will help in no power dissipation. Also this will lead to minimal delay which will lead to high speed of the circuit. Another advantage of using CVSL is that it helps in decreasing the number of transistors to be used, thus reducing the chip area [7].

III. CARBON NANOTUBE FIELD EFFECT TRANSISTORS

The Carbon nanotubes field effect transistors, short for CNTFET, are most likely similar in structure to the conventional complementary metal oxide semiconductor (CMOS) transistors [8]. The major difference lies in the material of the channel used for the construction of the CNTFET. In conventional CMOS based transistors, Silicon substrate is used as the channel material, whereas in the CNTFET, the carbon naotubes are used as the material for the construction of the channel. The carbon nanotubes are the tube like structure having cylindrical shape. These sheets are made up using the graphene,which is derived from Carbon. The Carbon atom is available in many different forms and dimensions (0D, 1D, 2D, 3D). The low dimensional (0D, 1D and 2D) allotropes are known as the nanomaterial. The 2-D material of graphite allotrope is known as graphene [9]. The carbon nanotubes are formed by rolling these graphene sheets into a cylindrical shape. The structure of nanotube and the graphene is as shown below in figure 3.

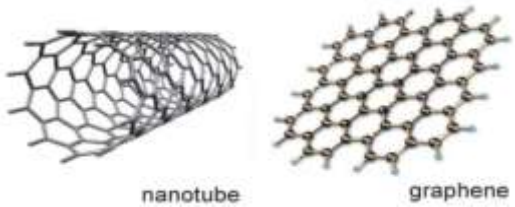

Figure 3: Structure of Graphene and nanotube.

These carbon nanotubes have many different forms and characteristics depending upon the angled ay which these sheets are rolled up. This is known as the Chirality [10]. Also they have different types of structures that may vary in thickness, number of layers, length. If the carbon nanotube has only 1 layer of graphene, it is known as **Single walled Carbon Nanotubes (SWCNTs)**. If it consists of two layers of graphene, then it is called as **Double walled Carbon Nanotubes**. And if it has multiple layers of graphene cylinder, then it is known as **Multi walled Carbon Nanotubes (MWCNTs).** These types of carbon nanotube are as shown below in figure 4, a, b, and c respectively for single, double and multi walled carbon nanotubes [11-12].

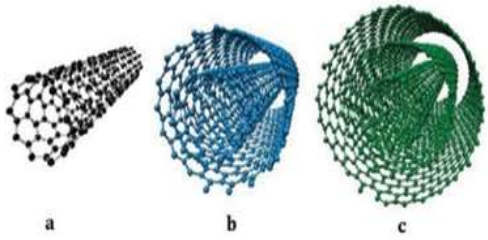

Figure 4: Different structures of CNTs.

The carbon nanotubes field effect transistors are constructed usin these nanotubes as the channel material. The basic structure of the CNTFET is as shown below in figure 5.

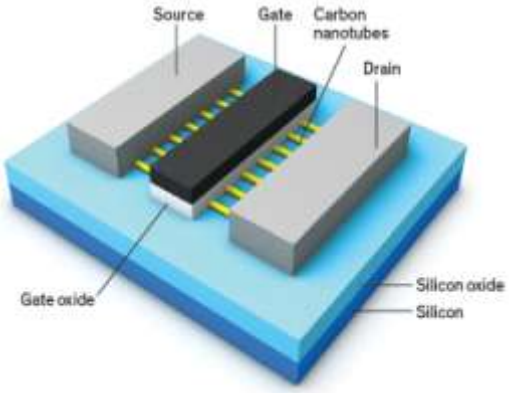

Figure 5: Structure of CNTFET

As is seen, the structure is identical to that of the CMOS transistors, the only difference being in the material of the channel used which is carbon nanotubes [13]. It has 3 terminals, source, drain and gate. The current enters through the source and leaves from the drain terminal. The gate is being used as the controller of the flow of current in the circuit [14]. Despite of so much similarity, there is a huge difference in the functionality, characteristics and performance of the CNTFETs. CNTFETs are much stronger, small in size, reliable than the CMOS transistors. Also they have helped in coping up with the short channel effects, `leakage current issue. Along with this they have high transconductance, great electron mobility, temperature resistant. They have proved to be a reliable substitute for the conventional CMOS transistors for almost all the applications. Also CNTFETs will give a push for moving towards the nanotechnology due to their nano size [15-16].

IV. CVSL BASED PROPOSED DESIGNS

The design and implementation of the full adder is done using the cascade voltage switch logic. There are two types of full adder designed in this paper. The transistor bases used are the carbon nanotubes based carbon nanotubes field effect transistor and the Silicon based CMOS transistors. Both the circuits are designed and implemented in the Cadence Virtuoso simulator. The schematic for the CMOS is constructed using the 45nm technology and 32nm Stanford CNTFET library for the CNTFET based full adder. The first circuit for full adder taken into consideration is the full adder present in the standard gpdk 45nm standard cell library. It is made functional using the suitable biasing. The circuit is as shown below in figure 6.

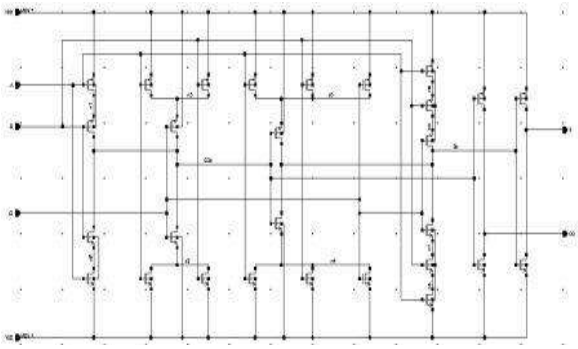

Figure 6: Standard 45nm Full Adder

The next circuit that is designed is the cascade voltage switch logic based full adder in CMOS. This circuit is as shown n figure 8 below. As is seen in the circuits, in the implementation of the cascade voltage logic, we require both the true and complementary form of the inputs. Also it can be seen from the circuit, as per the logic of cascade voltage, we get two outputs from the circuit that too in one cycle. These outputs are also in true and complementary form. As is the logic of full adder, it consists of total three inputs, two being the raw inputs and third is the output carry generated during the previous addition operation. The two outputs generated are the sum and the carry.

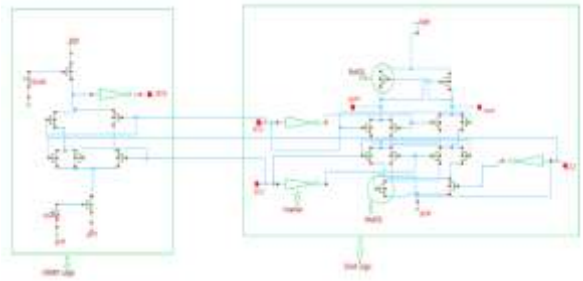

Figure 8: CVSL based Full Adder

The circuit for the inverter is as shown below in figure 9. In the circuit shown above, the symbolic representation of the inverter logic gate is used.

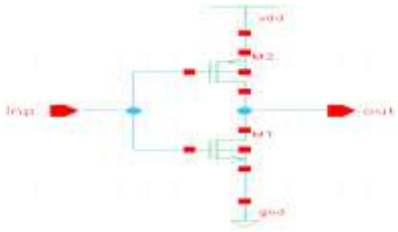

Figure 9: Inverter circuit used in CVSL based Full Adder

Now the next proposed circuits is the cascade voltage switch logic implementation of the full adder on the carbon nanotubes based field effect transistors. The circuit designed is as shown below in the figure 10. As is seen the implementation gives

the dual outputs that are complementary to each other. Suitable biasing is done for the complete functionality of the circuit.

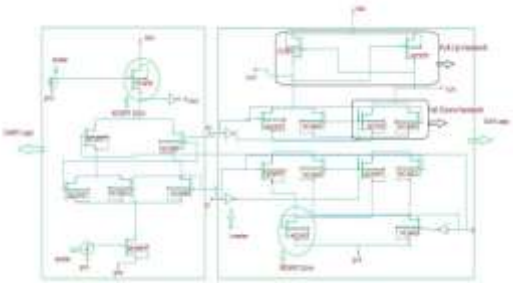

Figure 10: CNTFET based Full Adder using CVSL ADDED

Similar to the operation of CMOS based full adder, the CNTFET based full adder also have same set of inputs and outputs. In the circuit shown above, the symbolic representation of the inverter logic gate is used. The CNTFET based implementation of the inverter logic is as shown below in the figure 11.

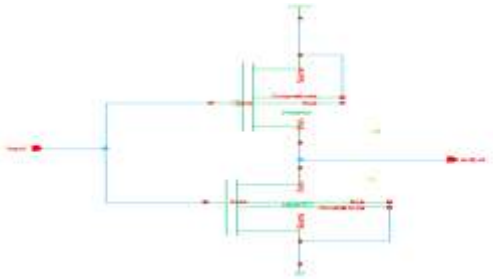

Figure 11: CNTFET based Inverter circuit used in Full Adder

V. RESULT ANALYSIS

The simulation for all the circuit designed is done in the Cadence Virtuoso simulator. The specifications and parameters are kept identical so that the symmetry in the analysis is maintained. The waveforms for all the circuits are obtained by proper simulation. The corresponding waveform for the full adder from the standard cell library is as shown below in the figure 12. The output waveform consists of the three inputs and the two outputs generated, sum and the carry.

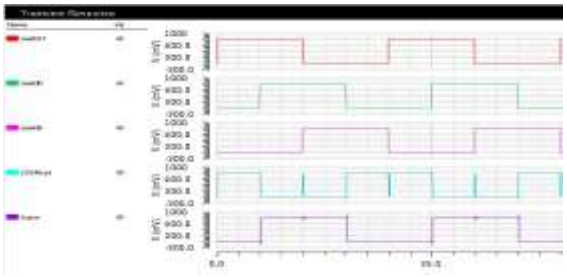

Figure 12: Standard Cell Full Adder Waveform

Now the simulation outputs for the proposed design of full adder are as shown below in figure 13 and 14. The simulation result for the CMOS based full adder based on cascade voltage switch logic is as shown in figure 13 and the CNTFET based full adder implementation again using cascade logic is as shown in figure 14. For both the waveforms, all three inputs and two outputs are plotted.

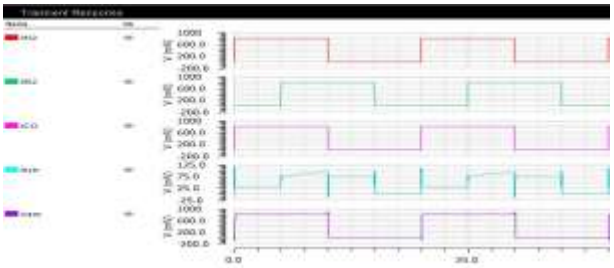

Figure 13: CVSL Full Adder output waveform.

Figure 14: CNTEFT based CVSL Full Adder output waveform.

For the purpose of analysis, all these circuits and the waveforms are designed and compared using a set of parameters. These are the power consumption, delay, the power delay product, and the transistor count. These parameters are observed for both CMOS and CNTFET based circuits. The observations results are summed up in a tabular form. This is as shown below in table 2.

Table 2: Performance analysis of Full Adder

Parameter	**Conventional Full Adder**	**CMOS based CVSL Full Adder**	**CNTFET based CVSL Full Adder**
Power (W)	26.461E-12	17.865E-12	8.818E-12
Delay (s)	112.31E-12	69.81E-12	35.64E-12
PDP	2.747E-21	1.247E-21	3.14E-22
No. of Transistors	29	27	27

It is very much clear from the observations made in the above table that the power consumption in case of the conventional standard cell full adder is 26.461pW. This when compared with the CMOS based full adder using the CVSL is very high, which is only 17.86pW. Now both these value becomes high when are compared with the CNTFETs based full adder. The power consumption in case of the CVSL implementation of full adder in CNTFETs

based circuit is only 8.818pW. Now the next parameter is the delay. In case of the standard cell full adder, the delay occurring in the circuit is 112.31ns, while in that of the CMOS based circuit is almost half of this which is 69.81ns. The value further reduces when the implementation is done on the CNTFETs circuit. The value comes out to be only 35.64ns which is considerably low. Also the number of transistors is reduced from 29 to 27 when CVSL is implemented. The analysis is summarized in the graphical form and is shown below in figure 15.

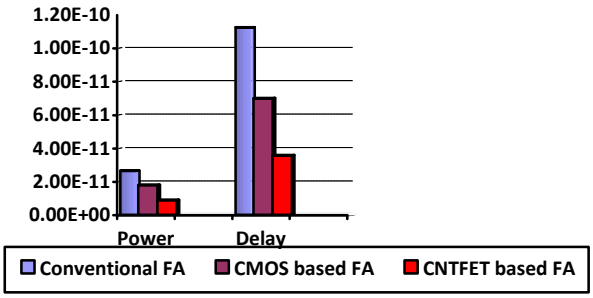

Figure 15: Performance analysis of Full Adder

VI. CONCLUSION

In this research work, the logic of full adder is designed, simulated, analysed and compared using a set of parameters. The observed values are tabulated in the table 1. It is clearly seen from the tabulated values that the power consumption for the CMOS based CVSL full adder is 32.4% less than that of the conventional standard full adder while this when compared to the CNTFET based full adder, it was found that the power consumption is exactly one-third of the standard cell full adder which is 66.6% less. Now for the delay, it was found that CMOS based design have 42.5% less and CNTEFT based full adder has 68.26% less delay than he conventional full adder. The transistor count is also reduced when CVSL is implemented in the circuit. Also when both CVSL designs were compared, it was found that the carbon nanotubes based CVSL design has 50% less power consumption and 48.9% less delay in comparison with the CMOS based CVSL design. Therefore, it is very much apparent that the most efficient design among all is the carbon nanotubes based full adder circuit implementing cascade voltage switch logic. Thus the CVSL in combination with the CNTFET is a benchmark achievement in the design of the electronic circuits. This work can be further taken up to high end complex circuits for efficient and high performance circuit design with less power and high speed.

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