

An Area Efficient and High Speed Reversible Multiplier Using NS Gate

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ABSTRACT

In digital computer system a major problem has been found that the Power dissipation which leads to bring some research on the methods to decrease this Area efficient, high speed. This is the main cause to give birth to reversible computing systems for digital computers and designs. Reversible computing is the path to future computing technologies, which all happen to use reversible logic. In addition, reversible computing will become mandatory because of the necessity to decrease power consumption. Reversible logic circuits have the same number of inputs and outputs, and have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. Consequently, a computation is reversible, if it is always possible to uniquely recover the input, given the output. Each gate can be made reversible by adding some additional input and output wires if necessary. The main aim of this reversible computing is to lower the power dissipation, area efficient and high speed and some other advantages like security of data and prevention of errors etc... Reversible logic has so many applications low power CMOS, nanotechnology, DNA computing and quantum computing. There are two primary design implementations in this study which are the major spotlights. The first one is reversible design gate and the second one is multiplier design using reversible gates. In this manuscript we have implemented a $8 * 8$ reversible design called "NSG(Non linear Sign Flip)". The total project is implemented in Xilinx 14.7 ISE with Spartan 3E family.

Keywords: Low Power Consumption, Reversibility, NSG, Constant Input, Garbage Output, ALU.

I. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least $K \ln 2$ joules, where $K = 1.3806505 * 10^{-23} \text{m}^2 \text{kg}^{-1} \text{K}^{-1}$ (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components In 1973, Bennett showed that $K \ln 2$ energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Reversible logic supports the process of

running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation become Information-lossless

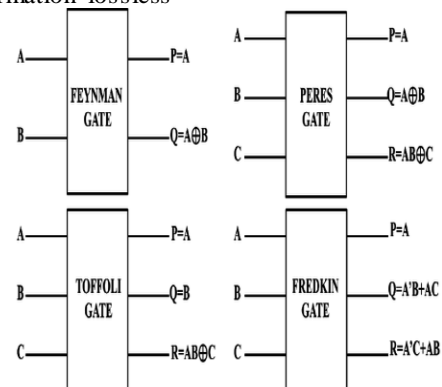


Figure: The Basic Reversible Logic Gates.

Energy loss is a very important factor in modern VLSI design. Irreversible hardware computation results in energy dissipation due to information loss. R.Landauer [1] has shown that for irreversible logic computations, each bit of information lost generated $KT\ln 2$ joules of heat energy, where K is Boltzmann's constant and T is the temperature at which computation performed. Reversible logic circuit does not have loss of information and reversible computation in a system can be performed only when the system consists of reversible gates. C.H.Bennet [2] showed that $KT\ln 2$ energy dissipation would not occur if the computation is carried out in a reversible way. Reversible logic is very crucial for the construction of low power, low loss computational designs which are very essential for the design process of arithmetic circuits used in quantum computation, Nano-technology and other low power digital circuits.

Lately, quite a few researchers have been paying their attention on the design, simulation and synthesis of proficient reversible logic circuits. The vital reversible gates [3] used for reversible logic synthesis are Feynman Gate and Fredkin gate [3, 4]. Reversible logic is emergent and drawing attention in the recent past due to its uniqueness i.e. less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. The NS Gate [5] i.e. "NSG" can singly be implemented in all logical Boolean operations. Reversible logic has publicized possibilities to have widespread purpose in upcoming emerging promising technologies such as quantum computing, optical computing, quantum dot cellular automata in addition to ultra-low power VLSI circuits, DNA computing to generate zero power rakishness under ideal conditions. In Proposed system, there exists a design of multiplier and adder units by number of reversible gates.

In This design, we are using only one reversible gate called NSG gate. By using this gate number of operations will be performed by only single gate and the garbage outputs also minimized. In this paper, we are also proposed a 8-bit Multiplier unit. Multiplier unit is an inevitable component in many digital signal processing (DSP) applications involving multiplications. Multiplier unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic

determines the execution speed and performance of the entire calculation. The multiplier and adder unit will be designed by NSG gate. The simulation output is verified using Xilinx ISE 14.7.

II. REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits. The number of Reversible gates (N): The number of? reversible gates used in circuit. The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function. The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility. Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates ($1*1$ or $2*2$) required to realize the circuit. A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

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III. 8-BIT MULTIPLIER UNIT USING CONVENTIONAL MULTIPLIER

A Multiplier unit having the sum of the earlier consecutive products. The inputs from the Multiplier will be obtained from the memory location and it will be given to the multiplier block. The design contains 8 bit modified multiplier, 16 bit ripple carry adder and a shift register. In multimedia information processing, DSP applications and various other applications, the Multiplier operation is the key operation. We are using the conventional Multiplier in the above Multiplier unit. The conventional multiplier of width $N \times N$ bits will generate the N number of partial products. The partial products are generated by bit wise AND in one multiplier bit with another multiplier. Hence, the $N \times N$ bit multiplier uses $2N$ multiplications and N -Adders in the architecture of Conventional multiplier.

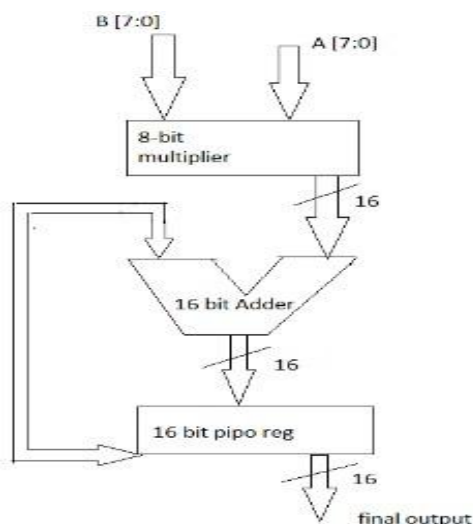


Figure: Multiplier Block Diagram.

IV. PROPOSED DESIGN

We have projected the reversible gate called NS gate “NSG” in this paper, which is a 4×4 one. The projected reversible NSG gate is shown in Figure.3.1. The analogous truth table of the gate is shown in Table I. It can be recognized from the Truth Table that the input pattern analogous to a particular output pattern can be completely resolute [5]. The NSG gate which is invented can perceive all Boolean logical operators. The input d , c , b and a are termed as input terminal 1, 2, 3 and 4 respectively and the output are termed as output 1,

output 2, output3 and output 4 correspondingly from first to last of the paper.

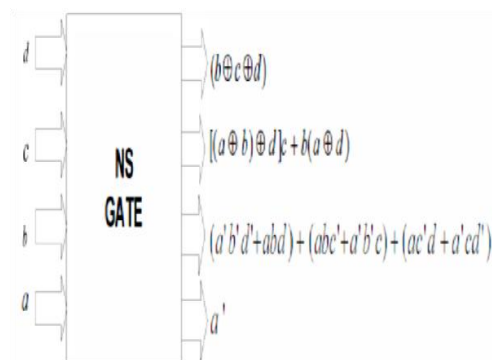


Figure: Proposed Reversible NS Gate.

Multiplier unit contains a multiplier, adder and register as mentioned above. In this paper, 8 bit modified Reversible NS multiplier has been used. The inputs of the Multiplier are obtained from the memory location and it will be given to the multiplier block. This will be very useful in the digital signal processor of the 8 bit. The input which is being fed from the memory location is 8 bit. Since the bits are vast and also ripple carry adder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The register is taken out or fed back as one of the input to the ripple carry adder. The above figure 2.1 shows [8] the basic architecture of Multiplier unit. The figures 3.2 shows the 8X8 NS multiplier.

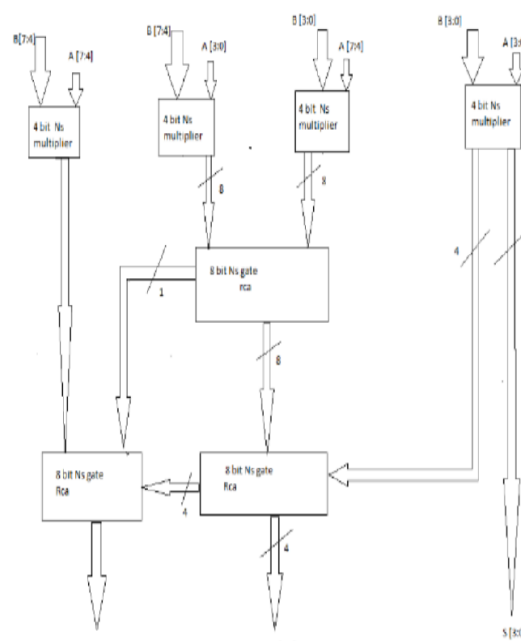


Figure: Multiplier architecture

V. COMPARISON RESULTS & ANALYSIS

The Reversible Multiplier unit simulated and synthesized using the Xilinx Design Suit13.2 with device family as spartan3E and device Xc3s100e5vq100. The simulation Results are verified by using Modelsim simulator i.e. given the input values are multiplier of a = 00110011 (51) and b = 00011110 (30) and get the final output is

final_out = 0000101111110100 (3060). The Figure 4.1 shows the model graph of Reversible Multiplier unit and Table I shows the comparison of conventional and Reversible Multiplier units.

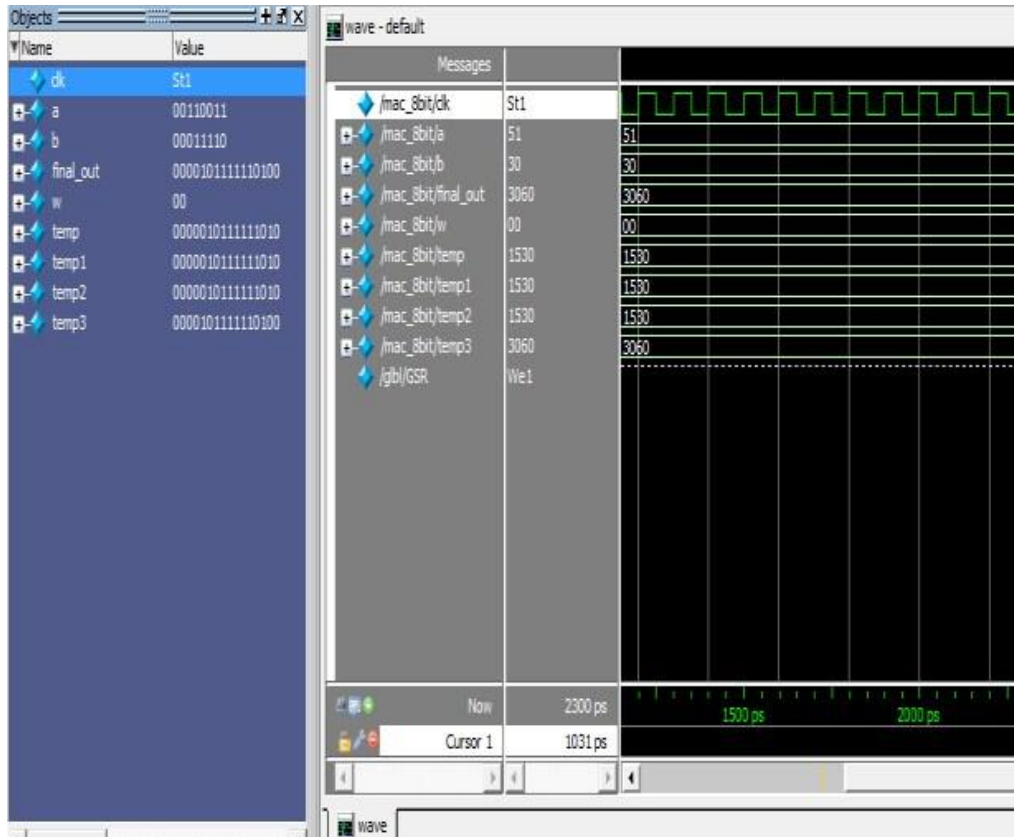


Figure: Simulation Results of Reversible Multiplier.

In the below table-I observe the number of (Look Up Tables) LUT's used in the general Multiplier unit is 214 which is higher than that of Reversible Multiplier unit. Here area occupied by the General Multiplier unit is higher than that of Reversible Multiplier unit. In reversible Mac unit, the multiplier we used was designed by using only

one reversible gate called as NS gate. So area occupied by reversible multiplier is low when comparing with normal multiplier used in general Multiplier unit. And also the delay produced by general Mac unit is very high when comparing with Reversible Multiplier unit.

Architecture	LUT's	Area (%)	Delay (ns)
EXISTED SYSTEM	214	11	36.286
PROPOSED SYSTEM	207	10	27.288

VI. CONCLUSION

Reversible multiplier can be designed with the different logical designs purposed in conventional combinational and sequential logic with the aim to improve the performance of computational units. Number of gates, Number of

garbage outputs, Number of ancillary inputs, is to be efficient to improve the performance of the reversible logic multiplier. Finally reversible logic gates are occupied less area and delay because it has a many to many input and output relations. So by using of these gates we can design any large

circuits with less components and it is the main advantage of reversible logic gates. Finally, this project presented an approach to the realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. 8×8 multiplication is realized with reversible NSG gate in an appropriate and enhanced manner. This unique approach multiplier is applicable for multipurpose applications in all domains.

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