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Effective Approach to Extract CMOS Model Parameters Based On Published Wafer Lot Data

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ABSTRACT
The VLSI electronic circuit designs have steadily grown in their capacity and complexity through the years. MOSIS fabrication services provide test data that designers can used to simulate their circuit designs. The provided test results are extracted from various lot wafers and BSIM3 or BSIM4 model card parameters in addition to technology parameters are provided. It may be cumbersome to ensure design functionality over the wide range of model set of parameters. In this paper, it is proposed to utilize the average model parameters to validate circuit design functionality. It can be shown through device characterization and simple circuit simulations that the average model parameters can provide a good representation of the wide range of supplied model parameters. This is specially attractive for students of circuit design classes where classroom and graduate research work were computing resources are limited. Utilizing average model parameters alleviate the need to run simulations over the large set of models from the fabrication facility.
Keywords: VLSI; Design; Automation; CAD; EDA; Higher Education, Circuit; Microelectronics.

I. INTRODUCTION

The VLSI electronic circuit designs have steadily grown in their capacity and complexity through the years. The circuit simulation based on technology test data is a core capability to ensure quality and functionality of circuit design. Established circuit design companies are well equipped with commercial and proprietary CMOS models. However, for educational institutes specially in developing countries the needs are massive. Circuit design students will have access to only published or granted set of CMOS device parameter models. One example provider of circuit manufacturing and model parameters is the MOSIS Integrated Circuit Fabrication Service[1]. MOSIS portal online site provides access to SPICE model parameter sets extracted through testing shuttles. The ability to enable circuit simulation as part of circuit design capability is critical to the whole circuit design and automation flow as desicribed by Osman et. al. with focus on developing country higher education institutes[2].

For teaching purposes, it is normal that a semiconductor modeling or circuit design class would require students to perform simulations using various circuit simulator tools. More advanced classes or project work would require class to complete circuit design projects going over steps of designing the circuitry, validating functionality, and in certain cases submit design for fabrication and test circuit performance post design and fabrication. Such task list would constitute the normal set of requirements for graduate level of research work.

The focus of this work is to scheme an approach that would enhance simulation capability for circuit design educational projects by extracting fewer set of model parameters to be used for design validity check. The approach would list technical steps to be followed to reach the minimum required parameter set that would enable circuit testing over the valid technology spectrum. It is also expected to enhance the simulation by providing a fewer set of model parameters needed for simulations by student and instructors. This approach is expected to lead to faster turn around time for school projects to complete and with more confidence on circuit simulations. Moreover, the approach would be attractive to educational firms where less number of simulations would be needed on these student projects, hence, better use of limited computational resources available to developing countries standard educational institutes.

The proposed approach will be described and detailed in the following sections. It will also be run over a set of MOSIS CMOS model parameters on various technologies.

II. DESCRIPTION OF MOSIS TEST RESULTS AND SPICE PARAMETERS

An example of fabrication services is provided by MOSIS Integrated Circuit Fabrication Service[1] which has a protal site that lists various test results extracted from many fabrication processes supplied to enable test chip designers from education institutes with circuit simulations. For this work, a list of test parameters were copied from MOSIS portal for processes 0.5um, 0.35um, 0.25um, 0.18um, and 0.13um. Model card were provided on level 49 BSIM3 which is level 7 when using PSPICE circuit simulator. Test results reported in this paper are from the 0.13um technology with a total of 140 NMOS device model cards, and 140 PMOS model cards.

```
.MODEL CMOSN1 NMOS (  LEVEL   = 7 VERSION = 3.1   TNOM   = 27   TOX   = 3.1E-9 XJ   = 1E-7   NCH   =
2.3549E17   VTH0   = 0.0423165 K1   = 0.3813948   K2   = -0.0429398   K3   = 1E-3 K3B   = -5.4914113   W0   =
2.842757E-7   NLX   = 8.587757E-7 DVT0W   = 0   DVT1W   = 0   DVT2W   = 0 DVT0   = 1.3517499   DVT1   =
0.1346369   DVT2   = 0.2573007 U0   = 433.1623269   UA   = -1.68513E-10   UB   = 2.595147E-18 UC   = 3.627474E-10
VSAT   = 1.996723E5   A0   = 1.9954199 AGS   = 0.7698052   B0   = 2.192287E-6   B1   = 5E-6 KETA   = 0.05   A1
= 7.984957E-4   A2   = 0.3 RDSW   = 150   PRWG   = 0.3438252   PRWB   = 0.1148206 WR   = 1   WINT   =
5.474932E-9   LINT   = 1.039388E-8 DWG   = 1.365899E-8   DWB   = -1.421557E-8   VOFF   = -1.629599E-3 NFACTOR
= 2.5   CIT   = 0   CDSC   = 2.4E-4 CDSCD   = 0   CDSCB   = 0   ETA0   = 2.742131E-6 ETAB   = -0.0105152   DSUB
= 4.04455E-6   PCLM   = 1.9827146 PDIBLC1 = 0.9615773   PDIBLC2 = 0.01   PDIBLCB = 0.1 DROUT   =
0.9985346   PSCBE1   = 7.935687E10   PSCBE2   = 5.002477E-10 PVAG   = 0.5388849   DELTA   = 0.01   RSH   = 7.1
MOBMOD   = 1   PRT   = 0   UTE   = -1.5 KT1   = -0.11   KT1L   = 0   KT2   = 0.022 UA1   = 4.31E-9   UB1   =
7.61E-18   UC1   = -5.6E-11 AT   = 3.3E4   WL   = 0   WLN   = 1   WW   = 0   WWN   = 1   WWL   = 0 LL
= 0   LLN   = 1   LW   = 0 LWN   = 1   LWL   = 0   CAPMOD   = 2 XPART   = 0.5   CGDO   = 3.74E-10   CGSO
= 3.74E-10 CGBO   = 1E-12   CJ   = 9.581078E-4   PB   = 0.9753695 MJ   = 0.4043404   CJSW   = 1E-10   PBSW
= 0.8 MJSW   = 0.5997932   CJSWG   = 3.3E-10   PBSWG   = 0.8 MJSWG   = 0.5997932   CF   = 0   PVTH0   =
1.666651E-3 PRDSW   = 3.233624   PK2   = 7.599199E-4   WKETA   = -2.992323E-3 LKETA   = 0.0331104   PU0   =
5.1738963   PUA   = -3.21747E-11 PUB   = 0   PVSAT   = 653.2294237   PETA0   = 1E-4 PKETA   = 8.356238E-4   )
```

Figure 1. Sample of model cards for NMOS devices with model names CMOSN1 from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted.

III. SIMULATION MODEL PARAMETERS PREPARATION STEPS

To validate circuit design functionality, one would need to run simulations using all of the reported models and ensure functionality is falling within required specifications. For example, if one uses the 0.13um from MOSIS portal, a 140 NMOS and PMOS model cards would be used to run circuit simulations and ensure functioanlity for all of the model cards. This pose a real challange to simulate circuit functionality and would require an abundance of resources to accomplish.

It is imperative to scheme a method to reduce required simulation runs without sacrificing circuit functionality. The following steps are proposed to tackle such challenge and enable designers to test functionality over the wide range of models provided by test data:

```
.MODEL CMOSN2 NMOS (  LEVEL   = 7 VERSION = 3.1   TNOM   = 27   TOX   = 3.2E-9 XJ   = 1E-7   NCH
= 2.3549E17   VTH0   = 0.0396554 K1   = 0.3658057   K2   = -0.0322543   K3   = 1E-3 K3B   = -2.451167   W0
= 8.01406E-7   NLX   = 1E-6 DVT0W   = 0   DVT1W   = 0   DVT2W   = 0 DVT0   = 1.433812   DVT1   = 0.1267043
DVT2   = 0.2429906 U0   = 455.7172913   UA   = -6.30664E-11   UB   = 3.188029E-18 UC   = 4.352734E-10   VSAT   =
1.660746E5   A0   = 2 AGS   = 1.0156223   B0   = 5.513384E-6   B1 = 5E-6 KETA   = 0.05   A1   = 1.158323E-3
A2   = 0.3000507 RDSW   = 150   PRWG   = -0.1949785   PRWB   = 0.2 WR   = 1   WINT   = 1.344912E-8
LINT   = 8.57538E-9 DWG   = 5.851826E-9   DWB   = -9.811963E-9   VOFF   = -1.437802E-4 NFACTOR = 2.5   CIT
= 0   CDSC   = 2.4E-4 CDSCD   = 0   CDSCB   = 0   ETA0   = 2.736004E-6 ETAB   = -0.0133399   DSUB   = 4.034666E-6
PCLM   = 1.9846072 PDIBLC1 = 0.9640054   PDIBLC2 = 0.01   PDIBLCB = 0.1 DROUT   = 0.9988769   PSCBE1   =
7.930138E10   PSCBE2   = 5E-10 PVAG   = 0.5367816   DELTA   = 0.01   RSH   = 6.8 MOBMOD   = 1   PRT   = 0
UTE   = -1.5 KT1   = -0.11   KT1L   = 0   KT2   = 0.022 UA1   = 4.31E-9   UB1   = -7.61E-18   UC1   = -5.6E-11
AT   = 3.3E4   WL   = 0   WLN   = 1 WW   = 0   WWN   = 1   WWL   = 0 LL   = 0 LLN   = 1   LW   =
0 LWN   = 1   LWL   = 0   CAPMOD   = 2 XPART   = 0.5   CGDO   = 3E-10   CGSO   = 3E-10 CGBO   = 1E-12   CJ
= 9.58142E-4   PB   = 0.9296269 MJ   = 0.3947908   CJSW   = 1E-10   PBSW   = 0.8 MJSW   = 0.3896111
CJSWG   = 3.3E-10   PBSWG   = 0.8 MJSWG   = 0.3886008   CF   = 0   PVTH0   = -1.290152E-3 PRDSW   =
9.0121815   PK2   = 1.586032E-3   WKETA   = 9.320148E-4 LKETA   = 0.0394768   PU0   = -4.2873558   PUA   =
4.19332E-11 PUB   = 0   PVSAT   = 653.2294237   PETA0   = 1E-4 PKETA   = -2.589568E-3   )
```

Figure 2. Sample of model cards for NMOS devices with model names CMOSN2 from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted

```
.MODEL CMOSN3 NMOS ( LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 3.2E-9 XJ = 1E-7 NCH =
2.3549E17 VTH0 = 0.0474349 K1 = 0.3755933 K2 = -0.0326732 K3 = 1E-3 K3B = 3.9388662 W0 =
1E-7 NLX = 9.516014E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.4512954 DVT1 = 0.1538308
DVT2 = 0.2283147 U0 = 435.021711 UA = -3.88398E-10 UB = 3.243607E-18 UC = 4.810495E-10 VSAT =
1.931402E5 A0 = 1.9928116 AGS = 0.7676187 B0 = 2.3777E-6 B1 = 5E-6 KETA = 0.05 A1 =
7.79429E-4 A2 = 0.3 RDSW = 150 PRWG = 0.3505365 PRWB = 0.1098466 WR = 1 WINT =
8.022373E-9 LINT = 1.03924E-8 DWG = 5.870869E-9 DWB = 1.038956E-8 VOFF = -0.0308797 NFACTOR =
2.5 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 2.753965E-6 ETAB = -0.0103481 DSUB
= 4.063875E-6 PCLM = 1.9769496 PDIBLC1 = 0.9713498 PDIBLC2 = 0.01 PDIBLCB = 0.1 DROUT = 0.9994665
PSCBE1 = 7.972806E10 PSCBE2 = 5.025876E-10 PVAG = 0.5362119 DELTA = 0.01 RSH = 6.7 MOBMOD =
1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18
UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = WWL = 0 LL = 0 LLN
= 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 3.74E-10 CGSO =
3.74E-10 CGBO = 1E-12 CJ = 9.581316E-4 PB = 0.9759771 MJ = 0.404514 CJSW = 1E-10 PBSW =
0.8002028 MJSW = 0.6 CJSWG = 3.3E-10 PBSWG = 0.8002028 MJSWG = 0.6 CF = 0 PVTH0 = 2.009264E-
4 PRDSW = 0 PK2 = 1.30501E-3 WKETA = 0.0114143 LKETA = 0.0250887 PU0 = 4.4729531 PUA =
1.66833E-11 PUB = 0 PVSAT = 653.2294237 PETA0 = 1E-4 PKETA = -6.687124E-3 )
```

Figure 3. Sample of model cards for NMOS devices with model names CMOSN3 from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted.

1. Download model parameters from MOSIS portal and save test results in a text file
2. Develop a utility to:

a) Extract the BSIM model card for NMOS and PMOS devices from test data file.

b) Process model parameters and save in CSV, Excell format, or any tabular format for later processing.

3. Compute BSIM model card using the mathematical function of minimum (MIN), maximum (MAX), and average (AVERAGE) value of all BSIM model parameters to produce new model cards.
4. Save the minimum, maximum, and average model parameter sets in their own model card with model name updated to reflect type of parameter set.
5. The average, min, and max model card can be used to run simulations to test circuit functionality.

```
.MODEL CMOSNMIN NMOS ( LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 3.1E-9 XJ = 1E-7 NCH
= 2.35E17 VTH0 = 0.013125 K1 = 0.2203486 K2 = -0.0831705 K3 = 1E-3 K3B = -10 W0 =
0.0000001 NLX = 5.81E-07 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.7405075 DVT1 = 0.121679
DVT2 = 0.0760517 U0 = 372.7539745 UA = -1.64E-09 UB = 2.39E-18 UC = 2.26E-10 VSAT = 54456.0
A0 = 0.1 AGS = 0 B0 = 2.93e-07 B1 = 0 KETA = -0.0199328 A1 = 0 A2 = 0.3 RDSW =
148.6773758 PRWG = -0.2 PRWB = -0.1200236 WR = 1 WINT = 0 LINT = 2.80E-09 DWG = -1.47E-
08 DWB = -3.73E-08 VOFF = -0.0836988 NFACTOR = 1.7361971 CIT = 0 CDSC = 2.4E-4 CDSCD =
CDSCB = 0 ETA0 = 0 ETAB = -0.0192992 DSUB = 4.03E-06 PCLM = 0.0763461 PDIBLC1 =
0.2222673 PDIBLC2 = 0.01 PDIBLCB = -0.1 DROUT = 0.925902 PSCBE1 = 78991210000 PSCBE2 =
5.00E-10 PVAG = 0.000172946 DELTA = 0.01 RSH = 3.4 MOBMOD = 1 PRT = 0 UTE = -1.
KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E
WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN =
LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 3.00E-10 CGSO = 3.00E-10 CGBO = 0 CJ = 0.00083574
PB = 0.8 MJ = 0.3947908 CJSW = 1E-10 PBSW = 0.8 MJSW =0.2172546 CJSWG = 3.3E-1
PBSWG = 0.8 MJSWG = 0.2172546 CF = 0 PVTH0 = -0.00373767 PRDSW = 0 PK2 = 0.000722611 WKET
= -0.0168505 LKETA = -0.0239663 PU0 = -5.2771597 PUA = -4.98E-11 PUB = 0 PVSAT = 12.976041
PETA0 = -0.0001 PKETA = -0.05 )
```

Figure 4. The minmum parameter model cards for NMOS devices named CMOSNMIN from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted.

```
.MODEL CMOSNMAX NMOS ( LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 3.3E-9 XJ = 1E-7 NCH
2.35E17 VTH0 = 0.0891106 K1 = 0.4574357 K2 = 0.006581333 K3 = 0.001002204 K3B = 11.036716
W0 = 4.81E-06 NLX = 0.000001 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.8962449 DVT1
0.2202769 DVT2 = 0.3403182 U0 = 462.3495227 UA = -6.31E-11 UB = 5.00E-18 UC = 6.05E-1 VSAT
200000 A0 = 2 AGS = 2.0640264 B0 = 7.68E-06 B1 = 0.000005 KETA = 0.050158 A1 = 0.105397
A2 = 1 RDSW = 150 PRWG = 0.5 PRWB =0.2 WR = 1 WINT = 3.01E-08 LINT = 1.38E-08 DWG
1.96E-08 DWB = 4.72E-08 VOFF = 0 NFACTOR = 2.5 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSC
= 0 ETA0 = 0.0101151 ETAB = 1 DSUB = 0.001292485 PCLM = 3.9763512 PDIBLC1 = 1 PDIBLC2 = 0.0
PDIBLCB = 0.1 DROUT = 1 PSCBE1 = 80000000000 PSCBE2 = 1.21E-06 PVAG = 0.5398298 DELTA = 0.0
RSH = 7.7 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-
UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 L
= 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 4.88E-10 CGSO
4.88E-10 CGBO = 0.000000001 CJ = 0.000959329 PB = 0.9869656 MJ = 0.5604981 CJSW = 2.52E-10 PBSW
= 0.99 MJSW = 0.6 CJSWG = 3.3E-10 PBSWG = 0.99 MJSWG =0.6 CF = 0 PVTH0 = 0.000842713 PRDSW
11.5791655 PK2 = 0.001958463 WKETA = 0.05 LKETA = 0.05 PU0 = 29.7807986 PUA = 3.09E-10 PU
= 9.70E-23 PVSAT = 2006.318 PETA0 = 0.000110348 PKETA= 0.004448585 )
```

Figure 5. The maximum parameter model cards for NMOS devices named CMOSNMAX from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted.

The proposed steps were executed on a the set of 140 model parameters from 0.13um with NMOS and PMOS models as well as from other processes. The min, max, and average cards are computed used the listed steps above. The model cards CMOSN1, CMOSN2, CMOSN3 are 3 sample model cards from the complete set of avaliable model cards are shown in Fig1., Fig2, and Fig3 respectively. The derived minimum parameter model card is derived and labelled with CMOSNMIN, and is shown in Fig. 4. The model card with maximum parameters model card and labelled with CMOSNMAX and is shown in Fig. 5. The average model parameters are computed and listed in the model card with label CMOSAVG as shown in Fig. 6. These model card are used with PSPICE circuit simulator for testing and analysis and the model parameter LEVEL is set to 7 as required by the simulator.

IV. SIMULATION AND ANALYSIS

To validate the extracted Min, Max, and Avgerge model cards accuracy and suitablity for circuit design and function testing, an experiment is devised with the following details:

```
.MODEL CMOSNAVG NMOS (  LEVEL  = 7 VERSION = 3.1  TNOM  = 27 TOX  = 3.18E-9 XJ  = 1E-7  NCH
+ 2.35E17  VTH0  = 0.049467694 K1  = 0.342605657  K2  = -0.03005055  K3  = 0.001000044 K3B  =
+.338059368  W0  = 2.01E-07  NLX  = 9.45E-07 DVT0W  = 0 DVT1W  = 0 DVT2W  = 0 DVT0  = 1.249306343
+VT1  = 0.157248832 DVT2  =  0.250724997 U0  = 434.264655 UA  = -4.95E-10 UB  = 3.56E-18 UC  =
+.31E-10  VSAT  = 161691.7625  A0  = 1.144061643  AGS  = 0.779744464  B0  = 4.38E-06 B1  = 4.84E-0
+KETA  = 0.037030822  A1  = 0.006343491 A2  = 0.392097627 RDSW  = 149.9765228  PRWG  = 0.300518243
+RWB  = 0.124658174 WR  = 1  WINT  = 9.74E-09 LINT  = 1.02E-08 DWG  = 5.42E-09 DWB  = 1.41E-08
+  VOFF  = -0.028415718 NFACTOR = 2.484046401  CIT  = 0  CDSC  = 2.4E-4  CDSCD  = 0
+CDSCB  = 0  ETA0  = 0.000501783  ETAB  = 0.218519938  DSUB  = 0.000206933  PCLM  = 1.659682388
+PDIBLC1 = 0.861948457  PDIBLC2 = 0.01  PDIBLCB = 0.064929156  DROUT = 0.996519893  PSCBE1 =
+9559942000  PSCBE2 = 3.60E-08 PVAG  = 0.41227375  DELTA  = 0.01  RSH  = 6.554285714 MOBMOD = 1
+RT  = 0  UTE  = -1.5 KT1  = -0.11  KT1L  = 0  KT2  = 0.022  UA1  = 4.31E-9  UB1  = -7.61E-18
+C1  = -5.6E-11 AT  = 3.3E4  WL  = 0  WLN  = 1 WW  = 0  WWN  = 1  WWL  = 0 LL  = 0  LLN
+ 1  LW  = 0 LWN  = 1  LWL  = 0  CAPMOD = 2 XPART = 0.5  CGDO = 3.85E-10  CGSO = 3.85E-
+0 CGBO  = 4.96E-11  CJ  = 0.000890833  PB  = 0.888723188 MJ  = 0.471696939  CJSW = 1.78E-10 PBSW
+ 0.820510135 MJSW = 0.414877851  CJSWG = 3.30E-10  PBSWG = 0.820510135  MJSWG = 0.414877851  CF
+ 0  PVTH0  = -0.000469729 PRDSW = 1.139909337  PK2  = 0.001390773  WKETA = 0.005086094 LKETA =
+.017343254  PU0  = 2.168917812  PUA  = 7.67E-12 PUB  = 2.84E-24  PVSAT = 888.8391865 PETA0 =
+.97E-05 PKETA  = -0.012664682  )
```

Figure 6. The average parameter model cards for NMOS devices named CMOSNAVG from the portal where 140 model cards NMOS and PMOS 0.13um Technology were extracted.

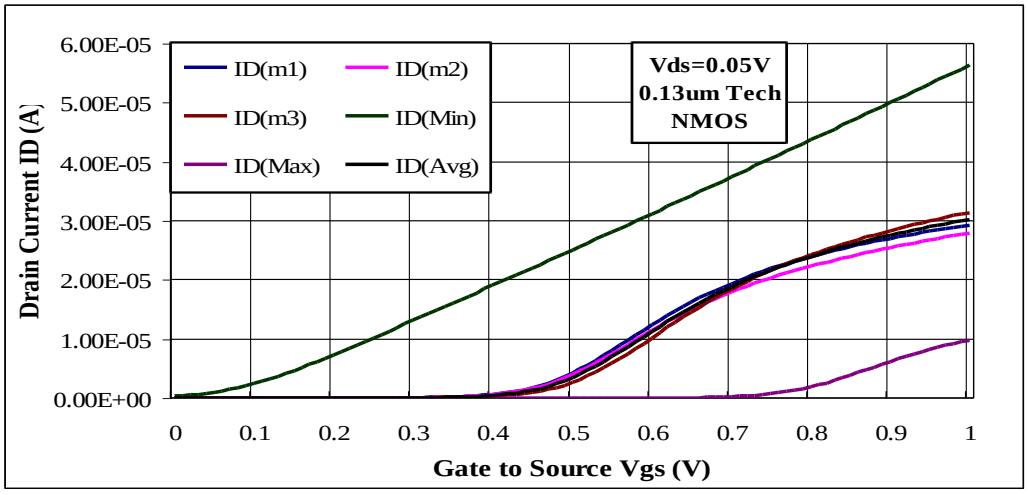


Figure 7: Linear region of NMOS device (0.5u/0.13u) at low Vds =0.05V and using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

1. Test validity over a single device (NMOS, PMOS) characteristics. The extracted models were used to simulate NMOS and PMOS:

A) drain current Ids,
B) drain conductance Gds,
C) and gate transconductance Gm
D) Sweep of drain to source (Vds) bias
E) and sweep of gate to source (Vgs) bias

2. A simple inverter circuit is also used to check model validity by testing inverter DC transfer charactistics.

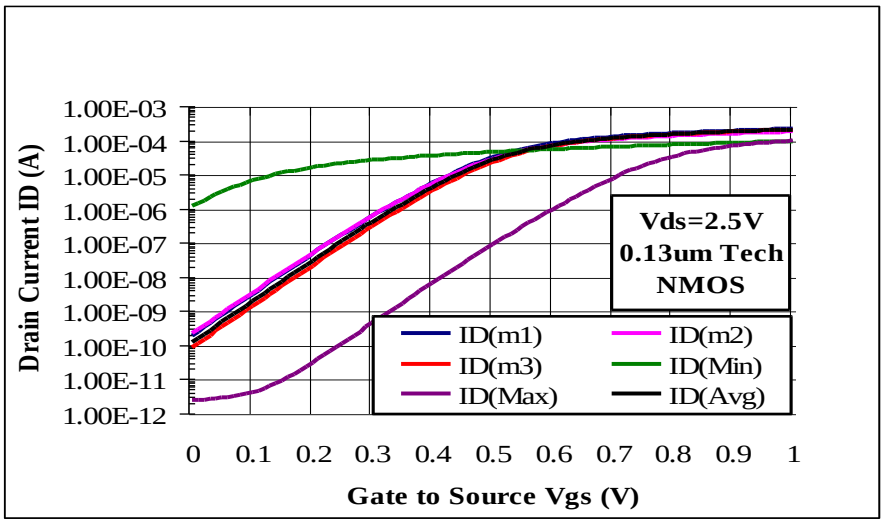


Figure 8: Linear region of NMOS device (0.5u/0.13u) at high Vds and using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

4.1. Single Device Characterization - NMOS

Fig. 7 and Fig. 8 show the linear Linear region of NMOS device (0.5u/0.13u) at low and high Vds using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

The NMOS device drain current characteristics is shown on Fig. 7 and The drain and gate conductance are also simulated using the computed models for NMOS device as shown in Fig. 8 and Fig. 9. From Fig. 7-10, it is noted that the CMOSNAVG model card tracks results from CMOSN1, CMOSN2, CMOSN3 results.

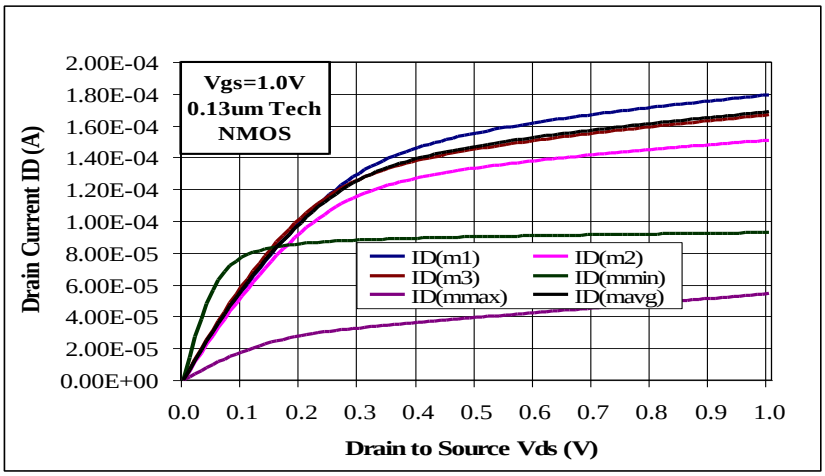


Figure 9: IV characteristics of NMOS device (0.5u/0.13u) at Vgs=1.0V and using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

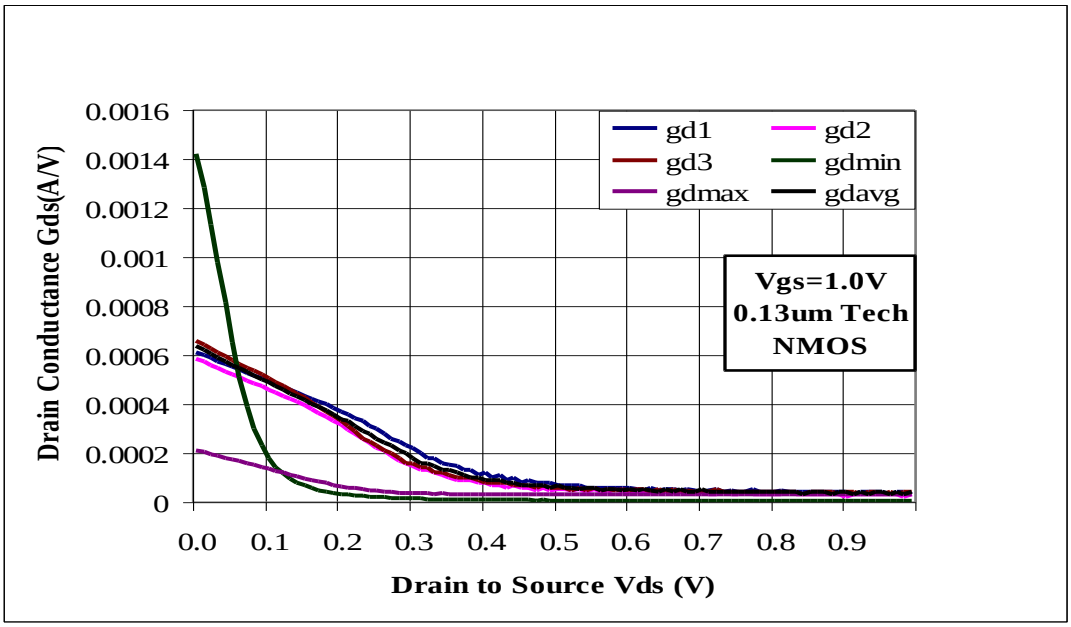


Figure 10: Drain conductance of NMOS device (0.5u/0.13u) at Vgs=1.0V and using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

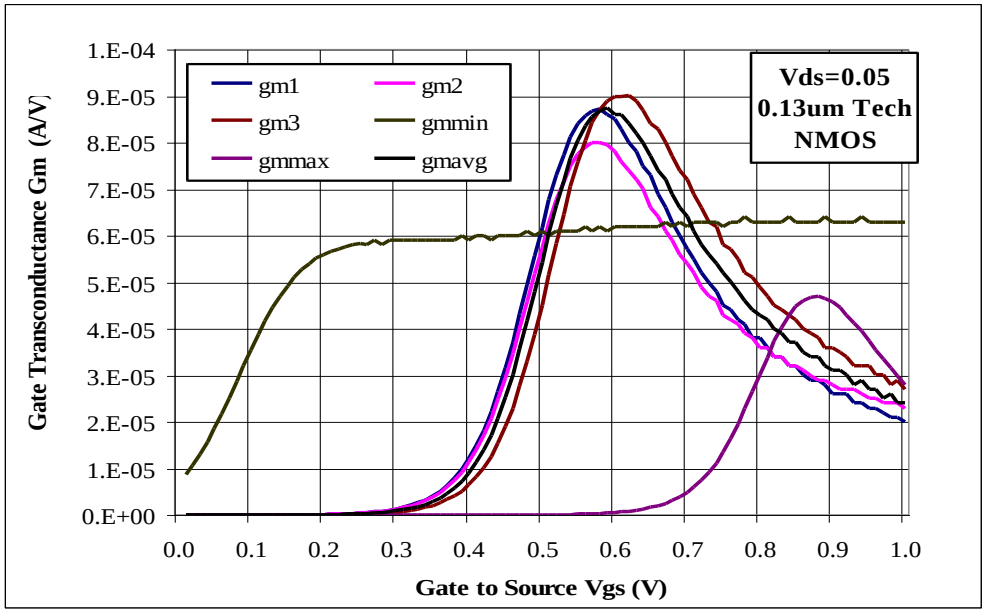


Figure 11: Gate transconductance of NMOS device (0.5u/0.13u) at Vds=0.05V and using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

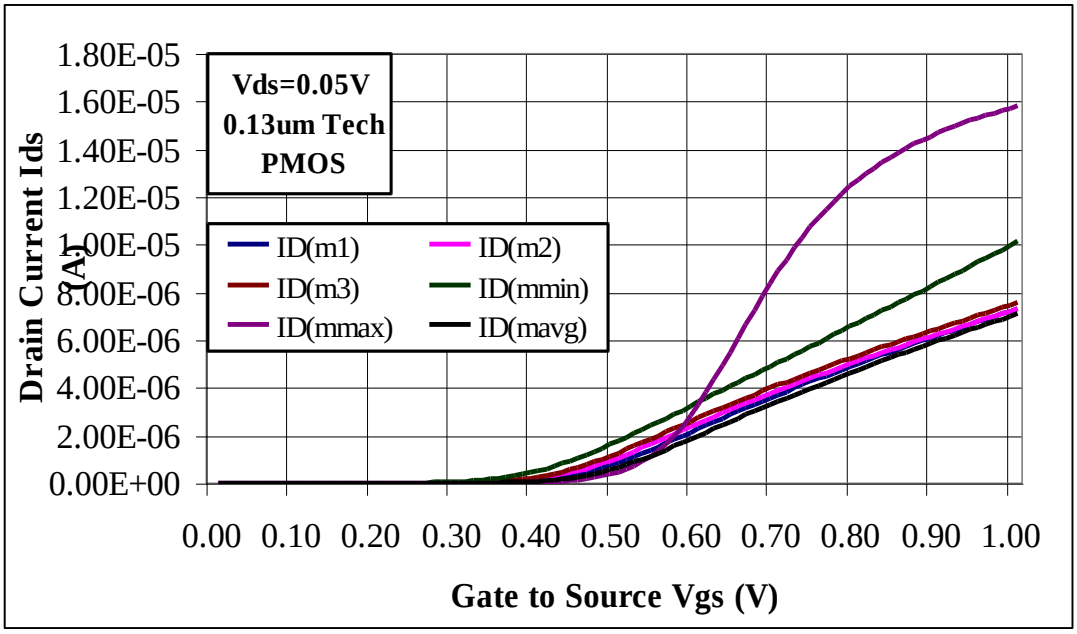


Figure 12: Linear region of PMOS device (0.5u/0.13u) at low Vds =0.05V and using model cards for CMOSP1, CMOSP2, CMOSP3 from the portal and the computed CMOSPMIN, CMOSPMAX, and CMOSPAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

The computed CMOSNMIN, CMOSNMAX models results are further away from the average results. This can be attributed to the computed parameters where the minimum shows lowest end of results while the maximum results shows the highest end of simulation results. From these results it can be concluded that if the average model card for simulations it would provide a good feedback on circuit functionality.

4.2. Single Device Characterization - PMOS

A PMOS device of (0.5um/0.13um) is used to run simulations using model cards for CMOSN1, CMOSN2, CMOSN3 from the portal and the computed CMOSNMIN, CMOSNMAX, and CMOSNAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

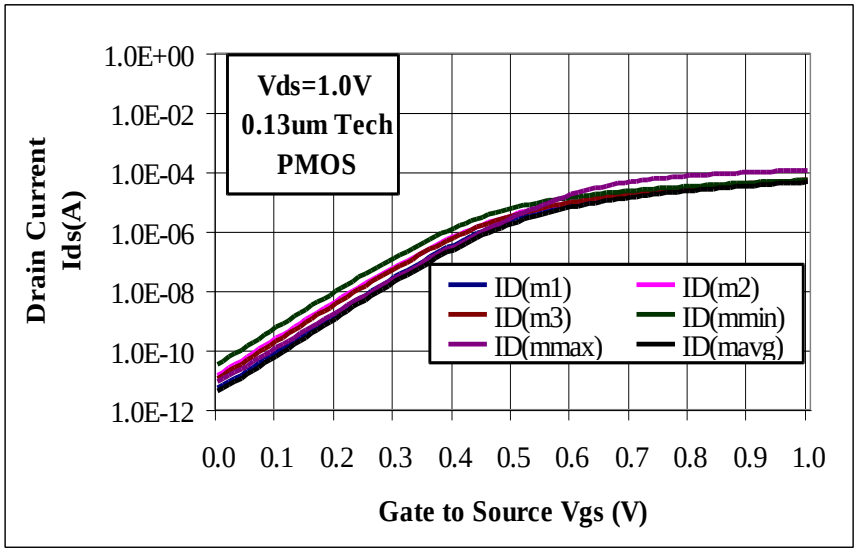


Figure 13: Linear region of PMOS device (0.5u/0.13u) at high Vds=1.0Vand using model cards for CMOSP1, CMOSP2, CMOSP3 from the portal and the computed CMOSPMIN, CMOSPMAX, and CMOSPAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

The plots shown in Fig. 12 – Fig.16 provide behaviour of PMOS device as predicted by the provided and computed model cards.

The PMOS device characteristics exhibits a similar behaviour observed for the NMOS device. Again, the CMOSPAVG model card tracks results from CMOSP1, CMOSP2, CMOSP3 results. The computed CMOSPMIN, CMOSPMAX models results are tracking low and high end of the model card spectrum and while the average model simulations are showing good representation of the sample model results.

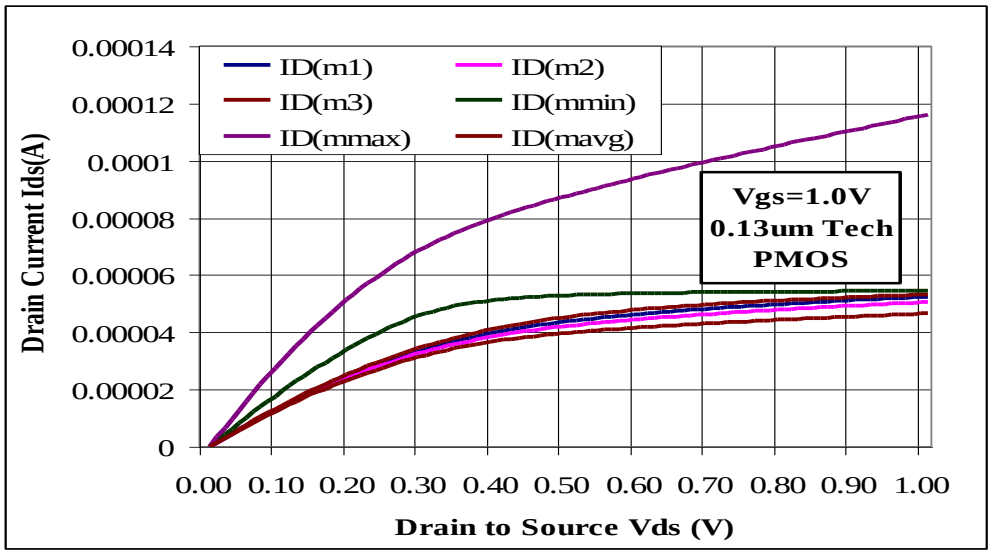
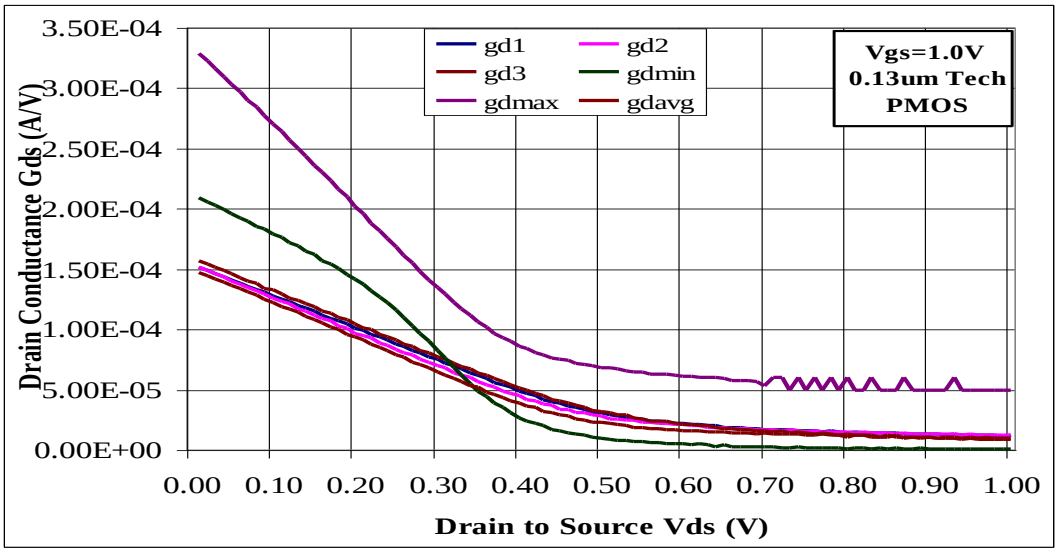


Figure 14: IV characteristics of PMOS device (0.5u/0.13u) at Vgs=1.0V and using model cards for CMOSP1, CMOSP2, CMOSP3 from the portal and the computed CMOSPMIN, CMOSPMAX, and CMOSPAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

Figure 15: Drain conductance of PMOS device (0.5u/0.13u) at Vgs=1.0V and using model cards for CMOSP1, CMOSP2, CMOSP3 from the portal and the computed CMOSPMIN, CMOSPMAX, and CMOSPAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.



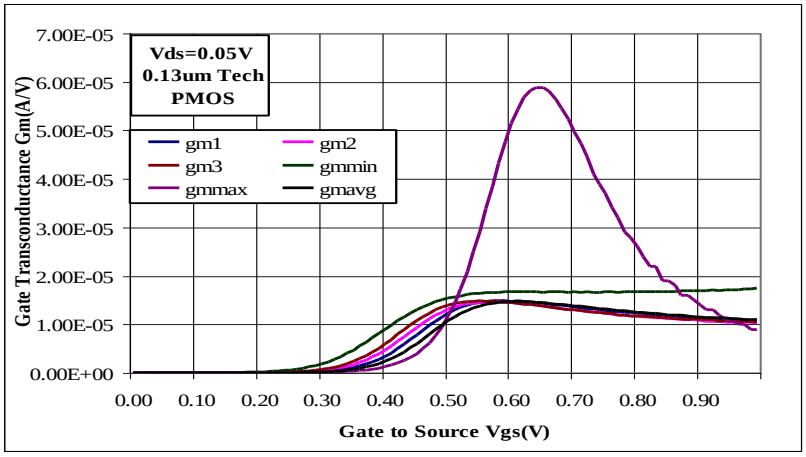


Figure 16: Gate transconductance of PMOS device (0.5u/0.13u) at Vds=0.05V and using model cards for CMOSP1, CMOSP2, CMOSP3 from the portal and the computed CMOSPMIN, CMOSPMAX, and CMOSPAVG model cards using the 140 model cards downloaded from MOSIS portal for NMOS and PMOS 0.13um Technology.

4.3. Simple Inverter Simulations

A simple inverter is constructed using a PMOS device with (1u/0.13u) and NMOS device with (0.5u/0.13u) sizes. The netlist of such inverter is shown in Fig. 11. The figure shows the case when the average model name is used for the PMOS and NMOS devices. The netlist is edited for the cases of all of the model names of N1(P1), N2(P2), N3(P3), NMIN(PMIN), NMAX(PMAX) model names. The DC transfer function of the inverter is then plotted while input voltage is swept across rail span from 0 to 2.5V.

The DC characteristics and the transient response of the inverter are simulated for the models of NMOS and PMOS devices as represented by the netlist file shown in Fig. 17 for PSPICE circuit simulator. The inverter characteristics are plotted as shown in Fig. 18, and Fig. 19 for DC transfer function and transient time characteristics respectively. The average model results are tracking results of models from 0.13um Technology.

V. CONCLUSIONS

Circuit simulations of single devices and simple circuits are performed using spice models downloaded from MOSIS fabrication services portal site. Several technology models were experimented with. To reduce the number of simulations required, it is found that user can produce an average model card by averaging the model parameters of all device model avaliable. Similarly, minmum and maximum model cards can e produced using the MIN and MAX functions of tabular data. In this work, a total of 140 models for NMOS and PMOS devices from 0.13um Technology were available for simulations. The model cards were used to simulate NMOS and PMOS device characteristics in the linear region, and saturation regions. Additionally, the single device gate transconductance, and drain conductance are also tested. It was found that the average model card produces results that closely represent sample model cards. To further test validity of using average model, an inverter circuit is simulated for DC

```
* My pspice cir

*mp1 d g sp sp  CMOSP1 w= 1e-6 l=0.13e-6
*mn1 d g sn sn  CMOSN1 w= 0.5e-6 l=0.13e-6

*mp2 d g sp sp  CMOSP2 w= 0.5e-6 l=0.13e-6
*mn2 d g sn sn  CMOSN2 w= 0.5e-6 l=0.13e-6

*mp3 d g sp sp  CMOSP3 w= 0.5e-6 l=0.13e-6
*mn3 d g sn sn  CMOSN3 w= 0.5e-6 l=0.13e-6

mpavg d g sp sp  CMOSPAVG w= 0.5e-6 l=0.13e-6
mnavg d g sn sn  CMOSNAVG w= 0.5e-6 l=0.13e-6

.inc mos_models.cir

Vdd sp 0 2.5
Vss sn 0 0

Vin g 0 2.5

c1 d 0 1p

.probe

.dc Vin 0 2.5 0.01
.print dc VD(mpavg)

.end
```

Figure 17: PSPICE net list file of a simple inverter using NMOS and PMOS devices from 0.13um Technology to evaluate provided and computed model cards behaviour.

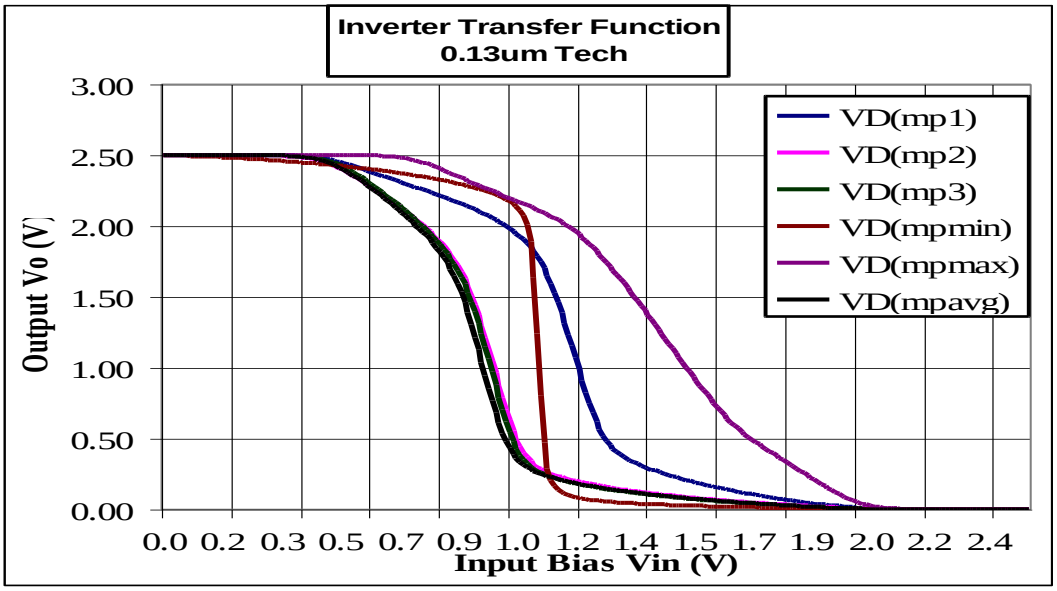


Figure 18: Inverter DC transfer characteristics simulated using the provided and computed models. transfer function and transient response. The average model response exhibit close fit to behaviour from sample model cards.

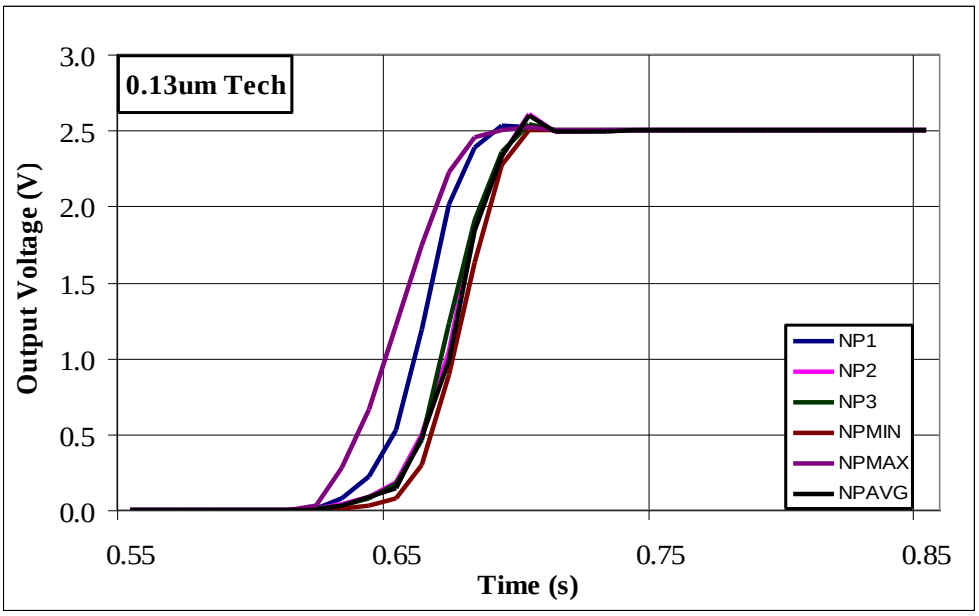


Figure 19: Inverter transient characteristics simulated using the provided and computed models.

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[1]. MOSIS Integration Circuit Fabrication Service, "https://www.mosis.com".

[2]. Ashraf Osman, Amin B. Abdel Nabi, Ismail El-Azhary, "The Potential of Establishing Computer_Aided_Design (CAD) Industry in Africa-Sudan As a Case-Study", IEEE, 2013 International Conference on Computing, Electrical and Electronics Engineering (ICCEEE), 26-28 Aug. 2013 , pp 87-91.