

Common Mode Voltage Control in Three Level Diode Clamped Inverter

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ABSTRACT

This paper presents simple sinusoidal PWM technique to reduced common mode voltage (CMV) at output terminal of the inverter. Multilevel inverter (MLI) is more suitable in high & medium power application, CMV is produced at the time of operation in output terminal of inverter. In this paper, an approach to reduced CMV at output terminal of MLI by using SPWM technique in three level diode clamped inverter (DCMLI) is proposed. A good transaction between the quality of the output voltage & the magnitude of CMV is achieved in this paper. The paper presents phase opposition & phase opposition disposition SPWM technique to reduced CMV in DCMLI. Simulation & experimental result presented to confirm the effectiveness of the proposed technique to control CMV.

Keywords: Diode clamped MLI, Common mode voltage, Sinusoidal PWM technique, PO & POD technique.

I. INTRODUCTION

Multilevel inverter (MLI) come to attention of researchers as soon as it was proposed by Nabae A in 1981. In the area of high power application multilevel inverter is a first choice where the demand is increasing & produced energy does not cope with the increasing demand. To obtain quality output voltage & current waveform with minimum ripple content, two level inverter require high switching frequency along with various PWM strategies. Two level inverter may not suit for high voltage application because of poor quality output. MLI have draw tremendous interest in the power industry application. Output of two level inverter is modified by increasing number of voltage level in the inverter without requiring higher rating an individual device can increase the power rating. Multilevel inverter consist of number of thyristor switches depends upon levels used in the

inverter. Now a day's thyristor switches replace by SCR's, BJT's, MOSFET's & IGBT's depending upon respective advantages. By switching action of the inverter switches staircase output is generated which is also called as multilevel output. As the number of voltage level increases the harmonic content of output waveform decreases significantly. Output generation by switching action results in common mode voltage (CMV) which are essentially zero sequence voltages superimposed with switching noise which will appear at rectifier, inverter & motor terminals. If not minimized then they appear on the stator winding with respect to ground results in motor life expectancy is shortened. As the number of voltage level increases the synthesized output waveform has more steps which produce a staircase wave that approaches a desire waveform & harmonic distortion of the output waveform decreases approaching zero as no of level increases.

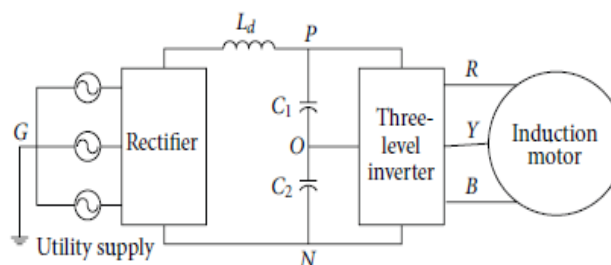


Fig 1: General block diagram of AC-DC-AC VSI or CSI fed ASD.

The diode clamped multilevel structure is more suitable for high & medium voltage drives which are directly connected to utility power system. Diode clamped inverter is also known as NPC. Diode clamped inverter deals with one major

problem that is generation of common mode voltage (CMV) and it is appear at the output terminal of the inverter. Generation of common mode voltage results in large bearing current due to heavy shaft voltage. This leads to failure of motor bearing.

Therefore best solution for this problem is only to eliminate CMV permanently. Variable frequency, variable voltage require in industrial application, medium and high voltage level supply given to three phase induction motors. multilevel inverter have been establish better counterpart to conventional two level

inverters. Recently number of techniques are used to eliminate common mode voltage, but in all the techniques SPWM techniques is more suitable. In this paper common mode voltage reduction techniques for three level diode clamped inverter is represented by using SPWM technique.

II. BACKGROUND

2.1. Three Level Diode Clamped Inverter:

In high voltage & high power application diode clamped multi level inverter (DCMLI) become a research hotspot. Multi level inverter is preferred

in between three to nine level inverter. As the number of voltage level increases total harmonic distortion is reduced. Three level inverter is shown in diagram below.

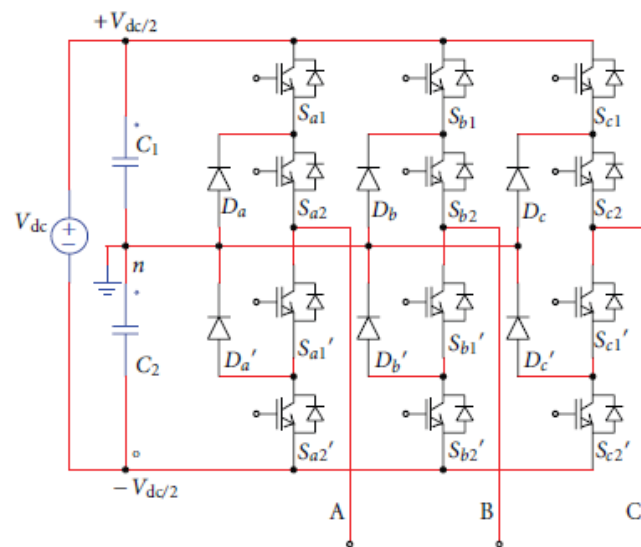


Fig 2: Schematic diagram of three phase, three level diode-clamped inverter.

Three phase diode clamped MLI have three legs with common DC bus, this DC voltage is subdivided into switching capacitors. Each diode has to block the voltage equal to number of switching above it times the supplied DC voltage. Basically one leg of DCMLI consist of 'M-1' capacitors & 'M-2' clamping diodes where 'M' is the total voltage levels & total number of switches are 2(M-1), in the

three level inverter number of switches used are 12, for the operation in numbering order of Sa1, Sa2, Sb1, Sb2, Sc1, Sc2, Sa1', Sa2', Sb1', Sb2', Sc1' & Sc2'. Dc bus consist of two capacitors C1 & C2, six diodes are used two for each leg. In DCMLI diode is used as clamping device to clamp the dc bus voltage so as to achieve staircase output voltage as shown in the diagram.

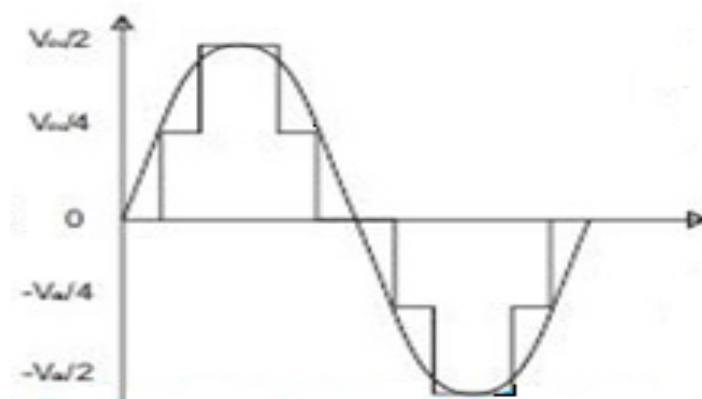


Fig 3: Staircase output of the Three level inverter.

2.2.Common Mode Voltage:

Common mode voltage is defined as the voltage between neutral point of the load & system ground. It may also defined as the voltage between neutral point of the load & dc midpoint given diagram shows generalized drive system , where V_{ag} , V_{bg} & V_{cg} are the voltages between ground to phase & V_{ng} is the voltage between neutral point of the motor and system ground. i. e. CMV & it is given as:

$$CMV = V_{ng} = \frac{V_{ag}+V_{bg}+V_{cg}}{3} \text{ (Two level inverter)}$$

$$CMV = V_{ng} = \frac{V_{ag}+V_{bg}+V_{cg}}{3} * \frac{V_{dc}}{2} \text{ (Three level inverter)}$$

$$CMV = V_{ng} = \frac{V_{ag}+V_{bg}+V_{cg}}{3} * \frac{V_{dc}}{4} \text{ (Five level inverter)}$$

Output of the inverter is not purely sinusoidal but square wave (discrete) , hence sum of the instantaneous value is not zero & develops common mode voltage. Meanwhile in purely sinusoidal three phase system sum of the instantaneous voltage is zero hence CMV is zero. Neutral point voltage variation results in generation of common mode voltage three times the fundamental frequency. If common mode voltages are not reduces they results in bearing failure of the motor connected as load in output terminal.

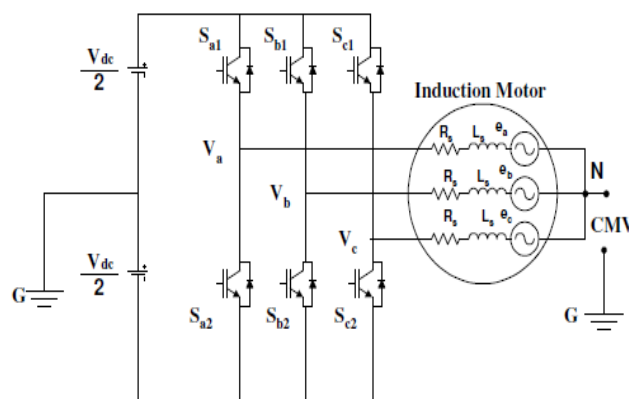


Fig 4: Three phase VSI inverter with Induction motor connected as a load.

III. CMV CONTROL STRATEGIES

Control strategies for common mode voltage can be classified as given below:

1. Using some extra hardware circuitry such as isolation transformer, active passive filter, common mode choke & dual bridge inverter etc.

2. Using modification in control strategy such as space vector PWM technique (SVPWM) & sinusoidal PWM technique (SPWM).

In the first method common mode voltage is minimized by selecting proper rating of the chock, but the main issue is that the total harmonic distortion (THD) increases with controlling CMV.

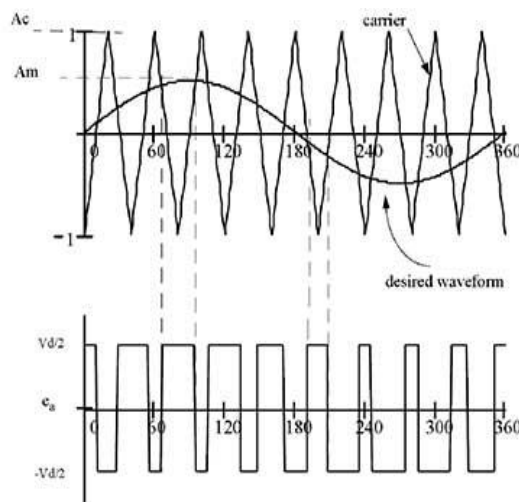


Fig 5: Sinusoidal pulse width modulation technique

High frequency triangular carrier signals superimposed with three sinusoidal reference signal known as the modulating signals to generates the gating signal for the inverter switches this process known as sinusoidal PWM technique. SPWM technique provides effective switching frequency of load voltage is 3 times the switching frequency of each cell as determine by its carrier signal & require less complex algorithm with ease to implement. Instead of maintaining width of all pulses same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of sine wave evaluate at the center at the same pulse. The distortion & lower order harmonics are reduced significantly. The gating signal generated by comparing sinusoidal reference signal with triangular carrier wave. When instantaneous value of

the sine reference is greater than the triangular carrier wave then the output is at +Vdc & when the reference signal is less than the carrier signal then the output is at -Vdc.

Different SPWM technique can be classified as:

- Phase disposition method
- Phase shifted method
- Phase opposition disposition method.

3.1 Phase disposition method:

Phase disposition method based on the comparison of sinusoidal reference waveform with triangular carrier waveform, all the carrier waveform have same frequency and amplitude & all the carrier waves are in phase with each other. If 'M' is the number of voltage level in inverter then 'M-1' carrier signals are used to generate voltage levels.

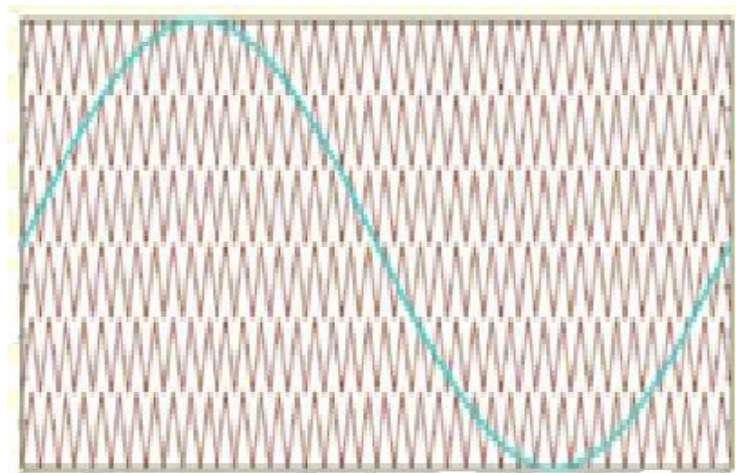


Fig 6: Phase disposition PWM technique.

3.2 Phase opposition disposition:

In this method sinusoidal reference wave superimposed on the carrier triangular wave (which are phase above & below the zero reference) like in phase opposition method but difference is that, triangular wave above & below the reference zero

axis have equal frequency and amplitude but they are phase shifted by 180 degree with each other. The reference signal is compared with all carrier waves thus gate pulses are generated & are related into each switching device.

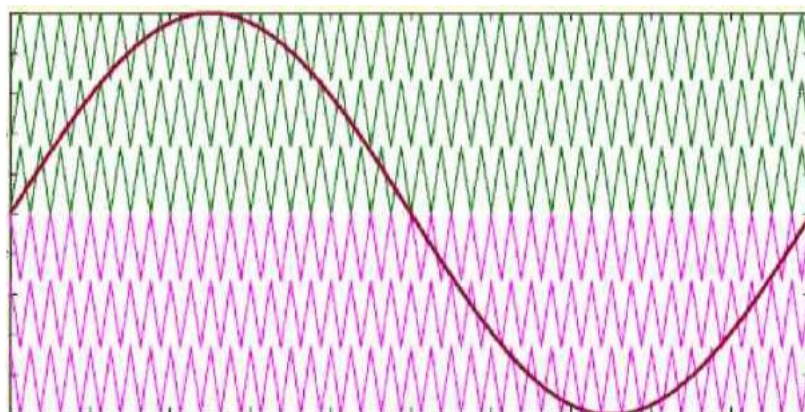


Fig 7: Phase opposition disposition SPWM technique

IV. EXPERIMENTAL RESULTS

Figure shows the simulation diagram of the proposed inverter. The circuit is designed in Matlab/simulink and the generation of pulses has

been made by comparing every carrier wave with the sine wave and the resultant pulses has been given to the appropriate switches to produce the three level staircase waveform

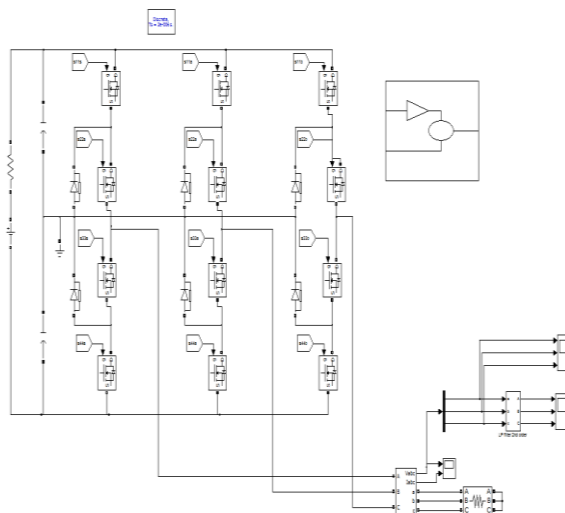


Fig 8: Simulation diagram for proposed 3 level MLI

Diagram below shows experimental results of three level diode clamped inverter common mode voltage reduction by PD-SPWM technique with &

without filter. Fig 9 shows output of inverter which is staircase wave. Sinusoidal waveform obtain after filtering inverter output.

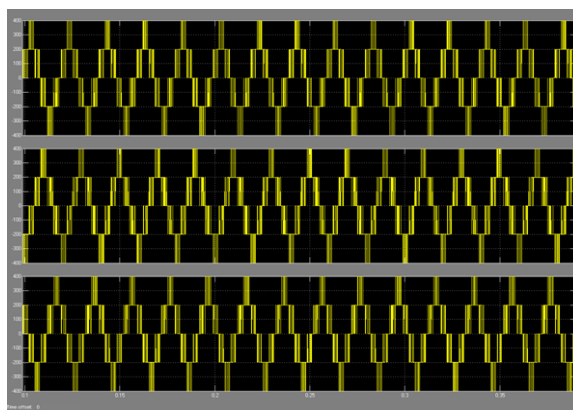


Fig 9: Output waveform of proposed MLI using PD technique.

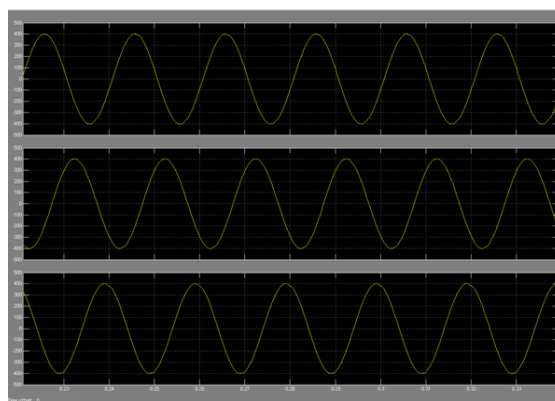


Fig 10: Filtered output waveform of proposed MLI

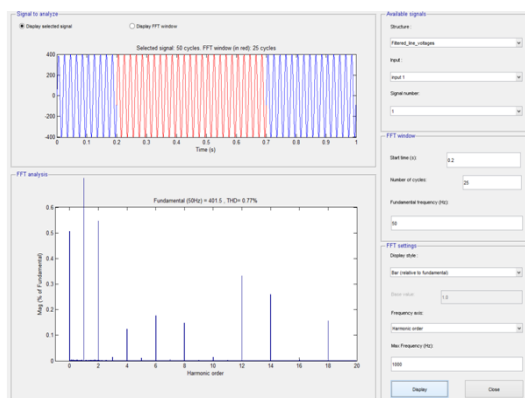


Fig11: FFT analysis of proposed technology using PD technique.

The total harmonic distortion (THD) of any fundamental wave shape. FFT analysis is done to determine the THD of the output waveform.

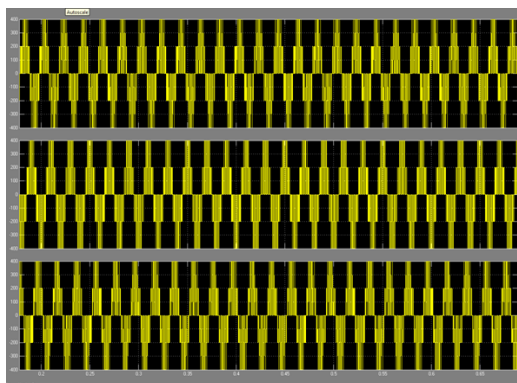


Fig 12: Output waveform of proposed MLI using POD technique.

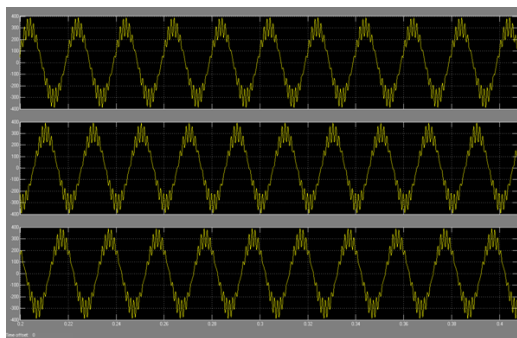


Fig 13: Filtered output waveform of MLI.

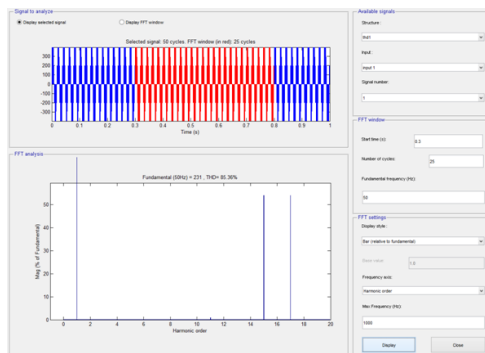


Fig 14: FFT analysis of proposed technology using POD technique.

Phase opposition disposition method uses reference wave & carrier wave, carrier waves are 180 degree phase opposite to each other. Comparing

reference signal with carrier wave results in gating pulses shown in diagram. Fig. 13 shows filtered output of the MLI.

Table 1: Comparison between PD & POD technique.

SPWM Technique	THD		CMV
	Without Filter	With Filter	
PD	45.13	0.77	Vdc/2
POD	85.36	18.58	Vdc/2

V. CONCLUSION

The proposed technique reduces CMV at the output terminal of the DCMLI. Experimental results & simulation shows the effectiveness of the proposed techniques giving reduction in magnitude of common mode voltage. Results prove that PO-SPWM technique is superior to reduced Total harmonic distortion & CMV.

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