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Harmonics Reduction of Multilevel Inverter Drive Using Sine Carrier Pulse Width Modulation Techniques

S. Ebanezar Pravin, S. P. Umayal

ABSTRACT
The main objective of this paper is to control the speed of an induction motor by using seven level diode clamped multilevel inverter and improve the high quality sinusoidal output voltage with reduced harmonics. The presented scheme for diode clamped multilevel inverter is sine carrier Pulse Width Modulation control. An open loop speed control can be achieved by using V/*f* method. This method can be implemented by changing the supply voltage and frequency applied to the three phase induction motor at constant ratio. The presented system is an effective replacement for the conventional method which has high switching losses, its result ends in a poor drive performance. The simulation result portrays the effective control in the motor speed and an enhanced drive performance through reduction in total harmonic distortion (THD). The effectiveness of the system is verified through simulation using PSIM6.1 Simulink package.
Keywords: Diode clamped multilevel inverter; Induction motor; Sine carrier PWM technique; THD; V/*f* method.

I. INTRODUCTION

AN induction motor being rugged, reliable, and relatively inexpensive makes it more preferable in most of the industrial drives. They are mainly used for constant speed applications due to unavailability of the variable-frequency supply voltage [1]. But, many applications are in need of variable speed operations. In early times, mechanical gear systems were used to obtain variable speed. Recently, power electronics and control systems have matured to allow these components to be used for motor control in place of mechanical gears. These electronics not only control the motor's speed, but can improve the motor's dynamic and steady state characteristics. Adjustable speed ac machine is equipped with an adjustable frequency drive.

It is a Multi level inverter drive for speed control of an induction motor. It controls the speed of the electric machine by converting the fixed voltage and frequency to adjustable values on the machine side. High power induction motor drives using classical three-phase converters have the disadvantages of poor voltage and current qualities. To improve these values, the switching frequency has to be raised which causes additional switching losses. Another possibility is to put a motor input filter between the converter and motor, which causes additional weight. The diode clamp method can be applied to higher level converters. As the number of level increases, the synthesized output waveform adds more steps, producing a staircase waveform. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels.

In this paper, a three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a five level unidirectional voltage balancing method of diode clamped inverter [2]. The voltage across the switches has only half of dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device [3]. The presented inverter can reduce the harmonic contents by using multicarrier SPWM technique. It generates motor currents of high quality. V/*f* is an efficient method for speed control in open loop. In this scheme, the speed of induction machine is controlled by the adjustable magnitude of stator voltages and its frequency in such a way that the air gap flux is always maintained at the desired value at the steady-state. Here, the speed of an induction motor is precisely controlled by using seven level diode clamped multilevel inverter.

II. CONVENTIONAL METHOD

The voltage source inverter produces an output voltage or a current with levels either zero or ±Vdc. They are known as two level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse-width modulation strategies. In high power and high-voltage applications, these five-level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. The dc link voltage of a Five-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered; hence the harmonic reduction becomes more difficult [4]. In addition, the five level inverters

generate high frequency common-mode voltage within the motor windings which may result in motor and drive application problems [5]. From the aspect of harmonic reduction and high dc-link voltage level, Five-level approachseems to be the most promising alternative. The harmonic contents of a seven-level inverter are less than that of a five-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage [6]. A seven level inverter will not generate common-mode voltages if the inverter output voltages are limited within certain available switching states. So, the seven-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems [7].

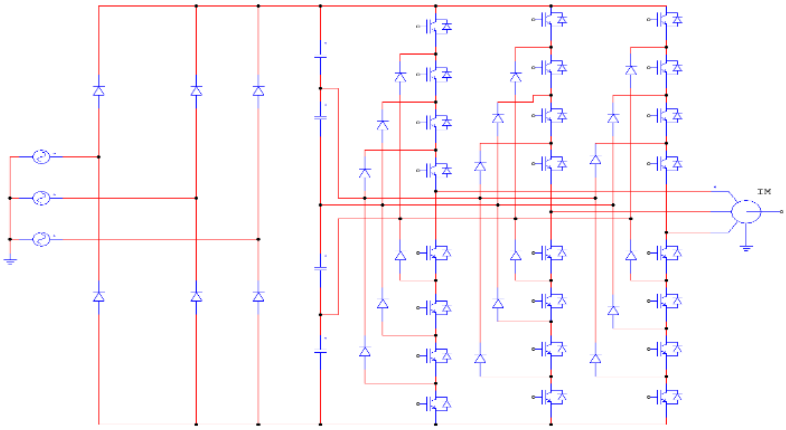

Fig 1. Five level inverter based drive circuit.

III. DRIVE SYSYEM DISCRIPTION

In the conventional technique normal PWM method is used. So that the voltage and current is of poor qualities and the switching frequency causes more amount of switching losses. Those drawbacks are rectified using three phase diode clamped multilevel inverter. The voltage and current quality are better and the switching losses are reduced when compared to the conventional technique. Also the THD is found to be better.

A. Structure of Seven Level Diode ClampedMultilevel Inverter

The seven-level neutral point-clamped voltage source inverter is shown in Fig.2. It contains 36 unidirectional active switches and 30 neutral point clamping diodes. The middle point of the 6 capacitors "*n"* can be defined as the neutral point [9]. The major benefit of this configuration is each switch must block only one-half of the dc link voltage (Vdc/6). In order to produce seven levels, only two of the twelve switches in each phase leg should be turned on at any time. The dc-bus voltage is split into three levels by two series-connected bulk capacitors, Ca and Cb, via. They are same in rating. The diodes are all same type to provide equal voltage sharing and to clamp the same voltage level across the switch, when the switch is in off condition. Hence this structure provides less voltage stress across the switch.

B. Principle of Operation

Table.1. shows the voltage levels and their corresponding switch states. State condition 1 means the switch is on, 0means the switch is off. There are two complementary switch pairs in each phase. These pairs for one leg of the inverter are (A1,A1'),(A2,A2'),(A3,A3'),(A4,A4'),(A5,A5'),(A6, A6'). If one of the complementary switch pairs is turned on, the other of the same pair must be off [10]-[14].

To produce a staircase-output voltage, consider one leg of the three-level inverter, as shown in Fig.3. The steps to synthesize the seven-level voltages are as follows.

1) For an output voltage level Vao=Vdc, turn on all upper-half switches A_1,A_2.A_3,A_4,A_5 and A_6
2) For an output voltage level Vao=5Vdc/6, turn on upper switch A_2.A_3,A_4,A_5,A_6 and one lower switch A_1'.
3) For an output voltage level Vao=4Vdc/6, turn on all lower half switches A_3, A4, A_5, A_6 and $A_{1'}$, A2'.
4) For an output voltage level Vao=Vdc/3, turn on all lower half switches, A_5, A_6, and $A_{1'}$, A2'.A3', A4'.
5) For an output voltage level Vao=Vdc/6, turn on all lower half switches, A_6 and $A_{1'}$, A2'.A3', A4', A5'.
6) For an output voltage level Vao=0, turn on all lower half switches , $A_{1'}$,$A_{2'}$.$A_{3'}$,$A_{4'}$,$A_{5'}$ and $A_{6'}$
7) For an output voltage level Vao=Vdc/2, turn on all lower half switches, A_4, A5, A_6, and $A_{1'}$, A2'.A3'.

Table I Output Voltage Levels And Their Switching States

Voltage V_{a0}	**Switch State**											
	A1	A2	A3	A4	A5	A6	A1’	A2’	A3’	A4’	A5’	A6’
V7	1	1	1	1	1	1	0	0	0	0	0	0
V6	0	1	1	1	1	1	1	0	0	0	0	0
V5	0	0	1	1	1	1	1	1	0	0	0	0
V4	0	0	0	1	1	1	1	1	1	0	0	0
V3	0	0	0	0	1	1	1	1	1	1	0	0
V2	0	0	0	0	0	1	1	1	1	1	1	0
V1	0	0	0	0	0	0	1	1	1	1	1	1

The most attractive features of multilevel inverters are as follows:

1) They can generate output voltage switch extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion [15].
3) They generate smaller common mode (CM) voltage, thus reducing the stress in the motor bearings [16].
4) They can operate with a lower switching frequency [17].
5)

IV. PROPOSED SCHEME

The block schematic of multilevel inverter fed three phase induction motor is show in figure.15. The complete system will consist of two sections; a power circuit and a control circuit. The power section consists of a power rectifier, filter capacitor, and three phase diode clamped multilevel inverter. The motor is connected to the multilevel inverter. An ac input voltage is fed to a three phase diode bridge rectifier, in order to produce dc output voltage across a capacitor filter. A capacitor filter, removes the ripple contents present in the dc output voltage [18]-[19].

The pure dc voltage is applied to the three phase multilevel inverter through capacitor filter. The multilevel inverter has 36 MOSFET switches that are controlled in order to generate an ac output voltage from the dc input voltage The control circuit of the proposed system consists of three blocks namely microcontroller, opto-coupler and gate driver circuit. The microcontroller is used for generating gating signals required to drive the power MOSFET switches present in the multilevel inverter. The voltage magnitude of the gate pulses generated by the microcontroller is normally 5V. To drive the power switches satisfactorily the opto-coupler and driver circuit are necessary in between the controller and multilevel inverter. The output ac voltage is obtained fromthe multilevel inverter can be controlled in both magnitude and frequency (V/f open loop control).

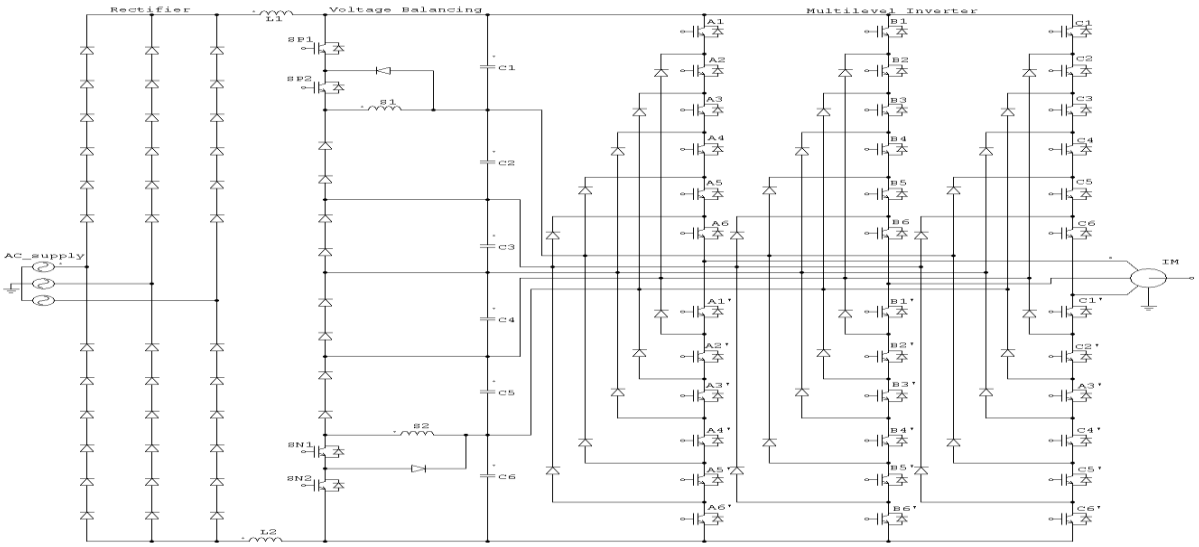

Fig 2. Seven level inverter based drive circuit

The controlled ac output voltage is fed to the induction motor drive. When the power switches are on, current flows from the dc bus to the motor winding. The motor windings are highly inductive in nature; they hold electric energy in the form of current. This current needs to be dissipated while switches are off. Diodes are connected across the switches give a path for the current to dissipate when the switches are off. These diodes are also called freewheeling diodes. The V/f control method permits the user to control the speed of an induction motor at different rates. For continuously variable speed operation, the output frequency ofmultilevel inverter must be varied. The applied voltage to the motor must also be varied in linear proportion to the supply frequency to maintain constant motor flux.

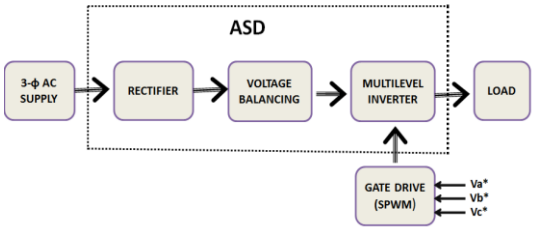

Fig 3. Basic block diagram.

V. MODULATION STRATEGY

This Paper mainly focuses on multicarrier SPWM method. This method is simple and more flexible than SVM methods. The multicarrier SPWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an n-level inverter is employed, n-1 carriers will be needed. The carriers have the same frequency WC and the same peak to peak amplitude Ac and are disposed so that the bands they occupy arecontiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency W_m and amplitude A_m. At every instant each carrier is compared with the modulating signal. Each comparison gives 1(-1) if the modulating signal is greater than (lower than) the triangular carrier in the first (second) half of the fundamental period, 0 otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Multicarrier PWM method can be categorized into two groups: 1) Carrier Disposition (CD) method 2) Phase shifted PWM method.

1) Advantages of multicarrier PWM techniques
2) Easily extensible to high number of levels.
3) Easy to implement.
4) To distribute the switching signals correctly in order to minimize the switching losses.
5) To compensate unbalanced dc sources.
6) Alternative Phase Opposition Disposition (APOD), where each carrier band is shifted by 180° from the adjacent bands
7) Phase Opposition Disposition (POD), where the carriers above the zero reference are in phase, but shifted by 180° from those carriers below the zero reference.
8) In-Phase Disposition (PD), where all the carriers are in phase [8].

In this paper the gating pulses for IGBT switches are generated by using In-phase disposition technique

Modulation Index;

(1)

N=number of Levels, A*m*=Modulation signal Amplitude, A*c*=Carrier Signal Amplitude

a. V/F Control Theory

Figure.7. shows the relation between the (voltage and torque) versus frequency. The voltage and frequency being increased up to the base speed. At base speed, the voltage and frequency reach the rated values. We can drive the motor beyond base speed by increasing the frequency further. But the voltage applied cannot be increased beyond the rated voltage. Therefore, only the frequency can be increased, which results in the field weakening and the torque available being reduced. Above base speed, the factors governing torque become complex, since friction and windage losses increase significantly at higher speeds. Hence, the torque curve becomes nonlinear with respect to speed or frequency

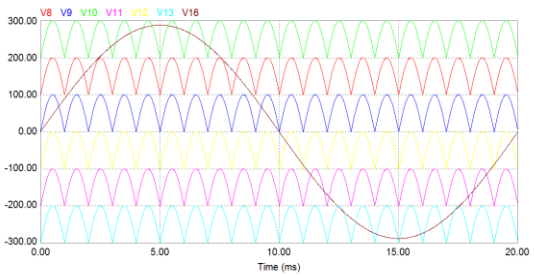

Fig 4. Sine Carrier PW Technique

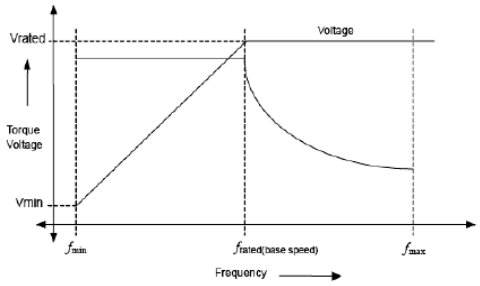

Fig 5. Speed-Torque characteristics with V/f control

b. Energy Saving In Variable Torque Load Application

Many systems are used constant speed motors and control process flow rates or pressures by mechanically regulation using throttling valves, dampers, fluid couplings or variable inlet vanes etc. These devices generally do not control flow or pressure efficiently because energy is dissipated across the throttling device. Running a motor at full speed while throttling the input or output is like driving a car with one foot on the accelerator and the other on the brake; a part of the produced output immediately goes to waste. A variable speed drive can save over 60% of the energy.Variable speed drives and the loads they are applied to can generally be divided into 3 groups

1) Constant power
2) Constant torque
3) Variable torque

In variable torque load applications, both torque and power change with speed. Torque varies with speed squared, and power varies with speed cubed. This means that at half speed, the power required is approximately one eighth of rated maximum. Common examples of variable torque loads are centrifugal fans, blowers and variable discharge pressure pumps. The use of a variable speed drive with a variable torque load often returns significant energy savings. In these applications the drive can be used to maintain various process flows or pressures while minimizing power consumption. In addition, a drive also offers the benefits of increased process control, which often improves product quality and reduces scrap. Effective speed ranges are from 50% to 100% of maximum speed and can result in substantial energy savings.

(2)

(3)

(4)

P = Power in Watts; T = Torque in N-m; N = Motor rotation speed in rpm;

A variable speed drive can also make it possible to stop a motor completely when it is not required as re-starting with a variable speed drive causes far less stress than starting direct on line - soft start is an inherent feature of the drive.

Regulating the motor speed has the added benefit of easily accommodating capacity rises without extra investment, as speed increases of 5-20% is no problem with an AC variable speed drive as long as there is enough spare capacity in the system. Reduced maintenance compared to DC systems (brushes and commutators) reduced motor/application noise levels.

VI. SIMULATED CIRCUITS AND WAVEFORMS

Figure 7. Shows the PWM circuit to generate the gating signals for the multilevel inverter switches. To control a three phase multilevel inverter with an output voltage of seven levels; sixcarriers are generated and compared at eachtimetoa set of three sinusoidal reference waveforms. One carrier wave above the zero reference and one carrier wave below the reference. These carriers are same in frequency, amplitude and phases; but they are just different in dc offset to occupy contiguous bands. Phase disposition technique has less harmonic distortion on line voltages.Simulated model for entire circuit is shown in Figure8.Induction Motor Drive using Seven Level Inverter Simulation DiagramOutput voltage for 50 Hz and 45Hz frequency are shown in be figure 8 and 11

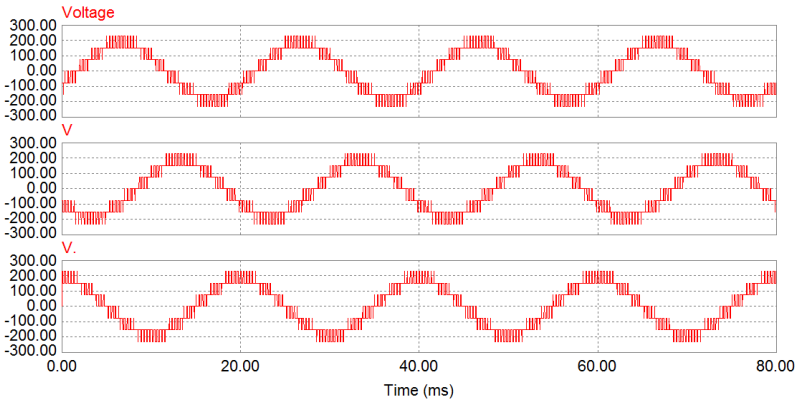

Fig 6. Output Phase Voltage for 50Hz Frequency.

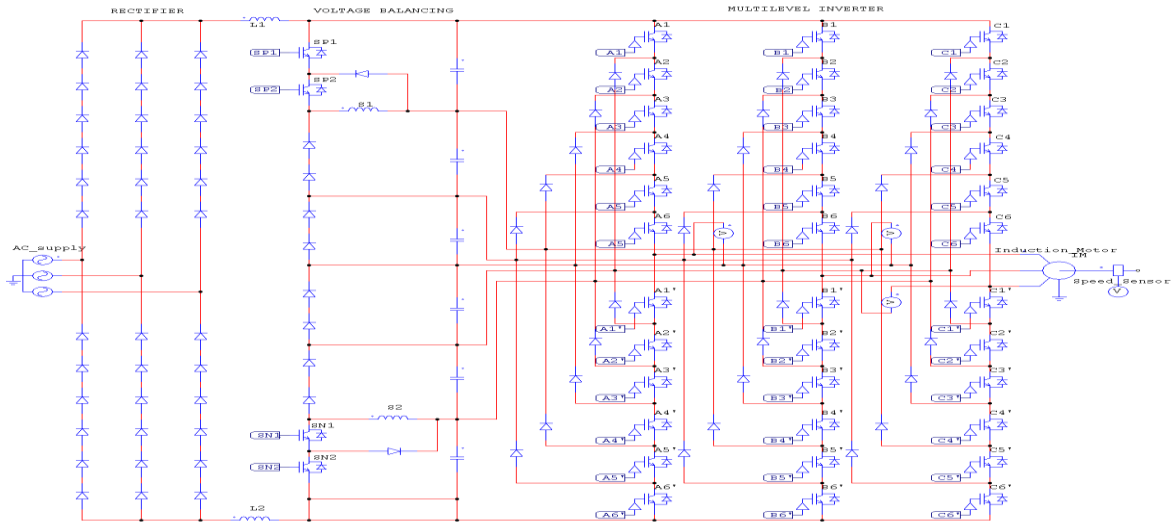

Fig 7. Simulation Circuit

Speed-Torque curves for 50 Hz and 45 Hz frequencies are shown in figure 9 and 12.

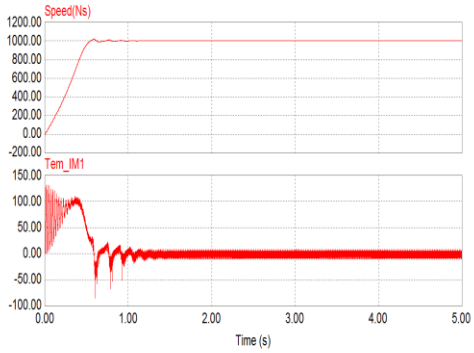

Fig 8. N-T Curves for 50Hz Frequency

The FFT plot of the output voltage is shown in Figure10. The plot shows that the harmonic content present in the output voltage is very Low.

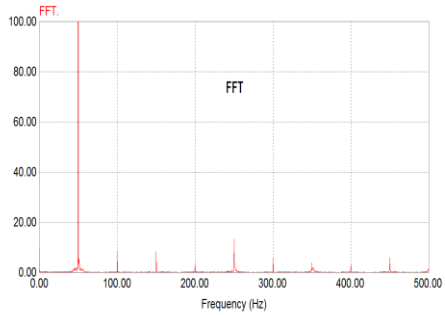

Fig 9. FFT for Output Voltage 50HZ. THD=0.4%

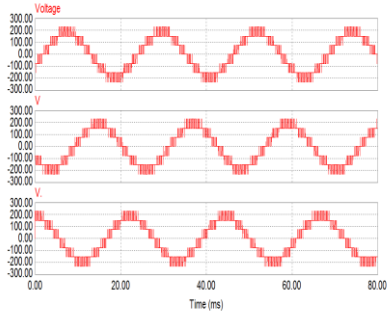

Fig10. Output phase-phase voltage for 45Hz frequency

The frequency of reference signal determines the inverter output frequency; and its peak amplitude controls the modulation index. The variation in modulation index changes the rms output voltage of the multilevel inverter. By varying the reference signal frequency as well as modulation index, the speed of an induction motor gets controlled.

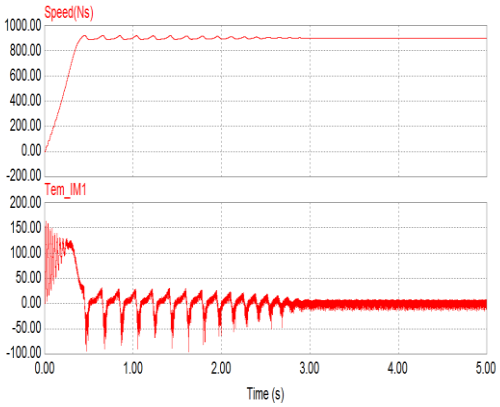

Fig 11. N-T curves for 45Hz frequency

The speed-torque curves conclude that the voltage and frequency applied to the motor gets decreased; then the speed of an induction motor also decreases simultaneously.

VII. CONCLUSION

In this paper a diode clamped multilevel inverter has been presented for drive applications. The sine multicarrier SPWM technique can be implemented for producing low harmonic contents in the output; hence the high quality output voltage was obtained. This high quality output voltage is better then the SPWM. The open loop speed control was achieved by maintaining V/*f* ratio at constant value. The simulation results show that the proposed system effectively controls the motor speed and enhances the drive performance through reduction in THD. This drive system can be used energy saving in variable torque load applications like boiler feed pumps conveyors, rolling mills, printing machines etc.

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S.Ebanezar Pravinreceived his Bachelor of Engineering degree in Electrical and Electronics Engineering from Anna University, Chennai at 2009

and his Master of Technologydegree in Power Electronics and Drives from Karunya University, Coimbatore at 2011. He is currently working towards his Ph.D in the Department of Electrical Engineering, Anna University, Chennai. He is also working as an Assistant Professor with the Department of Electricaland Electronic Engineering, at SCAD college of Engineering and Technology, Cheranmahadevi. His research interests are in the area of power converterand drives.

SP. Umayal is a Professor and also the Dean of Electrical and Electronics Engineering at Muthayammal Engineering College, Rasipuram. Shecompleted her Bachelor of Engineeringin Electrical and Electronics Engineeringat Thiyagarajar college of Engineeringat 1990 and also her Master of Engineering in Power Systemat the year 1999. She received her Ph.Dat 2008 inthe field of Power System Optimization. Her areas ofresearch include Power system optimization, FACTS andpower quality. She has 35 publications in her research area. Currently she is guiding 5 Ph.D. researchscholars. She is also a life member of IE (I) and ISTE.