

Modified Headfirst Sliding Routing: A Time-Based Routing Scheme for Bus-Nochybrid 3-D Architecture

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ABSTRACT

Several interesting topologies emerge by incorporating the third dimension in networks-on-chip (NoC). The Network-on-Chip (NoC) is Network-version of System on-Chip (SoC) means that on-chip communication is done through packet based networks. In NOC topology, routing algorithm and switching are main terminology. The routing algorithm is one of the key factor in NOC architecture. The routing algorithm, which defines as the path taken by a packet between the source and the destination. A good routing algorithm is necessary to improve the network performance. Here we are proposing a new architecture to improve the throughput and latency of the network. In the proposed approach we are using a fixed path for the packet to transmit from source to destination.

Index terms: NoC, Router

I. INTRODUCTION

Interconnect related problems, emerging from technology scaling and the integration limitations of systems-on-chip (SoC), originate from the functional diversity demanded by the electronics market. These issues have triggered a quest for nonconventional IC design paradigms, such as 3-D integration. For example, vertically stacked dies with through-silicon vias, together with networks-on-chip (NoC) have been proposed as potent solutions to address these interconnect problems and the design complexity of SoC. Each of these design paradigms offers unique opportunities. The major advantage of 3-D ICs is the considerable reduction in the length and number of global interconnects, resulting in an increase in the performance and decrease in the power consumption and area of wire limited circuits. Another important advantage of 3-D ICs is that this paradigm enables the integration of CMOS circuits with disparate technologies which can be non-silicon or even electro-mechanical.

Despite the significant advantages of three-dimensional integration, important challenges remain such as crosstalk noise analysis and reduction, thermal mitigation, and interconnect modeling. The wireless contact-less approach that connects chips in vertical dimension has a great potential to customize components in 3-D chip-multiprocessors (CMPs), assuming card style components inserted to a single cartridge communicate each other wirelessly using inductive-coupling technology. Although power supplies are provided by bonding wires at this moment, wireless power transmission techniques using inductive-coupling have been improved

recently. The inductive-coupling power transmission can be used for these card-style components inserted to a cartridge. In this case, adding, removing, and swapping chips in a package after the chips have been inserted to a cartridge are possible, which will bring us a great flexibility of "field stackable systems" using the card-style components in the future. Toward this purpose, the vertical communication interfaces should be simplified, while arbitrary or customized topologies should be used for intra-chip networks; thus, we focus on static Time Division Multiple Access (TDMA) buses for the inter-chip communication. The static TDMA-based vertical buses grants a communication time-slot for different chips at the same time periodically, which means they are working with different periodic scheduling. For example, at a certain Moment, vertical bus 0 gives a time-slot for chip 1, vertical bus 1 allows chip 2, and vertical bus 2 allows chip 0. At the next phase, vertical bus 0 gives a time-slot for chip 2, vertical bus 1 allows chip 0, and vertical bus 2 allows chip 1. Each vertical bus behaves just like an elevator in an office building.

One of the main disadvantages of xy routing algorithm is that the packet does not have a fixed path, it will move randomly to reach the destination node. The random movement of packet will affect the latency and the total power consumption of the chip. In xy routing algorithm the packet may run in to deadlock, livelock and starvation situations. To overcome these situations here introduced a new fixed path algorithm.

In first section II we are discussing about NoC router and in section III we are discussing xy routing algorithm. In section IV discussing modified algorithm

and its working. Finally we are comparing the simulation result of xy routing algorithm and the modified algorithm

II. NOC ROUTER

The design and implementation of a router requires the definition of a set of policies to deal with packet collision, the routing itself, and so on. A NoC router is composed of a number of input ports (connected to shared NoC channels), a number of output ports (connected to possibly other shared channels). The switching defines how the data is transmitted from the source node to the target one. Circuit switching and packet based switching is commonly used in routers. The routing algorithm is the logic that selects one output port to forward a packet that arrives at the router input. This port is selected according to the routing information available in the packet header. NoC, xy routing algorithm is used.

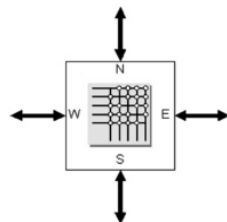


Fig 1 NoC router

III. XY ROUTING ALGORITHM

XY logic is the deterministic logic which analyses the header of data and send it to its destination port. The first four bits of the header are the coordinates of destination port. In XY logic a comparator is used which compares the header of the data to the locally stored X and Y coordinate and send the packet according to its destination address. Let the coordinates stored in header be H_x and H_y and locally stored coordinates be X and Y . So according to XY logic if $H_x > X$ then packet will move to east port otherwise move to west port. If $H_x = X$ then Y coordinate is compared, If $H_y > Y$ then packet will move to north port otherwise move to south port. Thus in this way XY logic will send the packet to the output channel of its destination port.

IV. PROPOSED SYSTEM

The router consists of east, west, north, south ports. Each port has its input channel and output channel. Data packet moves in to the input channel of oneport of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The buffering method used here is store and forward. The

movement of data from source to destination is called switching mechanism.

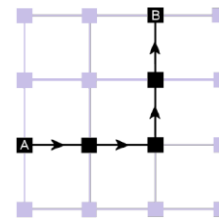


Fig 2 Concept of proposed routing

There are a couple of performance requirements that every Network on Chip implementation must satisfy, Small latency, Guaranteed throughput, Path diversity, Sufficient transfer capacity and Low power consumption. In the existing system the routing algorithm is xy routing algorithm. xy routing algorithm the packet will move randomly to reach the destination node and it does not have a fixed path. In order to avoid the randomness here introduced a new algorithm by introducing a busy signal.

In Fig 2 node 'A' is the source node and node 'B' is the destination node. So in here we are fixing a direct path from source node to destination node by using the new introduced busy signal. To transmit packet from source node 'A' to next node here we setting east busy signal in the east port of node 'A' empty. Each port of router consisting a request in, request out, acknowledgment and busy signals. During the packet transferring router requesting an idle link by making request in signal high and kept during the data transfer. The write operation takes place in the router by keeping the ack signal high. The busy signal at each port indicating that which output port is ready to accept the data packet, if the busy signal is high indicating that port is busy not ready to accept the packet, if it is low that output port is ready to accept the packet. When the packet is reached at the output port, request out signal goes high and the router is requesting idle link of another router. Likewise while setting the corresponding busy signal can fix a fixed path. Likewise while setting the corresponding busy signal can fix a fixed path.

V. PERFORMANCE ANALYSIS

In both existing and modified systems the source node and the destination nodes are same, while comparing the total time taken to reach destination node, in the existing system time taken by the packet to reach from source node to destination node is 315.522ns and in modified system the time taken by the packet to reach from source node to destination node is 231.170ns. From the comparison results it's clear that the modified system is reduced the total time taken to reach source to destination node and

improved the latency and throughput of the system.

Table 1

Source node	Destination node	Time taken to reach destination	
		Existing system	Modified system
Node-4	Node-15	315.522ms	231.170ms
Node-0	Node-3	392.00ms	153.00ms
Node-1	Node-7	311.959ms	156.00ms
Node-3	Node-7	314.00ms	72.00ms

Table 1 shows the analyzing result of xy algorithm and proposed algorithm.

VI. CONCLUSION

There are a couple of performance requirements that every Network on Chip implementation must satisfy Small latency, Guaranteed throughput, Path diversity, Sufficient transfer, capacity and Low power consumption while using the xy algorithm the packets will transmitted randomly and does not have a fixed path.in the existing system the total time taken by the packet to reach from source to destination is high and it will affect the latency and throughput of the system.in order to overcome this situation a new algorithm is introduced which defined a fixed path from source to destination. While comparing the existing and modified algorithm its shows that in modified system the time taken by the packet to reach destination is minimum compared to existing algorithm and thus its improve the latency and throughput of the system.

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