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Analysis and Comparison of CMOS Comparator At 90 NM Technology

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Abstract—
In this paper, A CMOS comparator with low power dissipation is presented. The preamplifier latch comparator is compared with conventional double tail comparator. The comparators designed and simulated in 90nm Cadence virtuoso environment technology. The particular preamplifier latch comparator will be mix of a good amplifier and a latch comparator can easily effect higher velocity and also low electric power dissipation. The proposed circuit topology improves kickback noise and reduces power dissipation compared with a conventional double tail comparator.Analysis are testified and compared with conventional comparator and enhancements are detected in this paper.
Index Terms-Pre amplifier latch comparator, Power dissipation, Kickback noise.

I. INTRODUCTION

Comparator can be widespread along the way connected with transforming analog impulses to be able to digital impulses. Inside A/D alteration process, it is necessary to be able to 1st small sample the actual insight. That tested indication can be than placed on combining comparators to determine the digital equivalent from the analog indication. [1].A comparator is a circuit that compares two signal, one input named as reference input with respect to the other input, and produce a digital output either (+) or (-) depending upon which input is greater[2]. Comparators have crucial influence on the overall performance of high-speed analog-to-digital converters [3]. Minimizing the power dissipation for the digital circuits requires optimization at all level of the design.

So, this optimization depends on circuit style, topologies and in fact includes the technology which is used to implement the digital circuits [4] .So a topology for the comparator is developed and compared with the existing model using the existing model Cadence Environment (Virtuoso) at GPDK 90 nm technology for analyzing. Block representation of the proposed design of the comparator is shown in Fig. 1. This designed comparator consists of three stages namely input stage, decision stage and output stage. The input stage (The actual insight point (the preamplifier stage) amplifies the particular insight indication to enhance the particular comparator sensitivity as well as segregate the particular insight in the comparator coming from moving over noises coming from optimistic responses point[5]. Choosing one signal may be the center from the comparator used to figure out which in turn from the input signs is larger. The last period may be the output buffer amplifies the details from latch as well as results an electronic signal. [6]

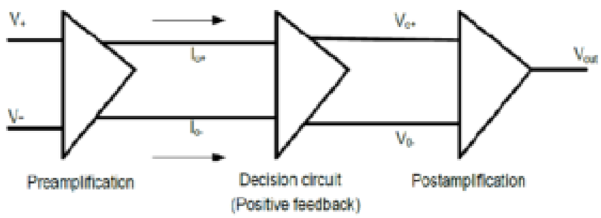

Figure1. Block diagram of preamplifier based Comparator [17]

The preamplifier latch comparator [7], is usually mix of the amplifier and also a latch comparator can purchase excessive rate and minimal electrical power dissipation.. Due to continue technology scaling, reduce intrinsic gain with reducing the drain to source resistance and increasing the static power dissipation [8]. The proposed circuit topology improves kickback noise and reduces power dissipation compared with a conventional comparator.

II. POWER AND DELAY ANALYSIS

A. Power Dissipation :

Dynamic comparator electric power dissipation is similar to of which connected with digital gates, which may have an electric dissipation offered somewhere around by means of.

$$p = f\, c\, (vdd)^2$$

Where
f = output frequency [1]
c = output capacitance
Vdd = supply voltage

B. Propagation delay :

Propagation delay can be defined as at how much speed the amplifier responds with applied input. Simply speaking propagation delay is the delay between output and input.

Propagation time delay = (Rising Propagation Delay time + Falling Propagation Delay Time) /2 [1]

III. CONVENTIONAL DOUBLE TAIL COMPARATOR

A rail-to-rail comparator design consists of a CMOS latch circuit and an S-R latch circuit. The latch has been designed by transistors T1-T10 and S-R latch by transistors T11-T18 The particular latch level can be used to ascertain which usually with the feedback indicators is bigger and amplifies the variation.[18] SR latch which acts as a memory to keep values for a clock period.

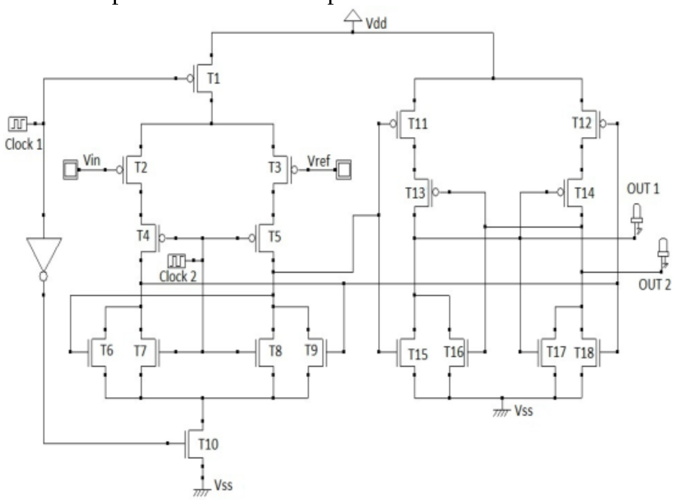

Figure 2: A high speed low power double tail latched comparator [9]

The conventional architecture of comparator shown in Fig. 3 subsists of an S-R latch circuit and a CMOS latch circuit .The CMOS latch circuit latch consists of transistors T1-T10 and S-R latch is made up of transistors T11-T18. Transistor T1 and T10 have been employed as enlarged end of the latch circuit. The latch stage plays the role of decide the larger input signals larger and intensely magnify their difference [11]. When the clock1 is small T1 and T10 gets ON and when it is huge (reset mode) transistors T1 and T10 gets OFF.

This method has least stacking help to perform at small supply power as comparison [11,12].In this DT comparator urn on and separate the inputs from remaining of the circuit [13]. PMOS differential pair (T1 and T3) creates current alteration for saturating T6 or T9 for a lesser alteration between V in and V ref .V ref effects the increment of voltage offset for the S-R latch for properly working of comparator. The transistors T6-T9 built the NMOS regeneration circuit in which T6 and T7 are the switching NMOS transistors touches the switching time [14,15]. Transistors T11-T18 built a SR latch play the part to performances as a memory for retaining values for a clock period.

IV. PROPOSED PREAMPLIFIER LATCH COMPARATOR:

proposed This proposed preamplifier latch comparator subsists involving about three stages: the actual suggestions preamplifier stage, some sort of latch stage, in addition to a good production load stage (it is usually inherently some sort of self-biased differential amplifier pursue by an inverter which gives the digital output).The preamplifier stage is a differential amplifier with active loads [16]. The preamp stage role is amplification of the input signal in order to get improvement in the particular comparator tenderness by means of improving the particular minimal input indication in which the particular comparator could make a decision and distinct the particular input from the comparator coming from transferring sound (also named kickback noise) from the constructive comments point. [16]. It also can reduce input referred latch offset.

The Ml as well as M2 sizes are usually fixed by subtracting straight into thinking about the diff-amp trans conductance along with the feedback capacitance. Your trans conductance sets the actual gain from the stage as well as how big Ml as well as M2 ascertains the actual feedback capacitance from the comparator [16]. Right here gary the gadget guy m1 = gary the gadget guy m2. The optimistic responses latch stage is employed to discover greater feedback indicators and others as well as next to each other incredibly amplifies their variation. [9].

It takes positive feedback from the cross gate connection of M8 and M9. Consider i+ >> i- so that M7 and M9 are ON and M8 and M10 are OFF. Here also β 7 = β 10 =β a and β 8 = β 9 =β b for which vo- is ~ 0V and v0+ is

$$vo+=\sqrt{\frac{i+}{\beta_a}+V_{th}}$$

(i)

When drain to source voltage value of M9 is reach equal to the threshold voltage, if we increase i- is and decrease i+ is V th of M8, switching occurs and. At the point M8 takes current afar from M7 which in

turn cause decrement in drain to source voltage of M7 and M9 gets turns off in result.
If we suppose that maximum value of v+ or v- is equal to 2V th, then below these circumstances M8 and M9 will operate under cut-off under steady state conditions [16]. Then voltage over M9 becomes V th and M9 gets saturated and current of M9 is

$$i- = \frac{\beta_b}{\beta_a} i+$$

This is the point at which switching occurs; i.e. M9 gets shuts off and in opposite M8 gets turns on. If β a = β b,then switching occurs when the currents, i+ and i-, are equal. A identical study of increasing i+ and decreasing i- results in

$$i+ = \frac{\beta_b}{\beta_a} i-$$

The output buffer which is the final component of the preamplifier latch comparator play the role of changing this productivity of the latch stage in to a total degree digital stage productivity (logic 0 as well as reasoning 1).
This end result barrier must get a differential enter signal and never to create slew-rate limitation.
This routine in the end result barrier is usually inherently a new self-biased differential amplifier pursued by a great inverter. The inverter is joined as a isolate supplementary gain stage and remove any load capacitance from differential amplifier [7].To conclude, the actual preamplifier dependent comparator tries higher velocity in addition to much less counteract voltage although has enormous static electrical power usage.

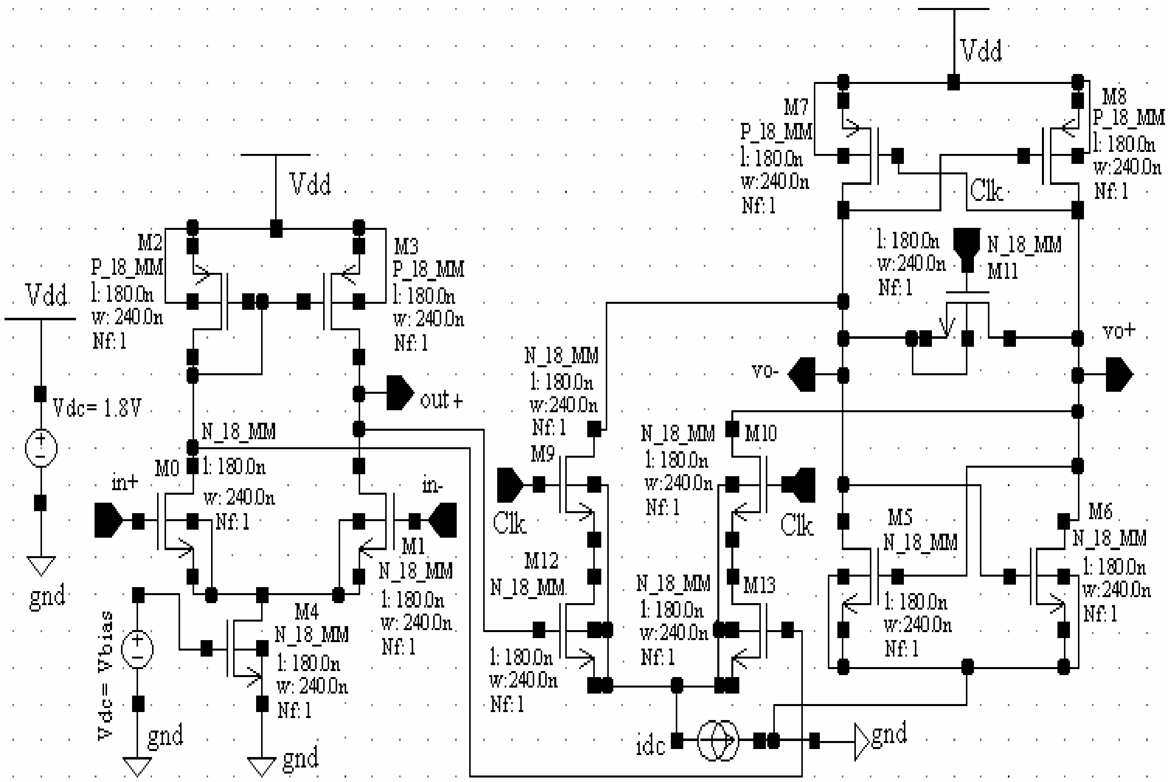

Fig.4.2 Schematic view of proposed comparator. [3]

The proposed preamplifier latch comparator subsists of transistors M1,M2,M3,M4. The differential part is made up of NMOS transistors M0 & M1, as well as the load transistor subsists of transistors PMOS M4 and M3.
Your gain on this preamplifier very easily achieve a suitable benefit using smaller the size of input differential pair can be retained this type of smaller benefit in order that the gain on this preamplifier very easily scopes an adequate benefit
.In this comparator design the part of Latch is the most susceptible. It this part subsists of two inverters which are joined returning to rear collectively compose a differential comparator and the two differential nodes of the latch are joined by an NMOS transistor .The latch part subsists of transistors from M5 to M13 in which two cross coupled inverter pair

M5-M6 & M7-M8 are used and as well as the charge asymmetry connections M9-M11 part also.

The most important regenerative loop is composing by rest Transistors M5-M8 for the latch. The width and lengths of regenerative loop transistors M5-M8 are put up minimum in order to obtain minimal capacitive possesions,and their W/L ratio is put up according to an ideal inverter. In addition measurements are fixed with regard to toning the metastable getaway stage of the inverter to help 1 / 2 of the voltage provide. Your switching transistor M11 will the a part of brief circuits the latch's differential nodes to a approved DC stage.

Their thickness is usually increased as a way to benefit to create available the DC stage shut nodes to each other.

Remainder Transistors M9-M10 are applied to help avert the timepiece nourish kickback outcomes from the latch on the feedback. M9-M10 transistors size furthermore selecting aspect on the efficiency in the latch like that in the event the size can be improved, this total on the similar capacitance around the nodes in the latch and raises the reply connected with timepiece nourish above the feedback; resulting in drop throughout reactivity in the latch. Within the reverse aspect in the event the size is decreased, subsequently essentially insight indicate should be greater otherwise latch charge asymmetry won't be properly generate.

The actual latch functions with a couple of stages; the first is recast as well as other will be regeneration. Inside Recast step, the particular impose asymmetry will be generated about the differential nodes with the latch proportional to the variances inside input signal..Where in regeneration mode, the voltage on nodes asymmetrates is strengthen to the rail-to-rail digital levels by regeneration loops of the NMOS and PMOS.When clk gets increase, the amplifier is handicapped and at this phase the latch has to amplify the difference achieved a input transistors M12-M13 to create logic levels at the output.

In the design transistors (two NMOS-PMOS pair) in the inverter combination is compose in order to obtain hence high comparison speed due to decrease in the parasitic capacitance. During the totally reset stage period, the particular changing transistor brief circuits the particular latch's components which can be somewhat corresponding to 1/2 voltage offer. A benefit due to this characteristic The idea offers furthermore benefit of which regenerative curl 2nd stage could move the particular result towards related binary degrees as resolute because of the asymmetry of demand. Within end result the particular velocity and also performance of the comparator obtains greater of the comparator gets increased.

V. RESULTS AND SIMULATION

Simulation of comparators is done using the 90nm CMOS technology. In this design, 1.8 V is used supply voltage1.8 V is used for procedure and clock period was 25ns. This design can be used where average power ,dynamic power and static power are the main parameters.

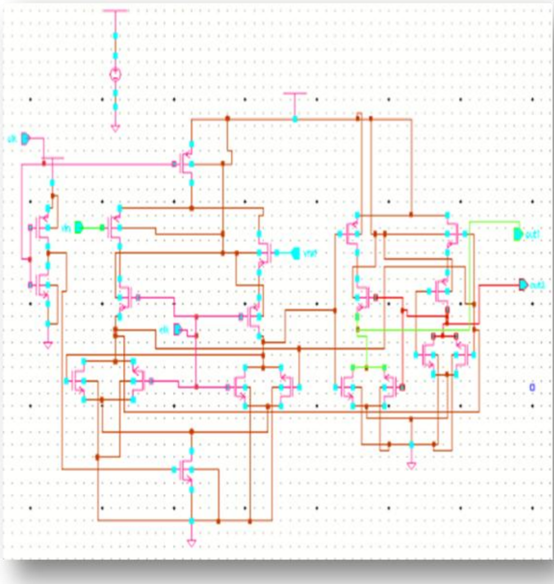

Fig. 2 Schematic of Conventional Comparator

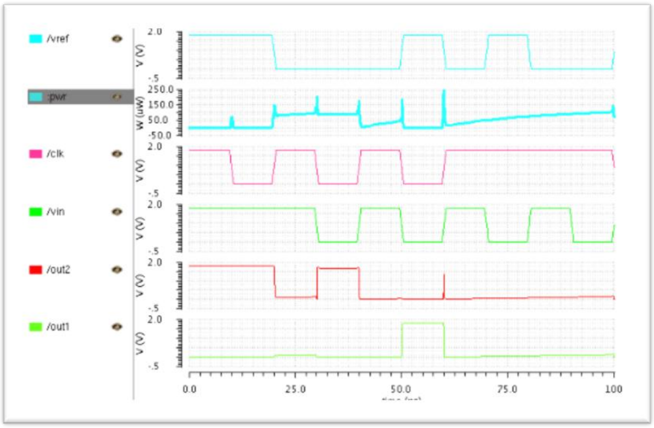

Fig. 3 Power Waveform of Conventional Comparator

Table 1. Power Calculation

PARAMETER	VALUES
Average Power	98.23E-6
Static Power	2.977E-6
Dynamic Power	96.253E-6

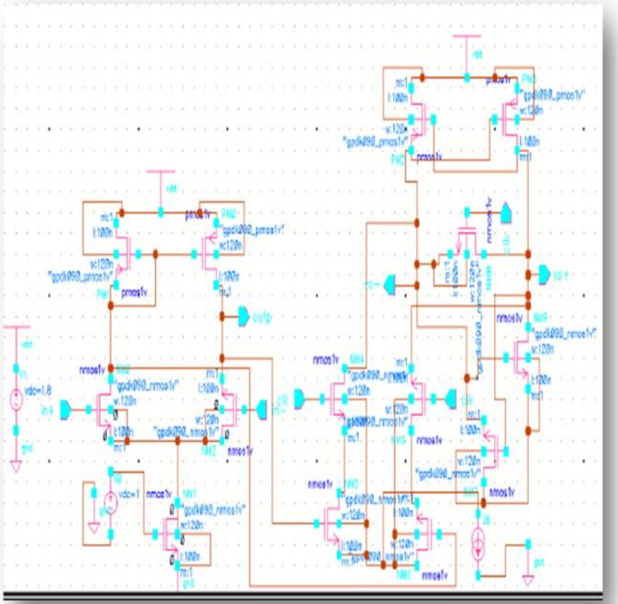

Fig 3 Schematic of proposed comparator

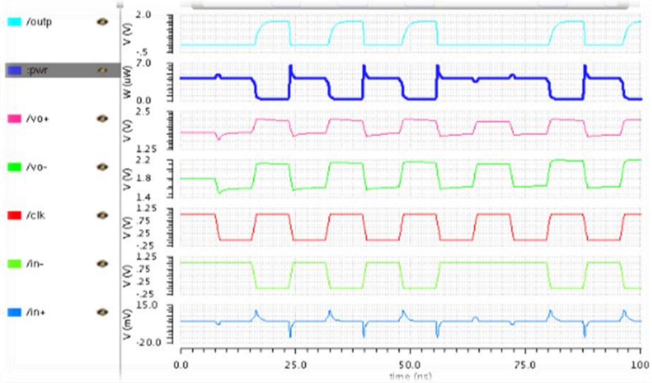

Fig 4 Power waveform

Table 2. Power waveform

PARAMETER	VALUES
Average Power	51.38E-6
Static Power	211.1E-6
Dynamic Power	-159.72E-6

Table 3. Comparison of Power Calculation

PARAMETERS	CONVENTIONAL COMPARATOR	PROPOSED COMPARATOR
AVERAGE POWER	98.23E-6	51.38E-6
STATIC POWER	2.977E-6	211.1E-6
DYNAMIC POWER	96.253E-6	-159.72E-6

VI. CONCLUSION

In this work Thesis subsists of a CMOS comparator analysis and comparison to find less power dissipation and. Propose analysis is centered on pre amplifier regeneration part and a latch part. This comparator is designed for analog to digital converters .Analysis achieved with 1.8 V input supply. Paper attained low average power consumption nearby 46.85E-6 compare to conventional comparator.

REFERENCES

[1] B.Razavi,"Design of Analog CMOS Integrated Circuits,"Tata McGraw-Hill, Delhi, 2002.

[2] Ramakant A. Gayakwad ―Op-Amps and Linear Integrated circuits fourth edition Pearson Education.

[3] Razavi and B. A. Wooley, "Design techniques for high-resolution comparators," IEEE J. Solid-State Circuits, vol. 27, no. 6, pp. 1916-1926, Dec. 1992.

[4] Geetanjali Sharma, Uma Nirmal, Yogesh Misra, " A low power8-bit magnitude comparator with small transistor count hybrid PTL/CMOS logic," International Journal of Computational Engineering & Management, Vol 12, April2011.

[5] R. Wang, K. Li, J. Zhang and B. Nie, "A High Speed High Resolution Latch Comparator For-Pipeline ADC," IEEE International Workshop on Anti-counterfeiting, Security, Identification, Xiamen, 16-18 April 2007, pp. 28-31.

[6] W. Rong, W. Xiaobo and Y. Xiaolang, "A Dynamic CMOS Comparator with High Precision and Resolution," IEEE Proceedings of 7th International Conference on Solid-State and Integrated Circuits Technology, 18-21 October 2004, pp. 1567-1570.

[7] J. M. Kim, "A 6-Bit 1.3 GSample/s A/D Converter in 0.35 µm CMOS," Doctor Thesis, University of Texas at Dallas, Dallas, 2005.

[8] B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006..

[9] Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 53, no. 12, pp. 1398-1402, Dec. 2006.

[10] Shubhara Yewale, Radheshyam Gamad" Design of Low Power and High Speed CMOS Comparator for A/D Converter Application"Scientific Reasarch, Wireless Engineering and Technology, 2012, 3, 90-95.

[11] Riyan Wang, Kaihang Li, Jianqin Zhang and Bin Nie, "A High-Speed High-Resolution Latch Comparator for Pipeline Analog-to-

Digital Converters", IEEE International workshop, April 2007, pp 28 – 31.

[12] J.-T. Wu and B. A. Wooley, "A 100-MHZ Pipelined CMOS Comparator", IEEE Journal Solid-State Circuits, Dec. 1988 Vol.23, No. 6, pp 1379 – 1386.

[13] P.M. Figueiredo and J.C Vital, "Low kickback noise techniques for CMOS latched comparators", International Symposium on Circuits and Systems, May 2004, Vol.1 pp 537 – 540.

[14] H. P. Le, A. Zayegh and J. Singh, " Performance Analysis of optimized CMOS Comparator", Electronics Letters, May 2003, Vol. 39 pp 833 – 835.

[15] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "Analysis and design of analog integrated circuits", John Wiley & Son Iuc, USA, 2009, 5th editon.

[16] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS- Circuit Design, Layout, and Simulation", IEEE Press Series on Microelectronic Systems, IEEE Press, Prentice Hall of India Private Limited, Eastern Economy Edition,2002.

[17] Rohit Mongre , R. C. Gurjar "Design of Low Power & High Speed Comparator with 0.18µm Technology for ADC Application" Rohit Mongre Int. Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 4, Issue 8(Version 1), August 2014, pp. 146-153.

[18] Riyan Wang, Kaihang Li, Jianqin Zhang and Bin Nie, "A High-Speed High-Resolution Latch Comparator for Pipeline Analog-to-Digital Converters", IEEE International workshop, April 2007, pp 28 – 31.