

A Low Phase Noise CMOS Quadrature Voltage Control Oscillator Using Clock Gated Technique

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ABSTRACT

This project presents the low phase noise cmos quadrature voltage control oscillator using clock gating technique. Here the colpitts vco is used to split the capacitance in the Qvco circuit producing quadrature output. The startup condition in the oscillator is improved by using G_m enhancement [12]. This QVCO performs the operation anti phase injection locking for device reuse [8]. The new clock gating technique is used to reduce the power with the power supply 1.5v. The QVCO uses a 0.5mA with phase error of 0.4° and exhibits a phase noise of -118dBc/Hz at 1MHz offset at the centre frequency of 500MHz.

Index terms: current switching, clock gating, phase noise, Qvco

I. Introduction

This paper presents the cmos quadrature voltage control oscillator with low power consumption in the clock gating technique. IC's of vco are the main building blocks of single chips in today's world. Noise is generated using the cross coupled vco which degrades the phase noise performances. Due to the several limitations occurring tradeoff between the quadrature phase accuracy, tuning range, phase noise and startup reliability in the conventional vco's. Injection locked LC QVCOS is based on the harmonics called first and super. Injection in RF circuits phase noise is favorable [1]-[3]. This work presents the low phase noise and low power clocked gated technique using g_m enhanced differential amplifier.

The main idea of clock gated technique is used to reduce power by including the small circuits. Here the gates of Mc1 and Mc2 in the inphase vco are connected to the outputs of Q-phase vco and the gates Mc3 and Mc4 are connected in the in-phase vco in an inverse manner [12]. By reducing the phase noise we are replacing the usual interconnected LC-VCOS. In the proposed clock gated techniques all the outputs are equal. In the arrangement of QVCO there is 180° phase shift between the potentials of I+ and I- and the nodes Q+ and Q-[11].

II. MOS VARACTORS

Mos varactors are variable; voltage control capacitors are based on mos structures. The main applications are LC- vco's. By the combination of inductor L the varactor C determines the vco frequency f_0 (without damping).

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The Mosfet is not a four terminal device as a transistor it is a three terminal device. The source and

drain regions are apply to the voltage tune that tunes the variable capacitor. The variable capacitor is presents between the gate node and all other node at the AC ground. Essentially it is the series connection of gate oxide capacitance and the depletion region capacitance.

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d}$$

III. INDUCTOR MODEL

Inductors are widely used in RF circuits as inductive load and matching elements are low noise amplifiers. This work focuses on integrated symmetrical inductors used for VCOs in standard digital CMOS technologies[4].

The performance of the inductor is limited by the losses through undesired currents in the substrate and in the series resistance of the inductor windings. Although there exist several definitions of quality factor they can be reduced to the common, when the quality factor increases when the losses decrease.

$$Q = \frac{(\text{inductively})\text{stored energy per cycle}}{(\text{resistively})\text{dissipated energy per cycle}}$$

IV. Band tuning capacitors and switches

In order to obtain a low VCO gain and still cover the full tuning range, digitally switched capacitors were implemented in the VCO tank. The sets of capacitors in the QVCO, approximately binary weighted were employed, resulting in 16-band tuning. Involving a higher number of bands provides better overlap between the bands; on the downside it adds some fixed capacitance from the pass transistor switches [7]. The capacitors used were of Metal insulator Metal (MIM) type. Initially, the capacitor values were selected based on binary weighted, but then adjusted for improved overlap.

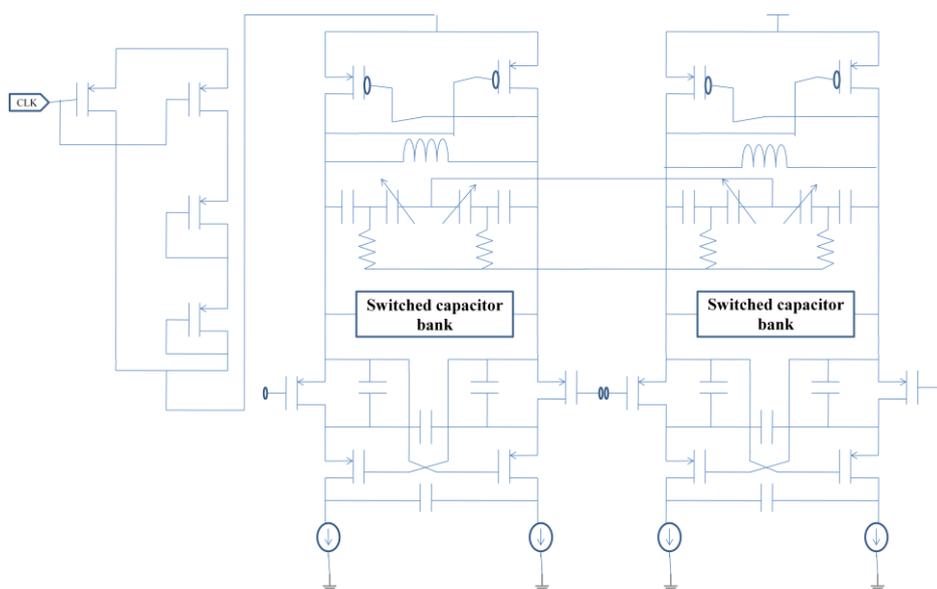
The band switches were designed using NMOS pass gate sizes were also binary weighted along with the capacitors. The source and drain of the pass gates were given as DC input, to keep them on when the output of the oscillator swings to extreme values and also to avoid high currents between source-bulk and drain-bulk junctions. The varactors of source and drain pins is connected to ground using two 3K-ohm resistors, which provide RF isolation.

V. ANALYSIS OF PROPOSED CIRCUIT

Either NMOS or PMOS or complementary solutions are capable of being used. In the CMOS

circuit power consumption is lower as current is reused. Exemplarily for the NMOS-only topology it has further been shown that phase noise at a given power consumption is inferior compared to the complementary case. The proposed coupling technique does not suffer from any of the disadvantage like phase noise, quadrature phase and figure of merit. In this circuits the oscillator are ac coupled to the varactors. The enhanced loop gain can be explained in the inversion factor of

$$\frac{1}{n} = \frac{(C_A + C_B)}{C_A}$$

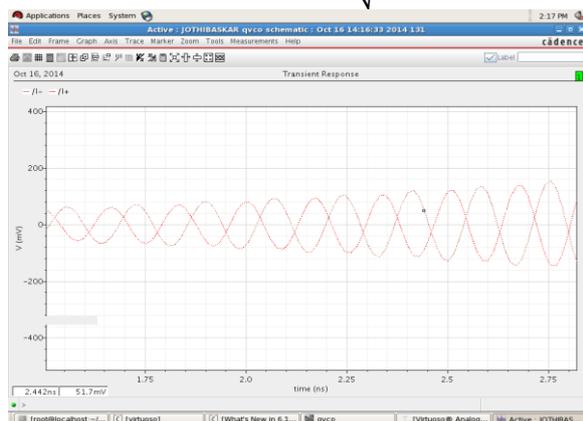


The current switching noise pair is added under colpitts oscillator noise shaping and g_m enhancement. Here we are deriving the oscillator start up frequency from the small signal model of the oscillator [12].

$$g_{mc} R_p \geq \frac{(C_A + C_B)^2 - g_{mn} R_p C_A (C_A + C_B)}{(C_A C_B)}$$

The minimum required values are derived as

$$(g_{mc} + g_{mn}) R_p \geq 2 + 2 \sqrt{1 - g_{mn} R_p}$$



VI. TABLE

	This work	10	11	12
CMOS PROCESS (μm)	0.18	0.5	0.18	0.13
F_{VCO} (MHZ)	500	433	403	403
PHASE NOISE@FREQ OFFSET	120@ 1M	100@ 600k	98@ 160k	127@ 1M
TUNING RANGE (%)	20	19	27.5	1.5
I/Q phase error	0.4^0	NA	NA	0.5^0
Supply voltage	1.5	3.3	1.5	1
Dc power	0.65	1.2	1.2	1
Fom	170	156	165	179

VII. Conclusion

In this project a new low phase noise low power quadrature voltage control oscillator is designed.

Here the startup condition is improved and also power consumption is reduced using the g_m enhancement. In this clock gated technique generates quadrature signal and tuning range is 20% at 500MHz outputs by coupling two differential colpitts vco with current switching via colpitts core without need of any coupling devices the phase noise is -120dbc/HZ@HZ at the operating frequency of 500MHz. the quadrature phase accuracy is 0.4° and tuning range is 20% while the power consumption is 0.65mw.

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