

## Energy efficient and high speed domino logic circuits

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### ABSTRACT

Domino CMOS circuit family finds a wide variety of application in microprocessors due to low device count and high speed. In this paper, various conventional and proposed designs for low leakage and high speed wide fan-in domino circuits are reviewed. The techniques used in the paper reduce the total power dissipation and delay by 25% and 58% respectively as compared to the conventional footed domino logic circuit. Simulations are performed on Tanner tool at 65nm technology for 16 input OR gate.

**Keywords** – contention, domino logic, leakage, power consumption, reliability.

### I. INTRODUCTION

Domino logic circuits are widely used in high speed and high performance microprocessor applications. A trade off occurs between noise immunity and performance. In order to increase reliability of a circuit, power supply has to be scaled but this leads to increased power consumption. So other techniques are to be employed to reduce power consumption and delay.

In a domino logic circuit a keeper transistor is used as leaving the dynamic node floating induces problems of leakage and charge sharing.

A conventional approach to increase reliability is sizing the keeper transistor. For keeper sizing [1], keeper ratio KPR is defined as

$$KPR = \frac{\text{Width of keeper}}{\text{Width of evaluation network}}$$

Upsizing the keeper transistor increases the noise margin but at the same time increases power consumption and vice-versa. Hence a trade-off occurs between reliability and performance. In order to address this issue several techniques are proposed in the paper. Various techniques including footless domino logic (FLDL), footed domino logic (FDL), conditional keeper domino logic (CKDL), high speed domino logic (HSDL) and conditional evaluation domino logic (CEDL) are reviewed and compared in order to compute power consumption, delay and power delay product.

### II. LITERATURE REVIEW

Conventional domino logic circuits such as footless and footed domino logic circuit are reviewed along with other proposed schemes. These circuits include the basic footless domino logic (FLDL), footed domino logic (FDL) [2], conditional keeper domino logic (CKDL), high speed domino logic (HSDL), conditional evaluation

domino logic (CEDL). Main aim of these circuits is to improve the circuit performance having wide fan-in [3].

Using a keeper transistor helps to address the problems of leakage and charge sharing but increases power dissipation. So sizing the keeper transistor helps to overcome the problem but then tradeoff occurs between reliability and performance.

#### A. Footless domino logic (FLDL):

Footless domino logic circuit is a standard domino logic circuit shown in fig.1. employing a PMOS keeper transistor to reduce charge sharing problem.

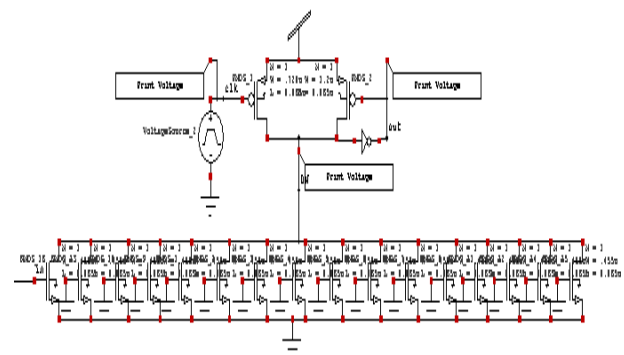


Fig.1. Footless Domino logic

#### B. Footed domino logic (FDL):

FDL is shown in fig.2. Here a footer NMOS transistor is employed to reduce the leakage current. During the precharge phase as clock is low, PMOS transistor PMOS\_1 turns ON and output node precharges to vdd. During the evaluation phase clock is high which turns off PMOS transistor and switches on the footer transistor N\_1. Now, depending upon

the evaluation network, output switches to low or high. This technique reduces power consumption but at the same time increases delay.

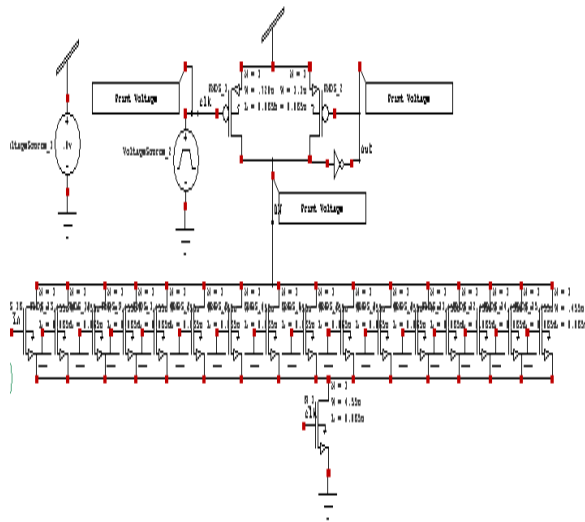


Fig.2. Footed Domino Logic

**C. Conditional keeper domino logic (CKDL):**

CKDL is shown in fig.3. In this technique two keepers are employed, small transistor (with small sizing) k1 and other large transistor (with large sizing) k2[4]. As the clock goes high k1 is ON, after delay of two inverters keeper k2 goes ON only if output of NAND gate goes LOW. NAND output is low only if both delayed inverters and dynamic node are HIGH. Here size of k2 is kept larger than k1 to improve noise margin of the circuit.

Main drawback of this circuit is delay increases due to two inverters and NAND gate[5].

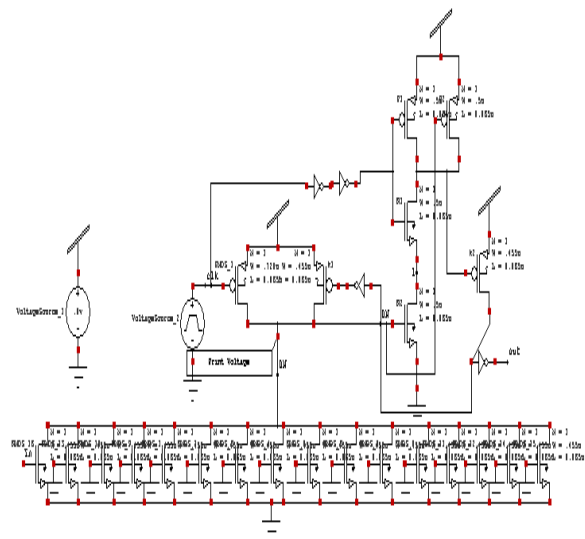


Fig.3. Conditional keeper Domino Logic

**D. High speed domino logic (HSDL)**

HSDL[4] is shown in fig.4.

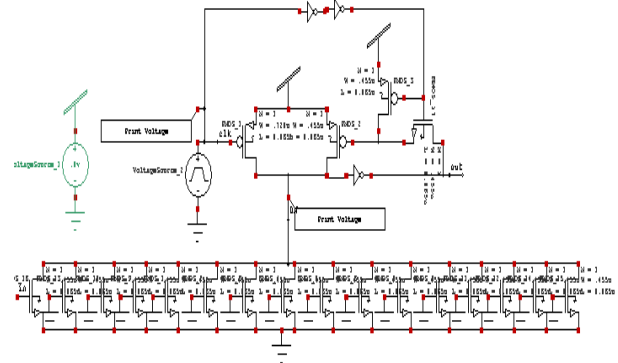


Fig.4. High Speed Domino Logic

As evaluation phase begins, clock goes HIGH, transistor P3 turns ON and the keeper transistor P2 turns OFF. Hence reducing the contention between the keeper and evaluation network. After the delay transistor P3 turns off. Depending upon the evaluation network transistor N1 may turn ON hence turning ON P2 i.e. if output of evaluation network goes high, it turns ON N1. This circuit has better speed.

Drawback of this circuit is if noise increases at input, dynamic node may get discharged giving false output.

**E. Conditional Evaluation Domino Logic (CEDL)**

Conditional Evaluation Domino Logic[6]. (CEDL) is another domino logic circuit shown in fig.5.

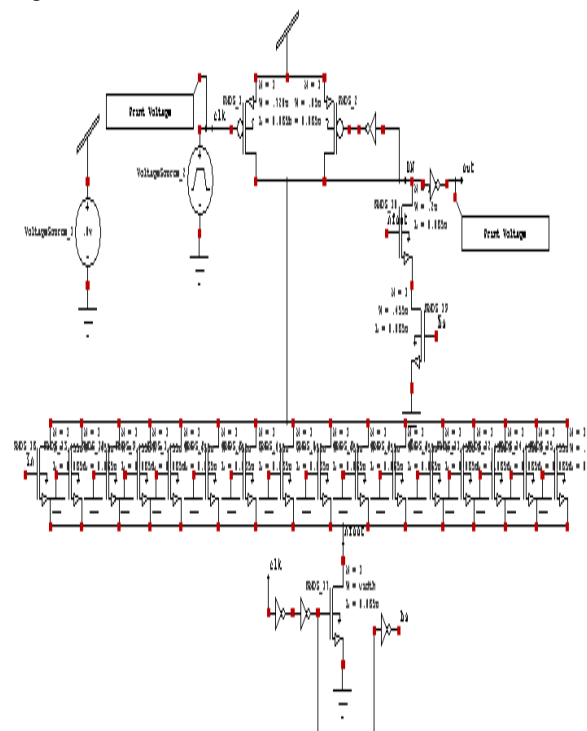


Fig.5. Conditional Evaluation Domino Logic

Here stacked NMOS transistors N2, N3 are used to evaluate the circuit which turns ON conditionally. As clock goes HIGH during evaluation phase for a delay of two inverters, transistor N1 remains OFF hence we get high voltage value at NFOOT node. Voltage at NFOOT node could be increased or decreased by sizing footer transistor N1 and evaluation network. If N1 is upsized voltage at NFOOT node decreases and upsizing evaluation network increases voltage at NFOOT node. This effect is shown in fig.6.,transistors in evaluation network are swept from 1um to 4um with constant footer width. As sizing increases NFOOT increases.

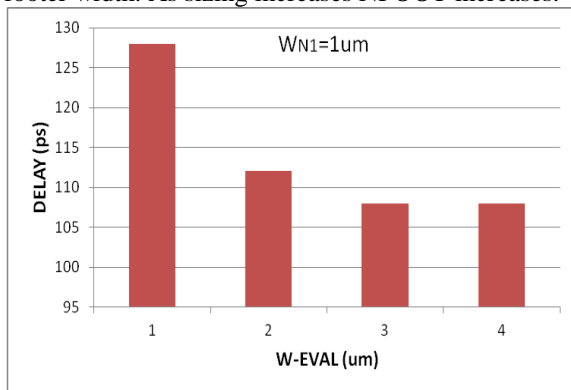


Fig.6. Delay versus evaluation network sizing

### III. SIMULATION AND PERFORMANCE COMPARISON

All the above topologies are simulated on tanner tool (TCAD) at 65nm technology model. Supply voltage used is 0.8V, temperature is 27 degree Celsius. Wide fan-in 16 input OR gate is used as benchmark circuit at 1 GHZ frequency.

Power, delay and power delay product are computed through simulations.

Power consumption is measured when one input is HIGH and discharges the precharge node.

Delay from input (IN1) to output (VOUT) is measured where all other inputs remain at zero. Fig.7 shows the waveform of input, clock, output and dynamic node voltage for 16 input OR gate of HSDL logic style.

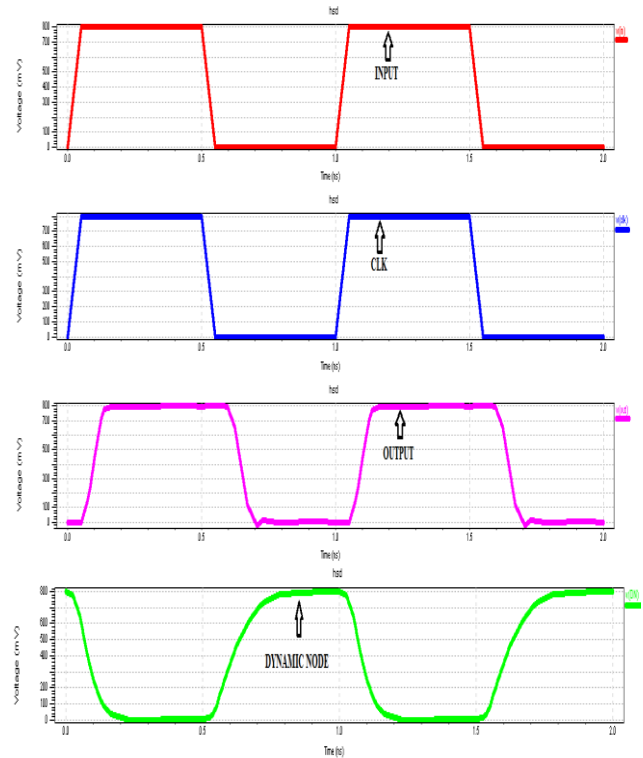


Fig. 7 HSDL waveform for 16 input OR gate

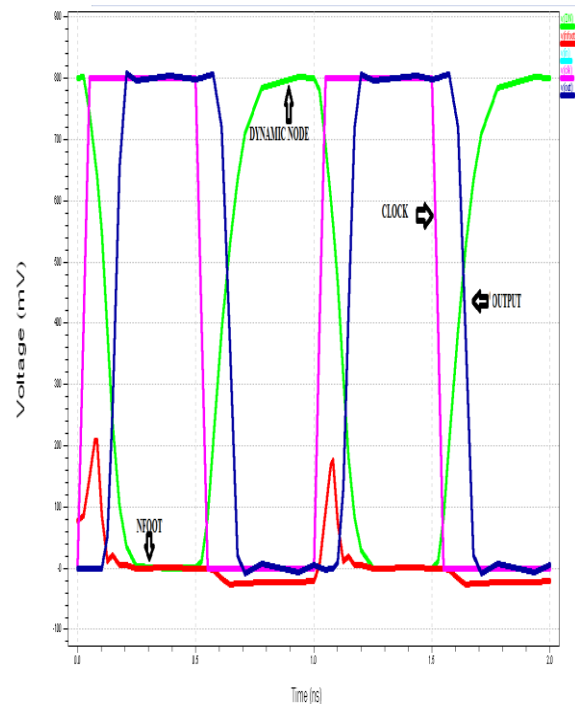


Fig. 8 CEDL waveform for 16 input OR gate

Fig.8 shows the waveform of dynamic node voltage, inputs, clock, NFOOT node and output for 16 input OR gate of CEDL logic style.

TABLE I  
 Result for 16 Input OR gate

CIRCUIT	POWER (uw)	DELAY (ps)	PDP (fF)	#OF TRANSISTORS
FLDL	51.6	174.8	9.01	18
FDL	50.0	185.5	9.25	19
CKDL	45.6	131.7	5.89	23
HSDL	39.7	72.4	2.85	20
CEDL	38.4	121.1	4.59	21

Simulation results of TABLE I shows that the power Dissipation [7] of CEDL circuit is low among rest of circuit topologies. Delay is minimum for HSDL circuit. As seen from Fig.9. PDP is also less for CEDL and HSDL circuit topologies.

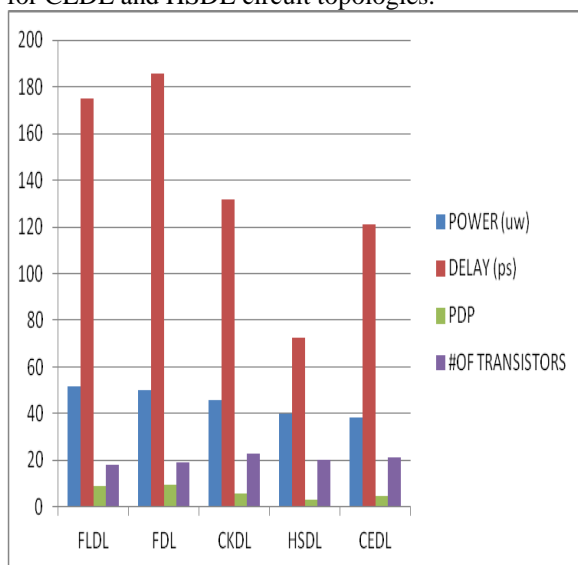


Fig.9.Comparison of power, delay, PDP and number of transistors for all circuit designs.

#### IV. CONCLUSION

In this paper, several domino logic circuit topologies were reviewed for high-speed and leakage-tolerant design. Table I shows 58% improvement in speed of HSDL compared to FLDL. CEDL shows power reduction by 25% compared to FLDL.

HSDL method can be used for very high speed circuits. Both HSDL and CEDL can be used in circuits that needs reduced power consumption.

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