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Effect of bulk traps and gate contact materials on the electrical parameters of FD-SOI device

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Abstract
The aim of study is to find out the effect of bulk traps on various electrical parameters of Full Depleted Silicon on Insulator (FD-SOI) devices, namely, threshold voltage, sub-threshold slope, generation recombination (G-R) current. G-R current depends mainly on the process of fabrication of semiconductor. So, this current involves impurities or traps. In this paper, we modeled FD-SOI using different contact materials, namely, n-polysilicon, Pallidium (Pd), Platinum (Pt), and Tungsten (W), Copper. Iron (Fe) is added as a deep level traps in bulk and generation- recombination current is calculated for various trap density and process parameters.
Keywords: - Bulk traps, Contacts, FDSOI, Threshold voltage.

I. INTRODUCTION

Fully Depleted Silicon on Insulator (FD-SOI) technology depends on a thin layer of silicon over an insulator known as buried oxide (BOX). FD-SOI solves the problem of conventional CMOS device scaling problems with less process complexity [1]-[8]. The result is that the gate has better electrostatic control over the full volume of the transistor body. FD-SOI devices have low Leakage current and good control of short channel effects. Thus, it enables to aggressively shrink gate length so that small transistors can fit into the circuit. The thickness of the top silicon layer for FD-SOI is typically 10 – 25nm.
Any metallic impurities in FD-SOI, if present, introduce deep level traps which is responsible for G-R current. Due to these impurities, new energy levels are introduced in silicon band gap which behave as recombination/generation center. Traps can be divided into two types depending upon its location in energy band diagram of silicon: donor like traps and acceptor like traps. Donor like traps lie below intrinsic Fermi level and acceptor like traps lie above intrinsic Fermi level.

TABLE I
Parameters used to model bulk traps in FD-SOI

Parameter	*Description*
U	Net transition rate
R	Recombination rate
G	Generation rate
n, p	Electron and hole concentration
n_i	Intrinsic carrier concentration
N_t	Trap density
τ_n, τ_p	Electron and hole lifetimes
v_{th}	Electron thermal velocity
σ_n, σ_p	Electron and hole capture cross sections
D_n, D_p	Electron and hole diffusion constants
E_t	Trap energy level
E_i	Intrinsic energy level

For a carrier to be captured by a trap, it must be in the vicinity of the trap. The effective area of trap under which if a carrier is found is captured by trap is known as capture cross section area, σ cm^2. The net transition rate, *U* in a semiconductor is the difference between the recombination rate and generation rate and is determined by:

$$U = R-G \quad (1)$$

U is positive if there is net recombination and negative if there is generation. To evaluate the net G-R rate, we use Shockley Read Hall (SRH) recombination process which gives net recombination rate as [9]:

$$U = \frac{\sigma v_{th} N_t (np - n_i^2)}{n + p + 2n_i \cosh\{(E_t - E_i)/kt\}} \quad (2)$$

In section II, simulation details of FD-SOI and physics of traps in FD-SOI are described. Results and discussions regarding the effect of bulk traps are included in Section III. Section IV outlines the conclusions arrived in this work.

II. SIMULATION DETAILS

A. Test structure:

The electrical parameters of FD-SOI device have been extracted from technology computer-aided design (TCAD) simulations based on mobility model which includes concentration dependent model, parallel electric field dependence, recombination model which includes Shockley-Read-Hall, Auger model. TCAD simulations showing the electrical properties, namely, net doping, threshold voltage, electric potential, electron current density, sub-threshold slope and electric field are presented in Figs.1-6.

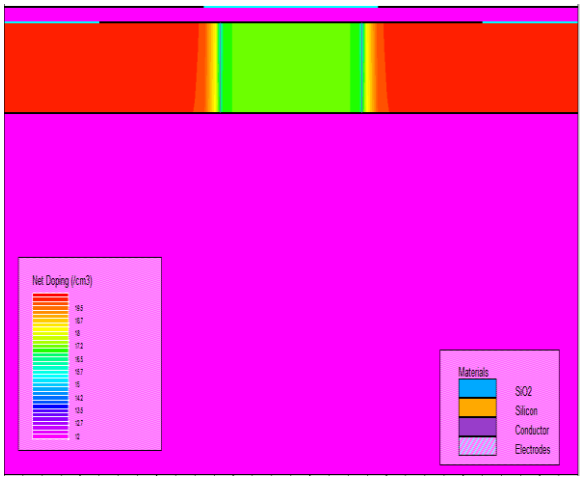

Fig 1: Net Doping in simulated FD-SOI device.

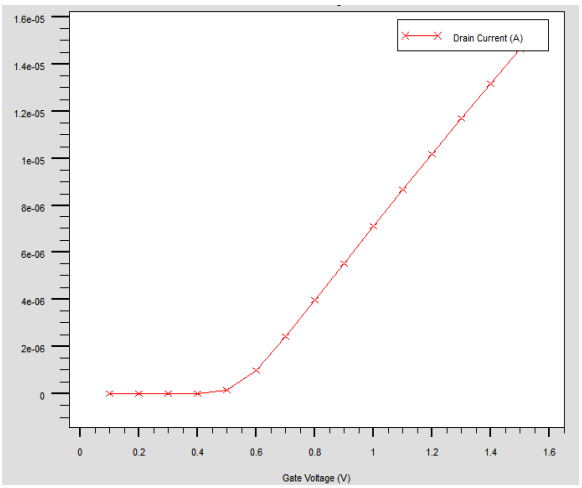

Fig 2: Drain current vs Gate voltage for FD-SOI with n-polysilicon as gate material.

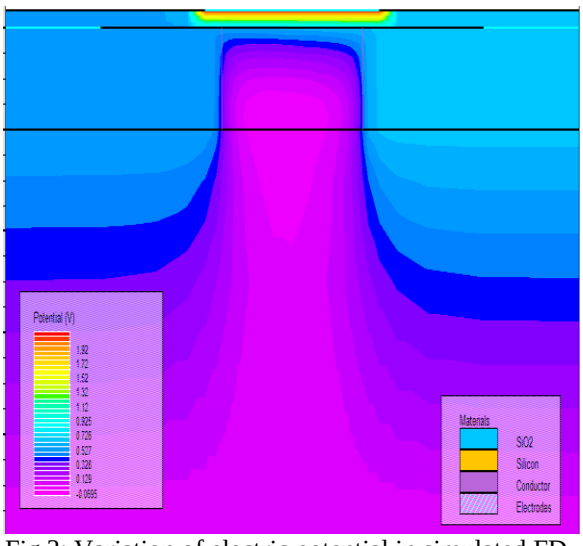

Fig 3: Variation of electric potential in simulated FD-SOI device.

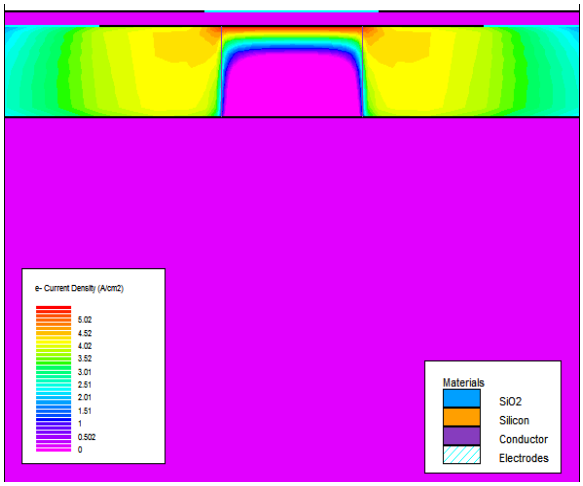

Fig 4: Electron current density in simulated FD-SOI device.

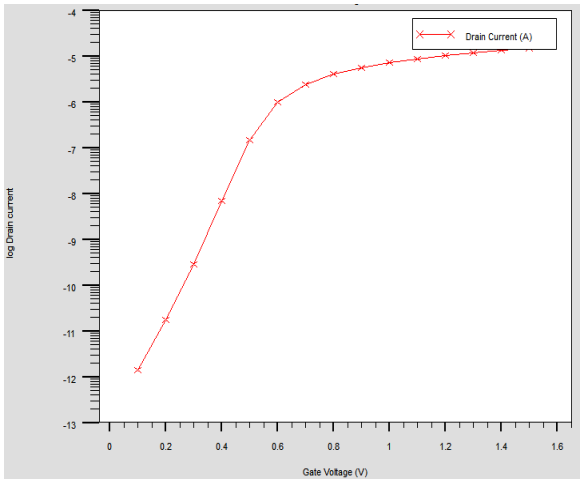

Fig 5: Sub-threshold slope for FD-SOI with n-polysilicon as gate material.

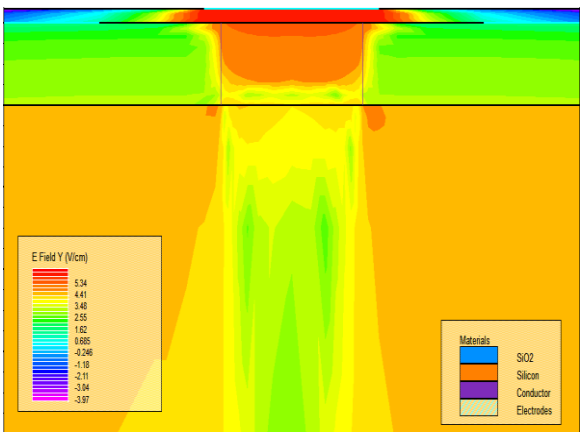

Fig 6: Variation of electric field in simulated FD-SOI device.

B. Traps in FDSOI

In this section, the device operation assisted by bulk traps is analyzed using 2-D simulation. To fabricate high doping profile, high dose implantation

could induce defect or heavy metal contamination, such as Fe, Ni, Zn, etc. [6]. Thus, deep traps namely iron (Fe) have been introduced to study the behavior of device. Dissolved iron in silicon exhibits a donor level in lower half of band gap ($E_t = E_v + 0.39eV$) [10].Fig 7 illustrates the location of trap level in forbidden energy gap of silicon.

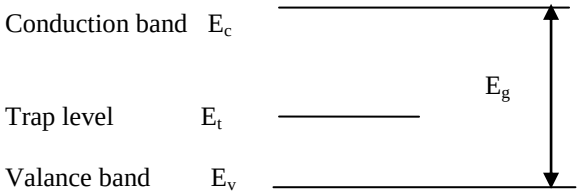

Fig 7: Energy band diagram showing trap level in forbidden gap

Electrical behavior of bulk traps as a carrier-generation center can be understood using energy band diagram. By carrying out 2-D simulation, the carrier distribution is analyzed and results are illustrated in section III. In the present simulation, deep traps are set by the Shockley-Read-Hall, Auger model in the bulk of silicon. It is found that charge carriers are emitted from the trap center.

III. RESULTS AND DISCUSSION

A. Effect of bulk traps on recombination rate in FD-SOI device with different gate material

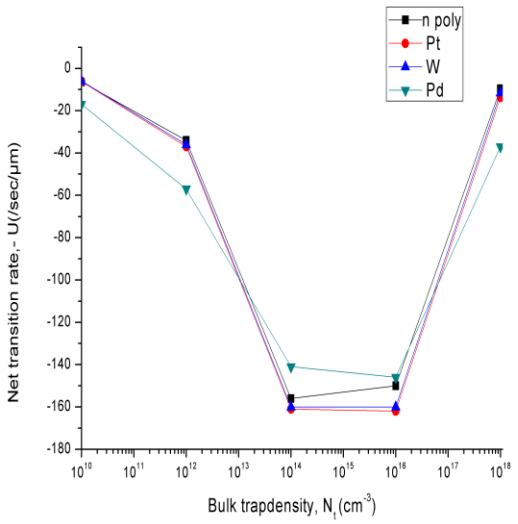

Fig 8: Bulk trap density (N_t) versus Net transition rate (U) for different gate material.

Net transition rate, U, is negative in all cases which implies generation of carriers. Generation rate is lowest when no traps are present and increases as trap density increases. Maximum rate of 160/sec/um is attained for Pt contact and minimum in case of Pd. As trap density increases above 10^{16} cm^{-3}, both generation and recombination of carriers take place and hence net transition rate approaches to zero value.

B. Effect of gate material on the threshold voltage of FD-SOI device

One of the physical component on which threshold voltage depend is the work function difference between the gate and the channel. In the simulation, FD-SOI device is modeled using four different gate materials, namely, n-polysilicon, Palladium, Platinum, and Tungsten. Since Pd has a work function of 5.12 eV, thus, threshold voltage is maximum and is equal to 1.3 V. The minimum value of threshold voltage is obtained using n- polysilicon.

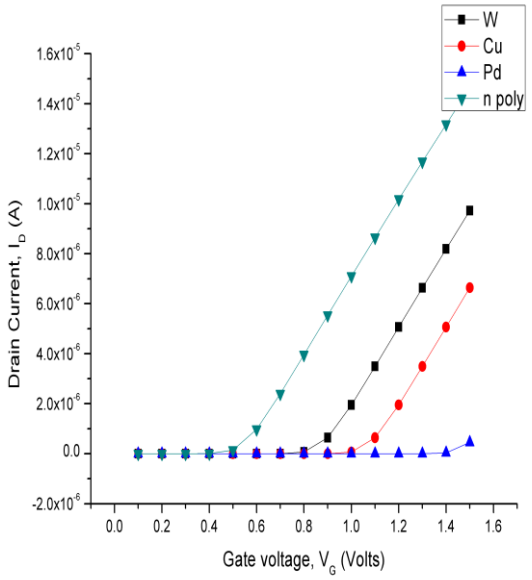

Fig 9: Drain current, I_D, versus Gate Voltage, V_G for different gate materials.

C. Effect of bulk traps on the threshold voltage of FD-SOI device

The value of threshold voltage marginally decreases when bulk trap density increases from 10^{10} to 10^{18} cm^{-3}. However, maximum variation in threshold voltage of 8% takes place in case of n-polysilicon gate material and minimum variation in threshold voltage of 4% takes place in case of Pd gate material.

D. Effect of bulk traps on the sub-threshold slope of FD-SOI device

Sub-threshold slope of 77mV/decade, in case of n-polysilicon, tungsten and palladium gate material remain constant when bulk trap density increases from 10^{10} to 10^{14} cm^{-3}. When bulk trap density increases further to 10^{18} cm^{-3}, sub-threshold slope increases to 100mV/decade. However, in case of Pt

contact, sub-threshold slope decreases from 70mV/decade to 60mV/decade when bulk trap density increases from 10^{10} to 10^{12} cm^{-3}.

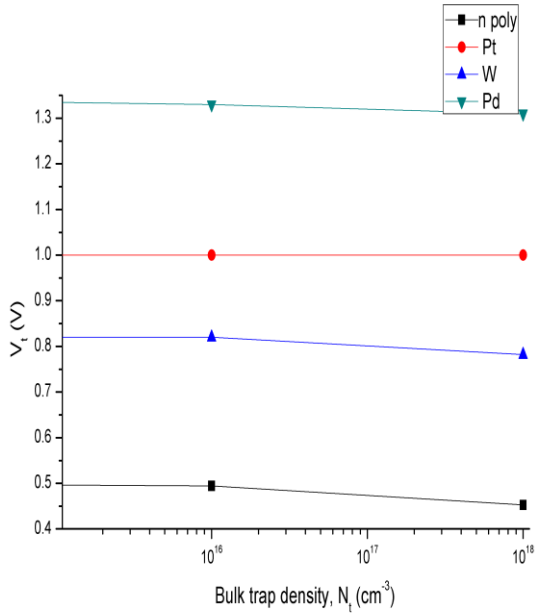

Fig 10: Threshold voltage, V_t versus bulk trap density, N_t for different gate materials.

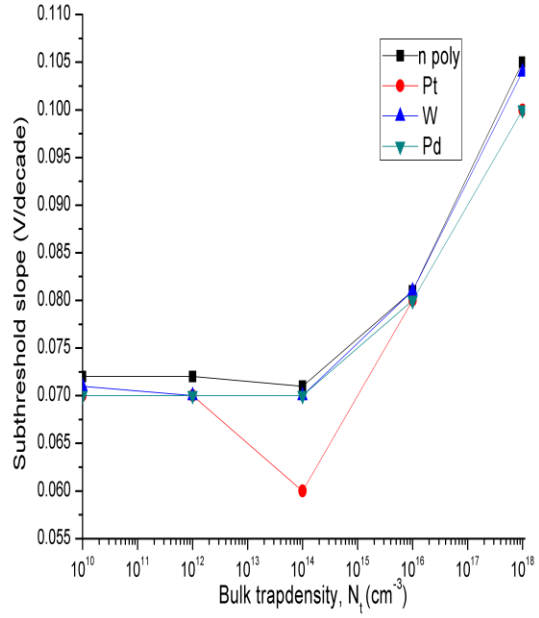

Fig 11: Sub-threshold slope versus bulk trap density for different gate materials.

IV. CONCLUSION

A new FD-SOI device is simulated in which effect of bulk traps and gate materials have been presented. This has been proposed to optimize the value of electrical parameters like threshold voltage, sub-threshold voltage. There is generation of charge carriers in FD-SOI device when bulk traps are present in the substrate. Threshold voltage has lowest value of 0.4 V when n-polysilicon is used as gate material and highest value of 1.2 V when palladium is used. Sub-threshold slope of 70mV/decade is achieved when no bulk traps are present and increases to 100 mV/decade using all gate materials.

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