

Ground Bounce Noise Reduction in Vlsi Circuits

Vipin Kumar Sharma^[1] Umesh Dutta^[2], Sneha Arora^[3], R.P. Sharma^[4]

^[1]M.tech Scholar, Department of Electronics and Communication, FET, Manav Rachna International University, Faridabad, E-mail Id – vipinkumarx2@gmail.com

^[2]Assistant Professor & Deputy Director MRIIC, Department of Electronics and Communication, FET, Manav Rachna International University, Faridabad

^[3]M.tech Scholar, Department of Electronics and Communication, FET, Manav Rachna International University, Faridabad

^[4]Associate Member and Chartered Engineer (I), AMIE (I), Institution of Engineers, India

ABSTRACT: Scaling of devices in CMOS technology leads to increase in parameter like Ground bounce noise, Leakage current, average power dissipation and short channel effect. FinFET are the promising substitute to replace CMOS. Ground bounce noise is produced when power gating circuit goes from SLEEP to ACTIVE mode transition. FinFET based designs are compared with MOSFET based designs on basis of different parameter like Ground bounce noise, leakage current and average power dissipation. HSPICE is the software tool used for simulation and circuit design.

Keywords: Sleep method, Tri mode, Tri transistor, MTCMOS Techniques, Invertor, Power gating, FinFET, Ground bounce

I. Introduction

Signal integrity is a crucial problem in VLSI Circuit and is becoming increasingly important as the minimum feature size of device shrinks to 130 Nano meter and below. A major component of circuit noise is the inductive noise. In fact faster clock speeds and larger no. of devices and i/o drivers as dictated by Moore's law (and therefore larger values of total value of total circuit current) have resulted in increased amount of this type of noise in the power and ground planes (i.e. the di/dt noise, also known as power /ground bounce). It is a critical and challenging design task to control the amount of inductive noise that is inserted into the power planes. Package pins, bonding wires, and on chip IC interconnections all have parasitic inductance.

When an Inductor current varies experiences time-domain variation, a voltage fluctuation is generated across the inductor. This voltage is proportional to the inductance of the chip – package interface and rate of change of the current. As the result when the logic cells in a circuit are switched on and off, the voltage levels at the power distribution lines of the circuit fluctuates [1]. This Ground bounce noise degrades the circuit reliability. Ground bounce noise is important issues in MTCMOS circuit [2]. In MTCMOS circuit when transistors of MTCMOS circuit from the SLEEP to ACTIVE mode, an instantaneous currents flow through the SLEEP transistor and the large amount of Voltage fluctuations occurs on both the real Ground and the real Power line[3].

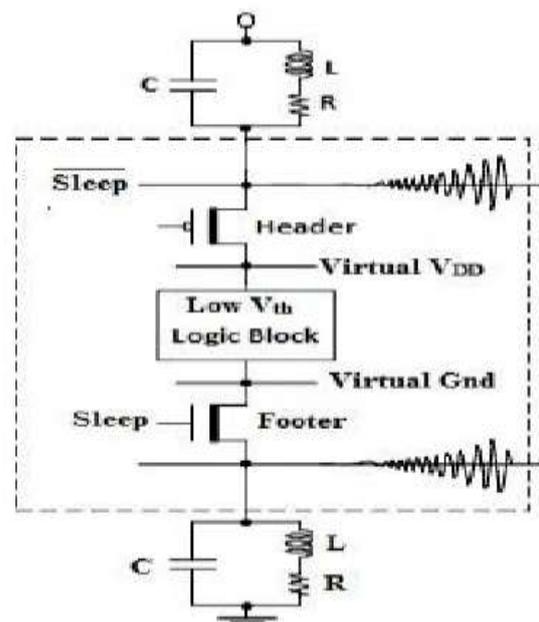


Figure 1: Ground and power bouncing in MTCMOS circuit [2]

In this paper, we have designed an invertor using FinFET technology in 32nm technology and ground bounce noise is measured and compared with the MOSFET counter-part in 32nm technology.

This paper is organised as follows: Ground Bounce Noise is explained in brief in Section 2. FinFET basics are presented in Section 3. Power gating techniques are explained in Section 4. In Section 5, proposed techniques are described followed by simulation results in Section 6.

II. Ground Bounce Noise in VLSI Circuit

Ground Bouncing noise is the primary cause of false switching in high speed circuits and a major cause of poor signal quality [4]. MTCMOS is the popular leakage power minimization strategy and it is also called power gating technique.

Power gating circuits, use high threshold voltage (high- V_{th}) SLEEP transistors (head and footer) which cut off the power supply or the ground connection to the low threshold (low- V_{th}) circuit block [4]. During transition of MTCMOS circuit from the SLEEP to the ACTIVE mode an instantaneous current flow through the SLEEP transistors and large amount of voltage fluctuation occurs on the both the end. Through the shared ground and power distributed network during wake up event the bouncing noise generated in one domain is transferred to the active block which will flipped the logic states o internal nodes distributed SLEEP transistors which shows the higher savings in leakage power consumption. This noise is known as ground bounce noise.

2.1 Factor Affecting Ground Bounce in VLSI Circuits:

The ground bounce noise is produced by capacitive and inductive of pins of package on chip bonding wires and power distribution network. The package parasitic impedances play major role in ground bouncing noise generation. Some factor affecting the ground Bounce noise are power supply voltage, magnitude of current surge, voltage swing of virtual ground during wakeup, output and ground inductance valves, output pin location, number of output switching, sleep and controlling transistor size, temperature , threshold voltage and the device technology [2].

III. FinFET

FinFET in classified as a type of magnitude metal oxide semi conductor field affect transistor/MSFET It was first developed at the university of Berkley California by Chenning Hu and his colleagues A Multi-Gate transistor incorporates more than one gate in to one single device. To minimize the short channel effect FinFET can be used in place of conventional CMOS circuits [8]. FinFET (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or bulk CMOS at 22-nm and beyond, offer interesting delay–power tradeoffs. Both CMOS logic and pass transistor logic were developed for conventional NMOS and PMOS transistor.

In FinFET the NMOS in CMOS technology is replaced with N-FinFET and PMOS with P-FinFET, then, both gates of FinFET are tied together. By using this approach, we can design a FinFET version of a CMOS logic circuit or a pass transistor logic circuit

that retains the same functionalities as the MOSFET version. In the mean time, FinFET provides better circuit performances and reduces leakage current through effective suppression of short-channel effect and near-ideal sub-threshold swing [9].

IV. Power Gating Techniques:

Multi threshold CMOS (MTCMOS) also known as power/ ground gating, is the most commonly used circuit technique for leakage power and ground bounce reduction [5]. There are different types of power gating techniques:

4.1 Tri mode MTCMOS Technique:

An intermediate PARK mode is introduced between the sleep mode and the active mode to lower the ground bouncing noise during transition A high - $|V_m|$ pmos transistor is connected in parallel with the footer sleep transistor (N1) as shown in the Figure 2. Now during the sleep mode both N1 and the parker transistor are turned off to reduce the sub-threshold leakage current of an idle circuit. The voltage of virtual ground line is maintained at VDD during SLEEP mode. The voltage of virtual ground live is maintained at VDD during the sleep mode. During transistors time before switching on the sleep transistor, Parker is turned on first and N1 is maintained cut-off.

The circuit transitions to the intermediate PARK mode. The virtual ground line is discharged to the threshold voltage of parker ($|V_{EP}|$). The ground bouncing noise is suppressed due to the lower range of the voltage swings on the virtual ground line with the two step transition from SLEEP mode to the ACTIVE mode through the intermediate PARK mode as shown in Figure 2.

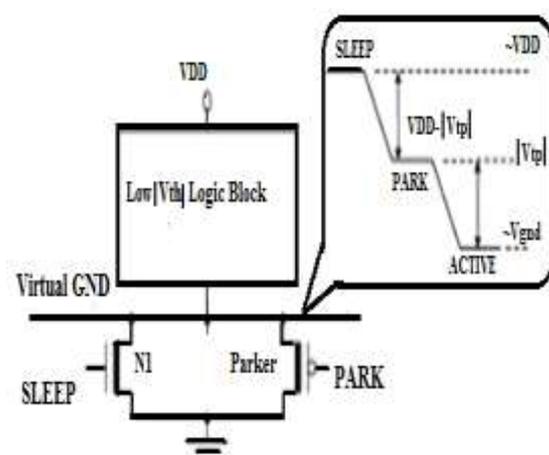


Figure 2: Tri-mode power gating structure with high V_{th} SLEEP and PARK Transisto [2]

4.2 Dual mode MTCMOS Technique:

In dual switch technique [6], an intermediate HOLD mode is introduced to suppress the ground

bouncing noise, similar to Tri-mode [4]. It is an alternative method to suppress the ground bounce in gated- & ground structure.

As shown in Figure 3, A high- V_{th} NMOS transistor is connected in parallel to the header sleep transistor connected in between real power line and virtual power line. Similarly high- V_{th} PMOS Transistor is connected in parallel to the footer sleep transistor which is connected in between the real ground and the virtual ground line. In an intermediate HOLD P2 and N2 high V_{th} transistor are turned on and the header (P1) and the footer (N1) are maintained at cut-off mode. In the SLEEP mode, all the transistors i.e. Sleep transistors (P1, N1) and Dozer transistor (P2, N2) are turned off which reduces the sub-threshold leakage current. The voltages maintained at virtual power and ground lines are approximately equal to (V_{mid}).

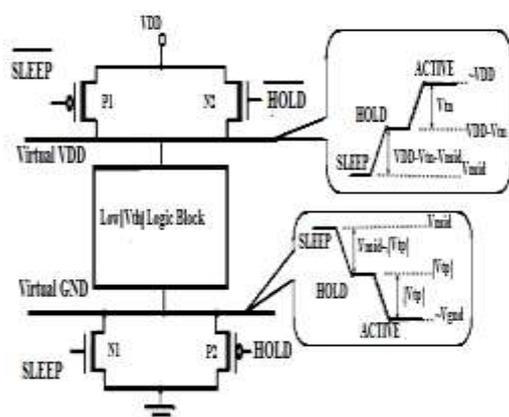


Figure 3: Dual Mode MTCMOS Technique [2]

Before the activation of the circuit, The circuit transitions to the intermediate HOLD mode i.e. from the SLEEP mode to the HOLD mode. $V_{DD} - V_{in} - V_{tp}$ voltage is produced between the virtual lines. And from the HOLD mode to the ACTIVE mode transition P1 and N1 are activated. The virtual power line and ground line is charged and discharged to $\sim V_{DD}$ and $\sim V_{gnd}$. HOLD mode reduces the voltage swing range which reduces the amplitude of Ground bouncing noise [2].

4.3 Tri-Transistor-Controlled MTCMOS Technique:

In tri-Transistor-controlled MTCMOS technique, to implement the intermediate DOZE mode for ground bouncing noise suppression from SLEEP to Active mode, a high- V_{th} PMOS sleep transistor (called Dozer) is connected in parallel with the footer [7].

As shown in Figure 4, in the SLEEP mode, all the transistors i.e Sleep transistors and Dozer transistor are turned off which reduces the sub threshold leakage current. In the DOZE mode, the Dozer and header are turned on. The footer is at cut-

off mode. In ACTIVE mode, the header and footer are turned on. The MTCMOS circuit operates with high speed .The SLEEP mode is the preferable mode of operation for minimizing the leakage power consumption. DOZE mode is an intermediate mode during SLEEP to ACTIVE mode to suppress the ground bouncing noise. The virtual power line is charged from intermediate voltage level V_{mid} ($0V < V_{mid} < V_{DD}$) towards $\sim V_{DD}$ and the virtual ground line is discharged from V_{mid} towards the threshold voltage of the Dozer. At the end of the intermediate transition period, to complete the circuit activation process, footer transistor is turned on.

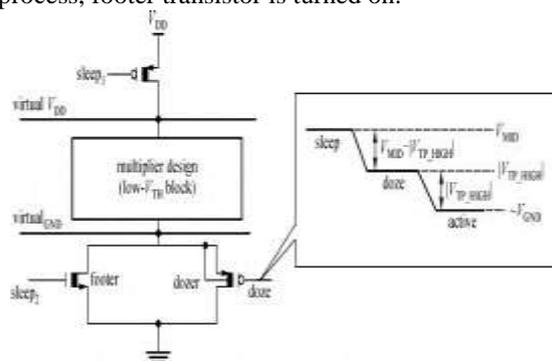


Figure 4: Tri-Transistor- controlled MTCMOS Technique [3]

During the transition from DOZE mode to the ACTIVE mode, the virtual ground line is discharged from V_{tp} to $\sim V_{gnd}$. Two-step wake-up process reduces the range of voltage swing on the virtual ground line which will reduce the ground bouncing noise To reduce the transition delay from the SLEEP to the DOZE mode, a low- V_{th} Dozer can be used, as shown in Fig.4. Tri-transistor-controlled MTCMOS with high- V_{th} dozer transistor (TTH) and the tri-transistor-controlled MTCMOS with low- V_{th} dozer transistor (TTL) of the tri-transistor-controlled technique is used for ground bouncing noise reduction.

V. Proposed Techniques:

Power gating techniques has been proposed using FinFET device in 32nm technology. The power gating techniques has been applied on FinFET to improve ground bounce noise, leakage current and power dissipation in logic circuits. The techniques applied are implemented on inverter logic circuit.

5.1 TRI-Mode Inverter FinFET:

- A high- p-FinFET data preserving transistor (Parker) is connected in parallel with the footer to implement a low leakage data retention PARK mode in idle inverter.
- Sleep transistor (M3) and the Park transistor are turned off in SLEEP mode to reduce the sub-threshold leakage current of an idle circuit.

- During the PARK mode, the Parker is activated while M3 is maintained at cut-off. The virtual ground line is maintained at the threshold voltage of the Parker.

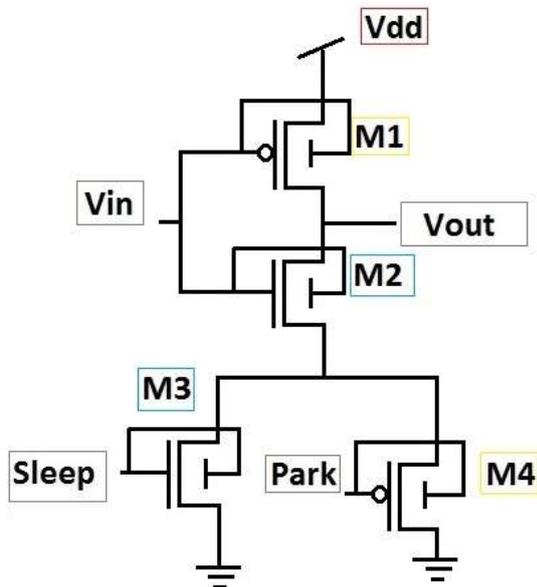


Figure.5. Tri-Mode Technique applied on FinFET inverter

- The circuit is at intermediate PARK mode and since the virtual ground line is discharge to the threshold voltage of Park transistor lower the voltage swing range, which reduces the amplitude of ground bouncing noise. The footer sleep transistor is turned on and the Park transistor is turned off.
- The virtual ground line is discharge to $\sim V_{gnd}$ to complete the reactivation process, and to fully activate the circuit.

5.2 Dual Mode Inverter FinFET:

- In the SLEEP mode, all the transistors i.e. Sleep transistors (M1, M5) and Dozer transistor (M2, M6) are turned off which reduced the sub-threshold leakage currents as in Figure 6.
- In an intermediate HOLD, M6 and M2 transistors are turned on and the header (M1) and the footer (M5) are maintained at cut-off mode.
- The voltages maintained at virtual power and ground lines are approximately equal to (V_{mid}).

The circuit transitions to the intermediate HOLD mode i.e. from the SLEEP mode to the HOLD mode. $V_{DD} - V_{tn} - V_{tp}$ voltage is produced between the virtual lines. From the HOLD mode to the ACTIVE mode transition M1 and M5 are activated.

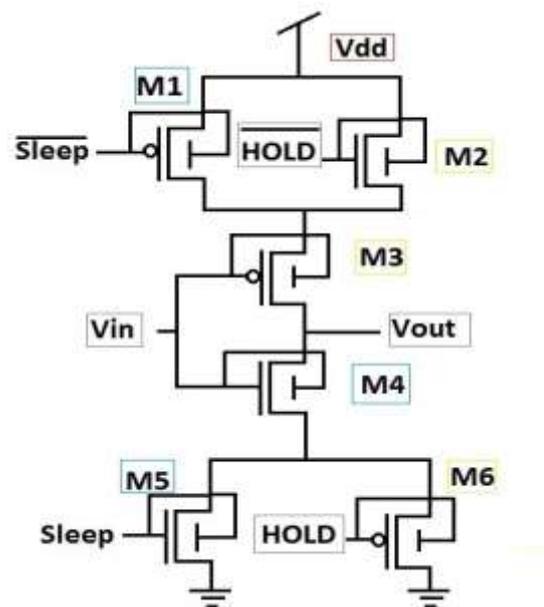


Figure.6. Dual Mode technique applied on FinFET Inverter

The virtual power line and ground line is charged and discharged to $\sim V_{DD}$ and $\sim V_{gnd}$. HOLD mode reduces the voltage swing range which reduces the amplitude of Ground bouncing noise

5.3 Tri-transistor Technique FinFET:

In tri-Transistor-controlled MTCMOS technique, to implement the intermediate DOZE mode for ground bouncing noise suppression from SLEEP to Active mode a High- V_{th} PMOS sleep transistor (called Dozer) is connected in parallel with the footer [18], as shown in Figure 7.

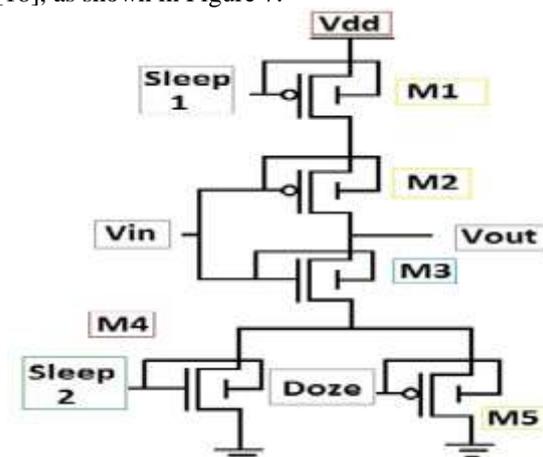


Figure 7: Tri transistor technique applied on FinFET inverter

In the SLEEP mode, an additional high V_{th} p-FinFET sleep transistor (Dozer) is connected in parallel with the footer to implement an intermediate DOZE mode in MTCMOS circuits. The SLEEP state would be the preferable mode of operation to

minimize the leakage power consumption. DOZE mode would be visited as an intermediate step during the SLEEP to ACTIVE mode transitions in order to suppress the ground bouncing noise.

VI. Simulation Results:

In Figure 8, it clearly states that the ground bounce noise is reduced by using FinFET instead of MOSFET. The least ground bounce noise is in the Dual-Mode technique FinFET. The results are also shown in tabular form.

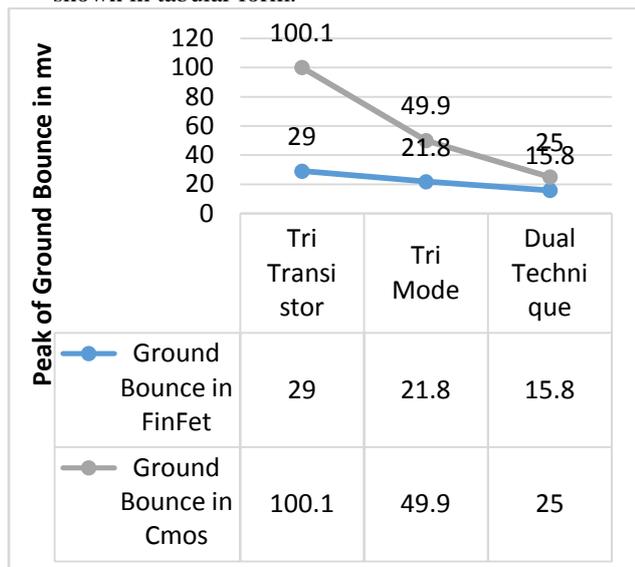


Figure 8: Ground Bounce Noise Comparison

Figure 9 shows the comparative analysis between FinFET and MOSFET designs on the basis of Average power consumption. FinFET devices are low power and have better control on channel of the transistor.

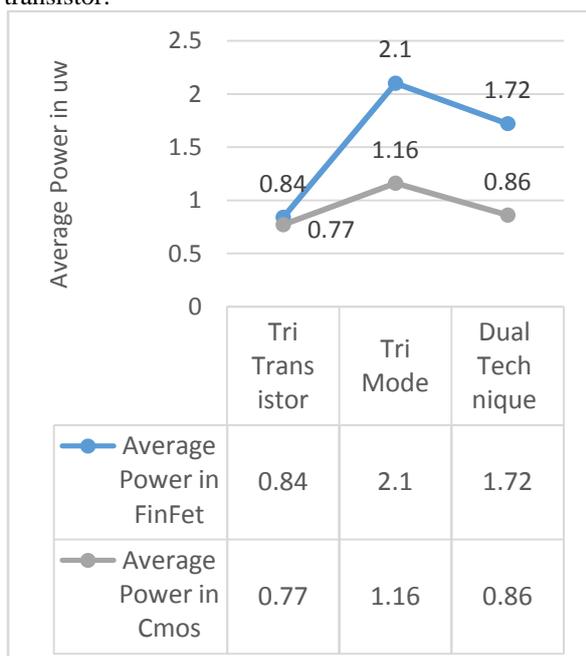


Figure 9: Average Power Comparison

Figure 10 shows that the leakage current is reduced by using FinFET as it has better sub-threshold swing. Dual Mode technique has the minimum leakage current.

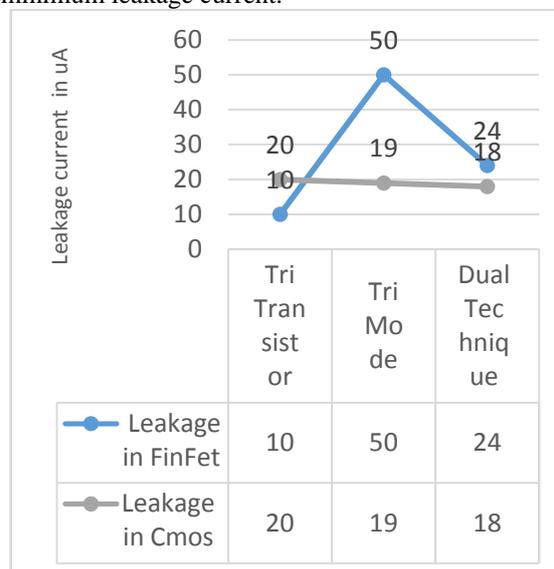


Figure 10: Average Power Comparison

VII. CONCLUSION

Tri-transistor technique using FinFET is best in terms of leakage current and average power. Ground bounce noise is reduced three times in FinFET when compared to MOSFET. Leakage current is reduced two times in tri transistor FinFET. 1% average power consumption is increased in tri transistor mode. Dual Mode technique has the least ground bounce noise. It is clear in the simulation results, that with the use of FinFET over MOSFET, the ground bounce noise problem is reduced.

REFERENCES

- [1] P. Heydari and M. Pedram, "Ground Bounce in Digital VLSI circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 11, No. 2, pp. 180-185, April 2003.
- [2] Nisha, Mr. Anup Kumar, Ms. Geetika Goyal, A Review of Ground-Bouncing-Noise Minimization Techniques in MTCMOS Circuits, *IJRITCC*, July 2014
- [3] J. C. Park and V. J. Mooney, Sleepy Stack Leakage Reduction, *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 11, pp. 1250-1263, November 2006.
- [4] S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, D. Heidel, and M. Immediato, Minimizing Inductive Noise in System-on-a-chip with Multiple Power Gating Structures,

in *Proc. European Solid- State Circuits*, pp. 16-18, 2003

- [5] D Ashok kr reddy, Mohammed mohasinulhuq, Noise Migigation in loe leakage MTCMOS circuit, IJECE, volume 1, issue-2, 2013
- [6] M. H. Chowdhury, J. Gjanci, and P. Khaled, Controlling ground bounce noise in power gating scheme for system-on-a-chip, in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI*, Apr. 2008, pp. 437–440.
- [7] H. Jiao and V. Kursun, Ground bouncing noise suppression techniques for MTCMOS circuits, in *Proc. IEEE Asia Symp. Quality Electron. Des.*, Jul. 2009, pp. 64–70.
- [8] Neha Yadav, Modelling and Performance Analysis of Various FinFET Based Design Techniques for XOR and XNOR Circuits at 45 Nanometer Regime, *International Journal Of Advanced Electronics & Communication Systems*, Issue 2 Vol 3, Apr-May-2014
- [9] Prateek Mishra, Anish Muttreja and Niraj.K.Jha; et. al “FinFET Circuit Design”.



^[4] **R.P. Sharma**, retired Indian Air Force, Electrical and Electronics Engineers Department and B.Sc in biological science. He is an Associate Member and Chartered Engineer of AMIE, The Institution of Engineers, India. His expertise includes Research and Development of Industrial Machines, Analog and Digital VLSI design, CPC machines.

About Authors



^[1] **Vipin Kumar Sharma**, received B.Tech. degree from the Bharti Vidyapeeth University, Pune, Maharashtra, India, in 2013, and M.Tech. Scholar from MRIU, Haryana, India in 2015. His current research interests include low power VLSI design, analog IC design and computer architecture, Embedded Systems and Robotics.



^[2] **Umesh Dutta**, Assistant Professor and Deputy Director, MRIIC in Manav Rachna International University where he received many awards for teaching excellence and Researches done in various areas. His area of interest is in VLSI and Embedded Systems.



^[3] **Sneha Arora**, received B.Tech. degree from the Rajasthan Technical University, Kota, Rajasthan, India, in 2012, and M.Tech. Scholar from MRIU, Haryana, India in 2015. Her current research interests include interesting problems in device modeling, simulation of multigate transistors, as well as low power digital circuit design, and computer architecture/VLSI implementations of architectural ideas, and Embedded Systems, Microcontrollers.