

Power Gating Based Ground Bounce Noise Reduction

M. Uma Maheswari*, Mrs. K. Srilakshmi**

*M.Tech, Embedded systems, Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, A.P. India

**Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, A.P. India

ABSTRACT

As low power circuits are most popular the decrease in supply voltage leads to increase in leakage power with respect to the technology scaling. So for removing this kind of leakages and to provide a better power efficiency many power gating techniques are used. But the leakage due to ground connection to the active part of the circuit is very high rather than all other leakages. As it is mainly due to the back EMF of the ground connection it was called it as ground bounce noise. To reduce this noise different methodologies are designed. In this paper the design of such an efficient technique related to ground bounce noise reduction using power gating circuits and comparing the results using DSCH and Microwind low power tools. In this paper the analysis of adders such as full adders using different types of power gated circuits using low power VLSI design techniques and to present the comparison results between different power gating methods.

Keywords- power gating, leakage current, stacking, ground bounce noise.

I. Introduction

Low power design is the recent design technology. Presently there are many portable devices like laptop, tablet PC, mobile phone, etc. run on batteries. The power dissipation in these devices is high because low power components are supplied with high voltages. For example, if an amplifier circuit is working with low input power then the output should be capable of driving a loud speaker. The complexity for the high speed devices is more. Thermal problems arise due to more hardware in a integrated packing, so there is heat dissipation due to compact packing. So, there is a need to provide heat sinks and cooling fans for heat exhausting.

To minimize the power consumption and to increase the battery life time, so different low power designs are used. Low power design by reducing the power dissipation increases the system performance. Low power design is responsible for discussion of the power in micro and nano watts. There are different low power design techniques.

i) Clock gating

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

ii) Multi-threshold CMOS (MTCMOS)

This is a body-biasing technique. Variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power. Low V_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low V_{th} devices have substantially higher static leakage power. High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage.

iii) Transistor stacking

This technique is a leakage reduction technique which works both in active and stand-by mode. It is based on the observation that two off-state transistors connected in series cause significantly less leakage than a single device.

iv) Dynamic Threshold MOS (DTMOS)

In this technique the transistors are provided with varying threshold voltages. Instead of this different logic gates are provided with different threshold voltages due to this the leakage current i.e. power dissipation will be less when compared to multi threshold MOS technique. This is used to reduce the active leakage power.

v) Dynamic voltage scaling(DVS)

Dynamic supply scaling overrides the cost of using two power supplies (static supply scaling), by adapting the single voltage to the performance demand. The highest supply voltage delivers the

highest performance at the fastest designed frequency of operation. When performance demand is low, supply voltage and clock frequency are lowered, just delivering the required performance with substantial power reduction.

vi) Dynamic frequency scaling (DFS)

This technique is also known as 'CPU throttling', is a technique in computer architecture whereby the frequency of a microprocessor can be automatically adjusted "on the fly," either to conserve power or to reduce the amount of heat generated by the chip. Dynamic frequency scaling is commonly used in laptops and other mobile devices, where energy comes from a battery and thus is limited. It is also used in quiet computing settings and to decrease energy and cooling costs for lightly loaded machines. Less heat output, in turn, allows the system cooling fans to be throttled down or turned off, reducing noise levels and further decreasing power consumption.

vii) Near Sub threshold supply

In this technique the supply voltage is scaled down such that the devices are also scaled down. So the devices can be operated at sub threshold voltage. The disadvantage in this technique is when the component is used just above the threshold voltage then there can be an electron migration in the transistors used in the circuit.

Power gating is a technique used in IC design to reduce power dissipation, by turning off the current to blocks of the circuit which are not in use. In addition to reduce the stand-by or leakage power in the circuits in the circuits those are implemented by this technique.

Power gating will affect the design architecture. It increases delay; as power gated modes have to be operated in multi modes. In Power gating low-leakage PMOS transistors are used as header switches to turn off power supply to various parts of a design in standby or sleep mode and NMOS footer switches are used as sleep transistors. Inserting the sleep transistors, will split the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

Typically high-V_t sleep transistors are used for power gating. The sleep transistor sizing is an important design parameter. Power gating can be implemented using cell-or (cluster-based) and fine grain approaches or a distributed coarse-grained approach. Different approaches for power reduction.

1. Power dissipation in CMOS

Broadly classifying, power dissipation in CMOS circuits occurs because of two components:

Static dissipation

- **Sub threshold conduction when the transistors are off.**

Both NMOS and PMOS transistors have a gate-source threshold voltage, below which the current (called *sub threshold* current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{DD} might have been 5 V, and V_{th} for both NMOS and PMOS might have been 700 mV). A special type of the CMOS transistor with near zero threshold voltage is the native transistor.

- **Tunneling current through gate oxide.**

SiO₂ is a very good insulator, but at very small thickness levels electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunneling current becomes very important for transistors below 130 nm technology with gate oxides of 20 Å or thinner.

- **Leakage current through reverse biased diodes. [8]**

Small reverse leakage currents are formed due to formation of reverse bias between diffusion regions and wells (for e.g., p-type diffusion vs. n-well), wells and substrate (for e.g., n-well vs. p-substrate). In modern process diode leakage is very small compared to sub threshold and tunneling currents, so these may be neglected during power calculations.

Dynamic dissipation

- **Charging and discharging of load capacitances.**

CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total of Q=C_LV_{DD} is thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device:

$$P=CV^2f \quad (1)$$

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor α , called the activity factor. Now, the dynamic power dissipation may be re-written as .

$$P= \alpha CV^2f \quad (2)$$

A clock in a system has an activity factor $\alpha=1$, since it rises and falls every cycle. Most data has an activity factor of 0.1 If correct load capacitance is estimated on a node together with its activity factor,

the dynamic power dissipation at that node can be calculated effectively.

- **Short circuit power dissipation**

Since there is a finite rise/fall time for both pMOS and nMOS, during transition, for example, from off to on, both the transistors will be on for a small period of time in which current will find a path directly from V_{DD} to ground, hence creating a short circuit current. Short circuit power dissipation increases with rise and fall time of the transistors.

As wires on chip became narrower and the long wires became more resistive. CMOS gates at the end of those resistive wires see slow input transitions. During the middle of these transitions, both the NMOS and PMOS logic networks are partially conductive and current flows directly from V_{dd} to V_{ss} . The power thus used is called *crowbar* power. Careful design which avoids weakly driven long skinny wires has ameliorated this effect, and crowbar power is nearly always substantially smaller than switching power.

There are certain leakage power reduction techniques that provide low leakage power dissipation by using the leakage power reduction design techniques. The different techniques used in leakage power reduction techniques include [1] [2]:

- i) Multiple supply voltage
- ii) Multiple threshold voltage
- iii) Transistor stacking
- iv) Power gating
- v) Variable body biasing

In this work, among these techniques the power gating technique is used to minimize the leakage power dissipation. Therefore, by using multi threshold supply voltages delay increases, no memory retention, and no short circuit protection but these are provided with Coarse-grain power gating technique which is a technique in power gating. The dynamic power consumed by the transistors depends on the switching frequency of the signal that is applied at the gate of the transistor, full supply voltage and the load capacitance used.

Supply voltage scaling was developed for switching power reduction. It is an efficient method for reducing switching power. It also helps to reduce leakage power because the sub-threshold leakage is due to Gate Induced Drain Leakage (GIDL) and Drain Induced Barrier Leakage (DIBL) these are also reduced as well as the gate leakage component when the supply voltage is scaled down. Static supply voltage scaling is a multiple supply voltage where as different supply voltages are provided. In order to satisfy the speed performance the critical and non-critical paths are made to operate with same speed without disturbing the system performance.

Ground bounce, also known as simultaneous switching noise or delta noise, is a voltage glitch induced at power ground distribution connections due to switching current passing through either wire substrate inductance or package lead inductance associated with power or ground rails [3]. These voltages glitches or surge phenomena are proportional to $L (dI/dt)$ [3]. [7]. Ground bounce noise is an important issue in the design of nanometer circuits and this inductive noise is also associated with clock gating [8] - [12]. Taking into account technology trends ground bounce due to internal logic has become an important issue in the design of high performance integrated circuits. This is mainly due to the increased speed and higher density in scaled-down technologies.

II. Design Principles

Transistors are designed in such a way that the width of the gate should be more when compared with the length of the channel this is made such that the for applied gate voltage the channel must be formed for logic high in NMOS and logic low in PMOS transistors. If the insulator used at the gate of the MOS transistor is of very less width than the channel length, hence if the transistor is OFF even though certain current flows due to charge induced due to capacitance effect. To reduce the leakage current the length and width of MOS transistor is made suitably for low voltage applications that for power gating technique.

III. Power dissipation

Power dissipation is reduced by reducing the length of the channel and width of the gate of transistors [3]. This is the easy way to reduce the power consumption of a transistor without disturbing its operation. The low voltage operation is that the conduction of transistor due to diffusion of charge carriers. Static power essentially consists of the power used when the transistor is not in the process of switching.

$$P_{static} = I_{static} * V_{dd} \quad (3)$$

Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power consumption (P_{cap}). $P_{transient}$ represents the amount of power consumed when the device changes logic states. Capacitive load power consumption is the power used to charge the load capacitance.

$$P_{dynamic} = P_{cap} + P_{transient} \\ P_{dynamic} = (C_L + C) * V_{dd}^2 * f * N^3 \quad (4)$$

Where 'N' is the number of logic values that are switching, 'f' is the switching frequency. The short circuit power depends upon the frequency of the transition. Hence the total power dissipated is the sum of all the power dissipations in the circuit.

$$P_{total} = P_{static} + P_{sc} + P_{dynamic} \quad (5)$$

The total power dissipated is the sum of static power dissipated, short circuit power and the dynamic power consumed by the circuit. A way to reduce leakage power consumption is to raise the V_{th} of some gates. This technique can be applied to any digital circuit

Power gating technique is used to reduce the leakage power .It uses high threshold voltage sleep transistors which cut off VDD from a circuit block when the block is not switching. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors.

IV. Implementation of power gating technique

The stack approach provides a solution for leakage power reduction; there are different types of stacking power gating techniques they are

i) Sleepy stack approach[3]

Another technique for leakage power reduction is the Stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors Figure 4.1 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

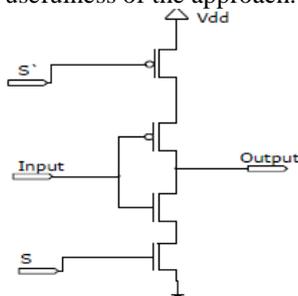


Fig: 4.1 Sleepy stack approach

The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

ii) Dual sleep stack approach

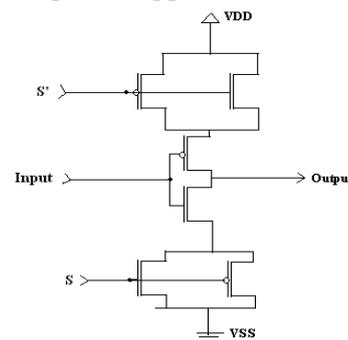


Fig: 4.2 Dual sleep stack approach

Another technique called Dual sleep approach shown in fig: uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

iii) Sleepy approach

In the sleep approach, a "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Gnd. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

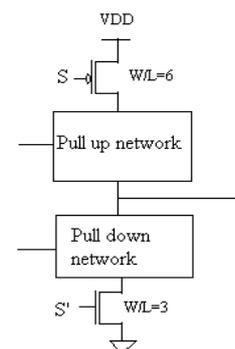


Fig: 4.3 Sleepy approach

iv) Sleepy keeper

In this leakage reduction technique, which is called as the "sleepy keeper" approach? This section explains the structure of the sleepy keeper approach as well as how it operates. In addition, some layout issues for the sleepy keeper approach. The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to

VDD and NMOS transistors connect to GND. It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing VDD.

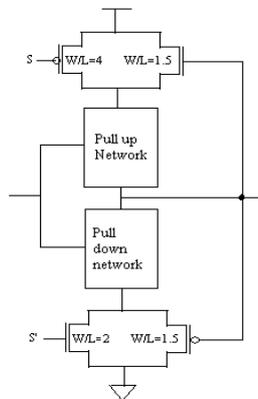


Fig: 4.4 Sleepy keeper approach

V. Dual stack

The dual stack method has noise efficiency & power efficiency than normal full adders. Dual stack technique that reduces not only leakage power but also dynamic power. Here the use of two PMOS in the pull-down network and two NMOS in the pull up Network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level.

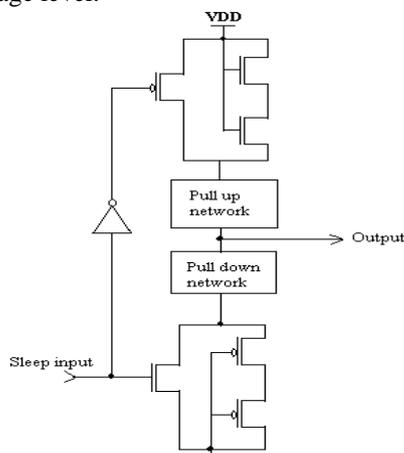


Fig: 4.5 Dual stack approach

So, the pass transistors decreases the voltage applied across the main circuit. As the static power is proportional to the voltage applied, with the reduced voltage the power decreases but there is the advantage of state retention [10].

VI. Results

Any CMOS circuits can be designed by implementing the power gating. The full adder has been designed as shown in below figures

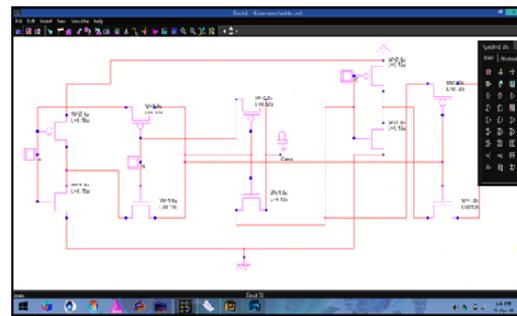


Fig: 5.1 Full adder schematic

The above designed schematic is full adder using CMOS transistors. This circuit has some leakage power when no input is given. The layout of the designed circuit is shown in figure 5.2.

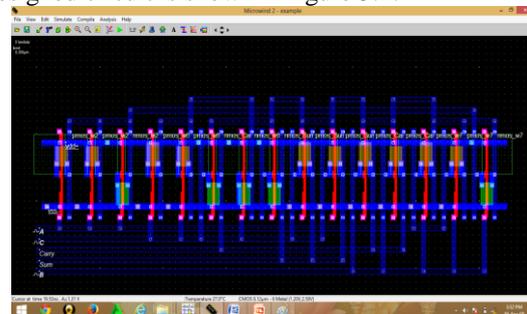


Fig: 5.2 Full adder layout

The layout of the full adder is obtained by using microwind tool.

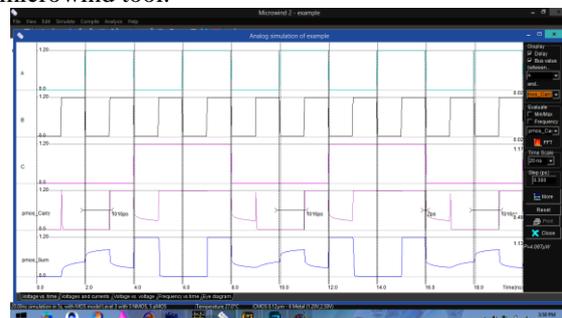


Fig: 5.3 Full adder waveform

The output waveform of full adder is shown in figure 5.3. The total power dissipation is also obtained

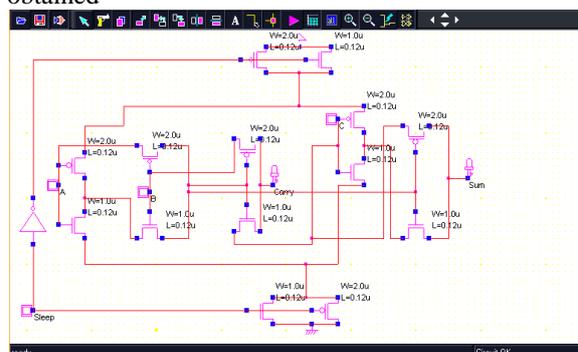


Fig: 5.4 Dual Sleep Circuit

In the above designed circuit the sleep transistors are connected in parallel (PMOS and NMOS). This allows the use of conduction of sleep transistors either for low and high. The input signals are A, B, C and sleep signal. The power dissipation is little higher than dual stack. This is due to the parallel NMOS and PMOS sleep transistors.

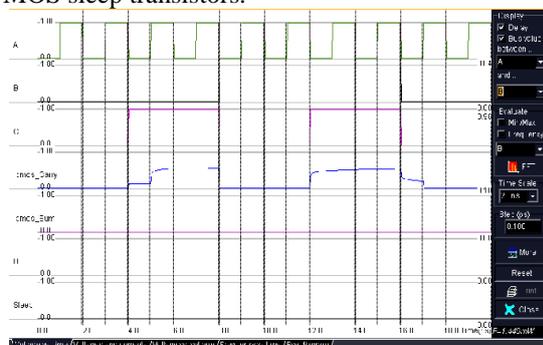


Fig: 5.5 Dual sleep output

In the output waveform of dual sleep full adder circuit the inputs are a, b, c and sleep signals. Depending upon the inputs applied the outputs are obtained.

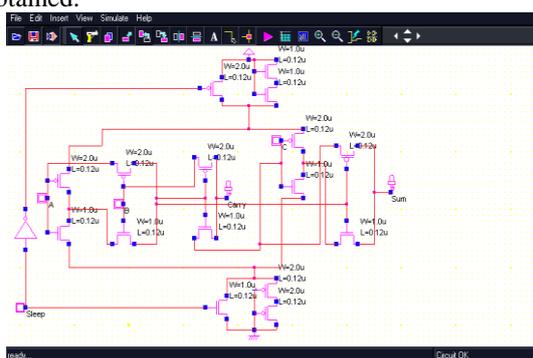


Fig: 5.6 Dual Stack circuit

In the above designed circuit the power supply is applied directly to the gate, there is a sleep transistor by which the voltage is applied to the below transistors, the dual stack is a process of placing the transistors in series. So the power dissipation is reduced to a great extent.

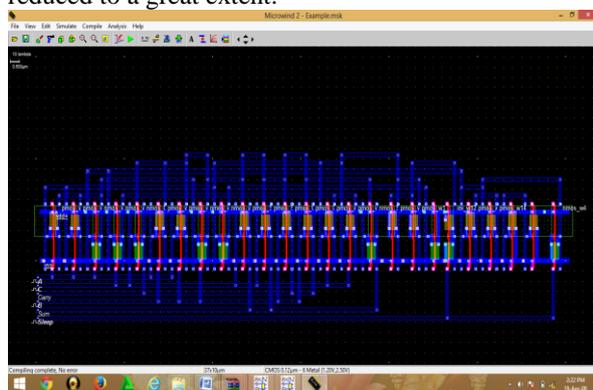


Fig: 5.6 layout of full adder using Dual Stack

The layout of the full adder using dual stack is obtained by using microwind tool.

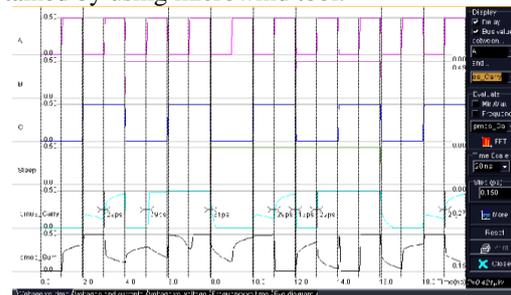


Fig: 5.7 Dual Stack circuit output waveform

In the dual stack the inputs are a, b, c and sleep signal. A and B are sum inputs, where C is carry input and Sleep is the signal to the sleep transistors in the pull up and pull down networks. Depending upon the sleep signal the transistors connected to the sleep transistor will conduct. This avoids the extra usage of power during off mode. The output of the full adder is obtained at PMOS sum and carry.

VII. power comparison

Circuits	Area(μm^2)	Power Dissipation
Full adder	23*12	4.087 μW
Full adder with stack	26*14	3.26 μW
Diode based stacking	31*10	1.254 μW
Dual Sleep Full adder	59*6	0.263 μW
Dual Stack Full adder	68*6	0.002 μW

From this comparison it is clear that the power dissipation for dual stack is very less, when compared to other power gating methods. The power dissipation is compared by using the graph

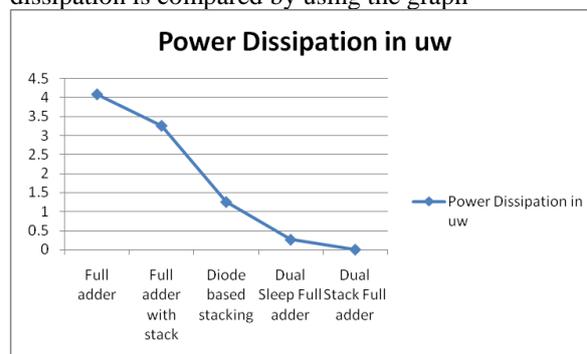


Fig: 5.7 Power comparison graph

From the graph it is clear that the dual stack approach has less power dissipation when compared with other approaches. The leakage power is reduced maximum to 83.5%.

VIII. Conclusion

In nanometer scale CMOS technology, although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, a novel circuit structure named "Dual stack" as a new remedy for designer in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-80% of power than the existing normal or conventional full adders. So, it can be used for future integrated circuits for power & area efficiency.

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