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# Phase locked loop control of 50-150 KHz Half Bridge Resonant type Inverter for Induction Heating Applications

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***Abstract***
A half-bridge resonant-type IGBT inverter suitablefor heating magnetic and nonmagnetic materials at highfrequencyis described. A series-parallel arrangement of capacitorsis adopted and an optimum mode of operation is proposed.In this mode, the inverter is operated at unity power factorby PLL control irrespective of load variations, with maximumcurrent gain, maximum overall system efficiency, and practicallyno voltage spikes in the devices at turn-off.The actual performance was tested on a 50-150 kHz prototyperated at 6 kW. The low-cost developed hybrid inverter is characterizedby its simplicity of design and operation, yet is versatilein performance. A simplified analysis and detailed experimentalresults are presented.

## I. INTRODUCTION

In recent years, there has been a great increase in the use of high-frequency currents for heat treatment ofmetals in such processes as surface hardening, brazing, andsoldering. Much attention has therefore been focused uponthe development of inverters capable of supplying high-powerto induction heating loads at frequencies ranging from 10to 200 kHz. **A** variety of different operating principles andinverter circuit configurations exist, each of which have theirown particular merits. Considerable interest has recently beenshown in resonant inverter circuits as these configurationsoffer reduced power device switching losses and attractivepossibilities in developing higher frequency of operation,higher efficiency, lightweight, and overall system simplicityin terms of inverter control, protection, and maintainability.Most increases in operating frequency have been the resultof improved semiconductor device technology and eliminationof switching losses by means of soft-switching techniques. Various devices, such as power MOSFET's, SI thyristors,and static induction transistors **(SIT'S),** applicable to highfrequencyandor high-power induction heating systems. Recent advances andbreakthroughs in the insulated gate bipolar transistor (IGBT) technology have made the device a viable power semiconductorswitch. The IGBT offers low on resistance andrequires very little gate drive power. Its characteristicof low conduction resistance fits well in a resonant inverterapplication in which a large resonant-current pulse flowsthrough the transistor, and the problems associated with turnoffcurrent tailing and turn-off latching in conventional PWMinverters can be avoided in quasi-resonant inverters 1.This paper describes a 50-150 kHz half-bridge resonanttypeIGBT inverter for induction heating applications. Theactual performance of the system was tested on a prototypewhose power rating **(6** kW) is within the range of the actualrequirements of industrial applications and allows significant scaling for larger implementations.

## II. INDUCTION HEATINGP RINCIPLE

Many practical work-pieces are cylindrical in form and areheated by being placed inside multi- or single-turn coils. Themagnetic field, induced in the coil when energized, causes eddycurrents to occur in the work-piece and these give rise to theheating effect. Theoretical analysis and practical experiencealike show that most of the heat, generated by eddy currentsin the work-piece, is concentrated in a peripheral layer of thickness $\delta$given by

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \quad (1)$$

Where $\mu$ and $\delta$ are the magnetic permeability and electricalresistivity of the work-piece, respectively; $f$ is the appliedfrequency.

The basic concepts are similar to the well known transformertheory, but modified to a single-turn short-circuitedsecondary winding.

The induction heating load (heating coil and work-piece) can be modeled by means of a series combination of itsequivalent resistance $R_L$and inductance $L_L$. Theseparametersdepend on several variables including the shape of theheating coil, the spacing between the work-piece and coil, theirelectrical conductivities and magnetic permeabilities, and thefrequency

## III. CIRCUIT DESCRIPTION AND OPERATION

Acircuit diagram of the basic system, as shown in Fig. 1, comprises essentially a three-phase full-bridge diode rectifier,a single-phase half-bridge IGBT inverter, an induction heatingload and a phase-locked loop (PLL) control circuit.The voltage, at the dc output terminals, can be adjustedby means of a slidacs; the input to which is the 50Hz 3-phase 200v supply

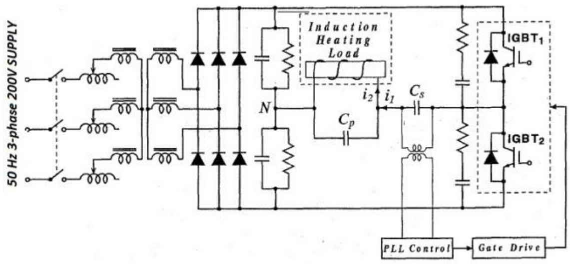



Fig. 1.Proposed inverter system configuration.

Two equal capacitors and resistors areconnected, as shown in the diagram, across the rectifier outputterminals for the junction *N* to be at midpotential withhalf the rectifier output voltage across each capacitor andresistor.

From the power semiconductor devices available, the insulatedgate bipolar transistor (IGBT) was selected for theconstruction of the inverter. IGBT's seem superior to othersemiconductor devices applicable to high-frequency and highpowersystems from the view point of power conversionefficiency and reliability. Two IGBT'swith internal antiparallel diodes are mounted in the samemodule. Electrical connections are made to screw terminalson the top of the module. The switches are actually madeup of eight devices in parallel to satisfy power requirementsand to increase the switching speed since the transistors aretypically two or three times faster when operated below 60%of their rated currents, Because of their relativelyshort switching turn-on and turn-off times, the IGBT's workedreasonably well in the frequency range of interest whenoperated below *2/3* of their rated current.Snubbercomponents are connected in parallel with theIGBT's to avoid any excessive voltage spike duringdeviceturn-off.The induction heating load constitutes a 0.42% carbon steelbillet placed inside a 7-turn water-cooled copper coil at aspecific air gap.The work-piece or billet, along with the heating coil, presents a highly inductive load to the power source. Inorder to minimize the reactive loading, series and parallelcompensating capacitors (Cs and *Cp)* are used in the outputcircuit. The series-parallel arrangement of capacitors has thedesirable characteristics of the series and parallel ones. Theload short circuit and the no-load regulation are possible.In operation, each IGBT conducts for the period correspondingto half the total cycle time. The phase angle betweenthe output current and voltage of the inverter depends onits operating frequency which is the switching rate of theIGBT's. The frequency is controlled in a phase-locked loop (PLL) circuit in sympathy with changing load characteristics.

### A. Phase-Locked Loop (PLL) Control Circuit

The effective parameters for the equivalent resistance andinductance of the induction heating load vary throughout the heating cycle. It thus becomes necessary to changethe operating frequency of the inverter in order to maintainits power factor near unity.The phase-locked loop (PLL) control circuit, as seen fromFig.2, plays a major role in the inverter operation. Theformer has the task of keeping a zero cross-current switchingmode, irrespective of load variations. This implies thatthe IGBT's switching frequency must vary during operation,depending on the resonant frequency of the invertercircuit. The desired performance is achieved by means ofa phase shifter, two comparators, an integrator and a lowpass filter, built around a CMOS PLL chip MC14046B soas to constitute a resonant frequency tracking control circuit.In order to detect the phase of the inverter output current, aninsulation high-frequency potential transformer type EX4462is used. The voltage signal, picked at the terminals of the seriescompensating capacitor $C_s$, is fed to the PLL circuit via thepotential transformer the output of which is then converted toa $90^o$ leading square wave signal $Sl_{IN}$.The IC has two phase detectors PD1 and $PD_2$.Based onan Exclusive-OR gate, PD1 (not used for our purpose) maybe used to give an indication of lock. PD2 is a positiveedge controlled logic circuit consisting essentially of four flipflopsand a pair of MOS transistors. When the frequencies of $S1_{IN}$and$S2_{IN}$ signals are unequal, PD2 gives an output signals $S_{OUT}$ indicating frequency difference, and when lockedit indicates a phase difference. The signal $S_{OUT}$ isused toshift the VCO toward lock before capture then holds thefrequencies in lock as in a conventional PLL circuit. Lockedcondition **is** obtained when both $S1_{IN}$ and $S2_{IN}$signalshave equal frequencies with their phase difference equal tozero. The VCO produces an output signal $VCO_{OUT}$ whosefrequency is determined by the voltage of input $VCO_{IN}$ and,the capacitor and resistors connected to pins 6, 7, 11, and12.

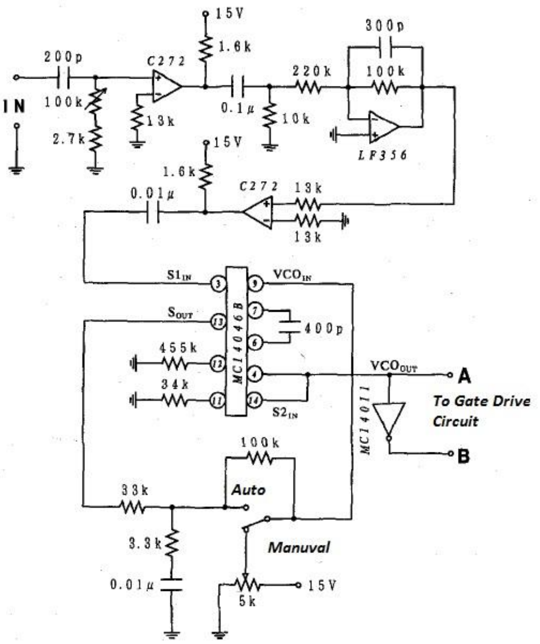



Fig. 2**.**Phase-locked loop (PLL) control circuit.

### B. Gate Drive Circuit

Recently, the insulated gate bipolar transistor is gainingpopularity for its relatively high speed and low gate powerrequirements. Its control terminals are the gate and emitter.The device turns on when a voltage greater than its gateemitterthreshold voltage is applied between the gate andemitter. Fig. 3 shows the IGBT drive circuit developed forthe work.The turn-on and turn-off pulses from the control circuitoutput terminals **(A** and B) are first amplified to appropriatemagnitudes, and then sent through small pulse transformerstype PT4463 to drive the MOSFET's (2SK277). The upperand lower pairs of MOSFET's form push-pull drivers forgating $IGBT_1$ and $IGBT_2$, respectively. The pulse transformerswith ferrite cores isolate the IGBT's from the controlcircuitry. The coupling capacitors (0.22 pF) prevent anyamount of dc current from flowing in the primary windingsand saturating the transformers. Back-to-back connected zenerdiodes (RD4A) limit the MOSFET gate to source voltage toabout 4 **V,** and protect the gates of the MOSFET's againstovervoltages induced by drain voltage spikes on the gates.These usual protections proved to be adequate to ensurereliable and safe operation of the devices. Rapid turn-offtimes for the IGBT's are achieved with the speed-up capacitors (0.1 pF). The 10**Ω** resistors, in series with theMOSFET's, provide supply protection against short circuitsin case the MOSFET's conduct at the same time. Dampingresistors (13**Ω)** are connected to the gates of the IGBT'sto minimize any possible high-frequency oscillations resultingfrom the stray inductances in combination with gate capacitances.

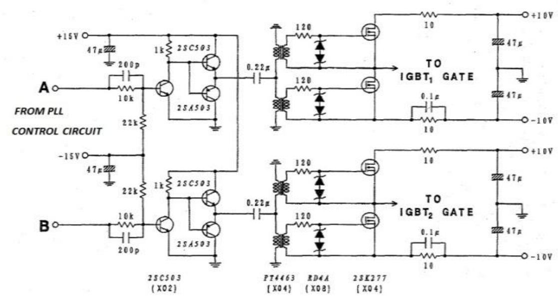



Fig.3. IGBT drive circuit.

## IV. THEORETICAL ANALYSIS

### A. Simplifying Assumptions

The analysis implies the following simplifications and assumptions

a) The input voltage of the inverter is constant.

b) The IGBT's and diodes are ideal.

c) The compensating capacitors are treated as ideal capacitanceswith no losses.

d) All semiconductor devices and line losses are lumpedinto a series resistance $R_s$

e) All stray and leads inductances are lumped into a seriesinductance $L_s$

f) The paralleled IGBT modules are identical and treated asone module where $IGBT_1$ and $IGBT_2$ are the equivalent transistors.

g) The effect of Snubber components is negligible.

Under these assumptions, the circuit of Fig. 1 can be reducedto the simplified form of Fig. 3(a) where the inductionheating load is modeled by a series combination of its equivalentresistance $R_L$ and inductance $L_L$.

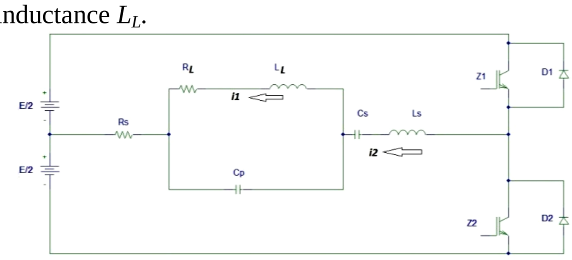



Fig.4. *(a)* simplified circuit of the inverter system

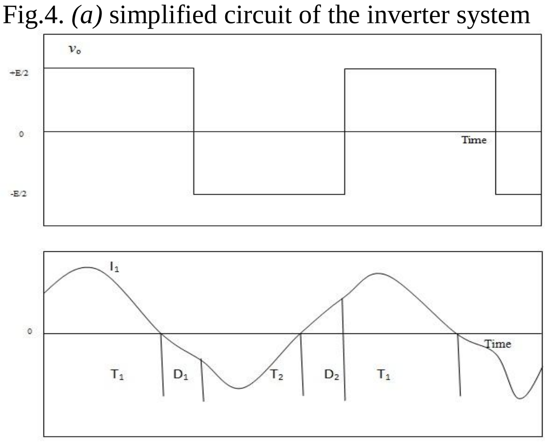



Fig.4. (b) typical steady state waveforms of the inverter output voltage $v_o$ and current $i_1$at a leading power factor

**B. Analysis of the Output Circuit**

In Fig. 5(b), typical on-off timings of the transistors anddiodes at a leading power factor are shown. For a steady statecycle of the inverter operation, there are basically four distinctintervals (overlap time ignored). The harmonic analysis approachcan be employed to develop expressions €or the outputcircuit variables.The instantaneous inverter output voltage can be expressedin Fourier series as

$$v_o(t) = \frac{2E}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}(\sin n\omega t) \tag{2}$$

Wherein$n$ is odd. $E$ is the input voltage of the inverter and$w$ is the angular frequency.The nth harmonic impedances of the series and parallelcircuits can be expressed as

$$Z_{sn} = R_S + j(n\omega L_S - \frac{1}{n\omega C_S})$$

$$Z_{pn} = \frac{R_L + jn\omega\, L_L}{1-n^2\omega^2 L_L C_P - j\omega\, R_L C_P} \tag{3}$$

The output current of the nth harmonic frequency is obtained as

$$I_{1n} = \frac{V_{on}}{Z_{1n}} \tag{4}$$

Where

$$V_{on} = \frac{2E}{n\pi}\text{And}Z_{1n} = Z_{sn} + Z_{pn} \tag{5}$$

The time-domain expression for the output current can berepresented by

$$i_1(t) = \sum_{n=1}^{\infty} \mathrm{I_{1n}} \sin(n\omega t - \emptyset_{1n}) \tag{6}$$

Where

$$I_{1n} = |I_{1n}| \quad \text{And}\emptyset_{1n} = \arg(Z_{1n}) \tag{7}$$

Using the output current harmonics as the basis, other outputcircuit variables can be computed as follows:

The induction heating coil voltage $v_2$ (t) and current $i_2$ (t) can be evaluated as

$$v_2(t) = \sum_{n=1}^{\infty} \mathrm{V_{2n}} \sin(n\omega t + \emptyset_n) \tag{8}$$

Where

$$V_{2n} = I_{1n}|Z_{pn}| and \theta_n = \arg(Z_{pn}) - \emptyset_{1n} \tag{9}$$

For the coil current,

$$i_2(t) = \sum_{n=1}^{\infty} \mathrm{I_{2n}} \sin(n\omega t + \emptyset_{2n}) \tag{10}$$

Where

$$I_{2n} = \frac{V_{2n}}{\sqrt{{R_L}^2 + (n\omega L_L)^2}} and \emptyset_{2n} = \theta_n - \tan^{-1}\left(\frac{n\omega L_L}{R_L}\right) \tag{11}$$

The RMS values of the inverter output, and induction heating coil current and voltage can be calculated as

$$I_1 = \sqrt{\sum_{n=1}^{\infty}\frac{I_{1n}^2}{2}}\ ,\ I_2 = \sqrt{\sum_{n=1}^{\infty}\frac{I_{2n}^2}{2}}\text{And } V_2 = \sqrt{\sum_{n=1}^{\infty}\frac{V_{2n}^2}{2}} \tag{12}$$

The overall system efficiency can be expressed as

$$\eta = \frac{I_2^2 R_L}{I_1^2 R_S + I_2^2 R_L}\eta_C \tag{13}$$

Where $\eta_C (\approx \frac{R_w}{R_L})$the heating coil efficiency and Rw is denotes the work-piece reflected resistance.

Maximum overall system efficiency occurs when the currentgain is maximum

$$\eta_{max} \approx \frac{1}{\frac{1}{\left(\frac{I_2}{I_1}\right)_{max}^2}\frac{R_S}{R_L}+1}\frac{R_\omega}{R_L} \tag{14}$$

**C. Optimum Mode of the inverter operation**

Considering only the fundamental component for simplicity, the magnitude of the current gain can be written in the form

$$\frac{I_2}{I_1} = [(1-\omega^2 L_L C_P)^2 + (\omega C_P R_L)^2]^{-\frac{1}{2}} \tag{15}$$

Maximum current gain is attained at

$$f_m = \frac{1}{2\pi}\sqrt{\frac{1}{L_L C_P} - \frac{R_L^2}{2L_L^2}} \tag{16}$$

And its corresponding value is

$$\left(\frac{I_2}{I_1}\right)_{max} = [\frac{C_P R_L^2}{L_L}(1 - \frac{C_P R_L^2}{4L_L})]^{-\frac{1}{2}} \tag{17}$$

For our practical cases,

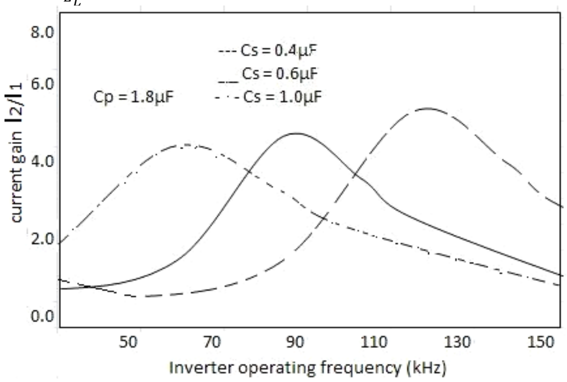
$$\frac{C_p R_L^2}{L_L} << 1 \tag{18}$$

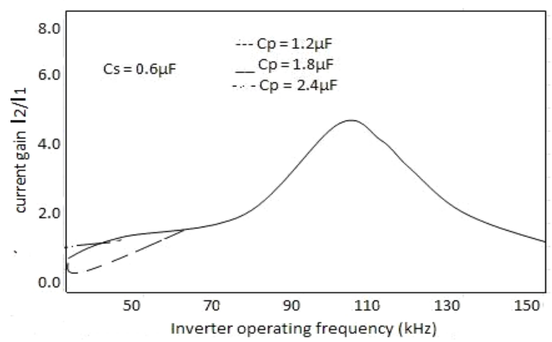
Then, (17) reduces to

$$\left(\frac{I_2}{I_1}\right)_{max} = \frac{1}{R_L}\sqrt{\frac{L_L}{C_p}} \tag{19}$$

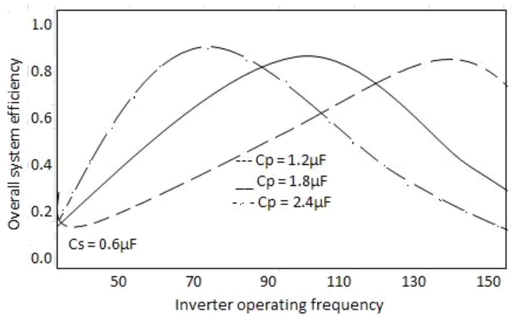
It is a simple matter to show that the inverter runs at unitypower factor with maximum current gain, i.e., operation atpoint $B$ as illustrated from Fig. 6(a), if the series compensatingwherecapacitance $C$, takes approximately the following value

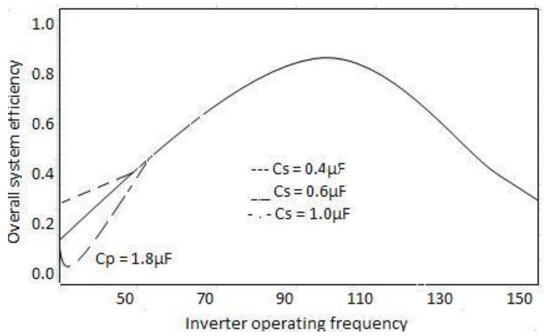
$$C_s \approx \frac{C_p}{\frac{L_S}{L_L} - 0.5} \tag{20}$$




(a)




(b)

Fig.5. (a) Calculated current gain as a function of the inverter operating frequency with *Cs andCp*as parameters (E = 40 V). (b) Overall system efficiency versus the inverter operating frequency with *Cs* and *Cp*as parameters (E = 40 V)

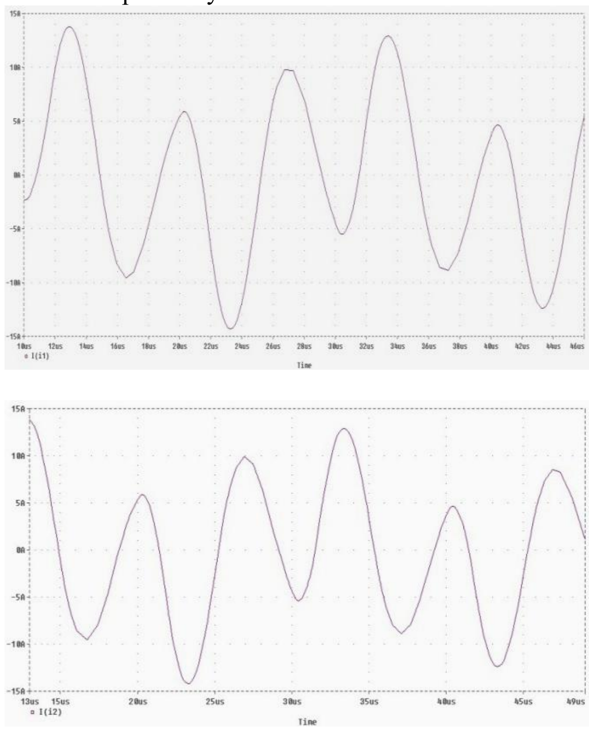
Furthermore, as shown from Fig.4 (a) and (b) the current gain and overall efficiency is maximum at a particular frequency. The phase-locked loop (PLL) control circuit wasdesigned to track only that particular frequency in the 50-150 kHz range. This frequency is the optimal frequency. Itis chosen according to the inductionheating application.

Fig.4 (a) and (b) illustrates the effect of changing the series and parallel compensating capacitors on the current gain and overall system efficiency. As seen from the figures, the current gain and overall system efficiency depend largely on *Cp*and are practically independent of the choice of *Cs.* By altering *Cp*, the peak of the current gain and that of the efficiency can be shifted depending on the desired operating frequency. Improvements in current gain and efficiency can be obtained when relatively low values of *Cs* are selected

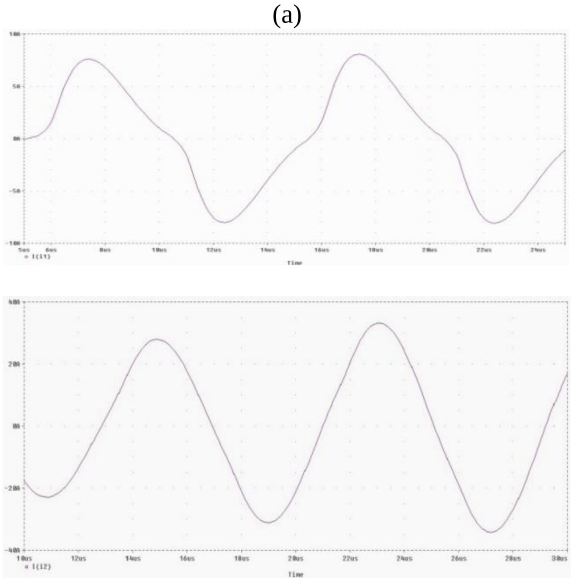
## V. SIMULATION RELSULTS

This simulation results shows the proposed inverter system circuit model. The discrepancies in results are mainly due to the assumption of ignoring the overlap time in the analysis

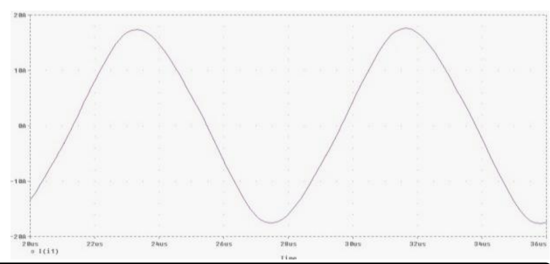
Fig. 5(a)-(c) shows at 50, 100, and 120 kHz the observed waveforms of the inverter output and heating coilcurrents. The series and parallel compensating capacitanceswere adjusted to 0.6 and 1.8 pF, and the inverter inputvoltage was maintained constant at 40 V. $R_S$and $L_S$wereexperimentally found to be 0.25Ω and 3.20$\mu$H, respectively.The induction heating load parameters $R_L$and $L_L$dependon the inverter operating frequency, and their values at 100 kHz are respectively 0.142Ω and 0.93mH.

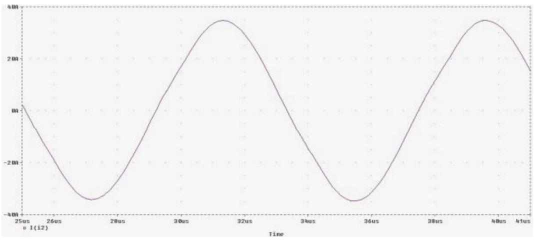


(a)



(b)





(c)

Fig. 6. (a)waveforms of the inverter output current $I_1$and heating coil current $I_2$at 50 kHz(C, = *0.6* pF**,** *C,* = 1.8 pFand *E* = 40V). (b) Simulated waveforms of the inverter output current $I_1$and heating coil current $I_2$at 100 kHz(C, = 0.6 pF**,** *C,* = 1.8 pFand *E* = 40V). (c) Observed and predicted waveforms ofthe inverter output current I1 and heating coil current I2at 120 kHz*(C,* = 0.6 pF**,** *C,* = 1.8 pF and *E* = 40 V).

## VI. CONCLUSION

The high-frequency half-bridge resonant-typeinverter for induction heating applications employing insulatedgate bipolar transistors as the switching devices. The behaviorOf the prototype, rated at kW7 was Observed under loadconditions in the 50-150 kHz range. It was found that bya Proper choice of the compensating capacitors $C_S$and $C_P$**,**the inverter could runat unity power factor with maximumcurrent gain, maximum efficiency and practically no voltagespike in the devices at turn-off. The PLL control circuitwas designed and constructed to track only the frequency at the inverter optimum operating point irrespective of loadvariations.The harmonic analysis approach, though ignoring the effectsof the overlap time and Snubber components for the sakeof simplicity, provided reasonably accurate information withrespect to the inverter output currents, current gain and systemefficiency. The main discrepancies in results were due to theassumption of neglecting the overlap time. The method cantherefore be used with confidence to predict various operatingcharacteristics of the inverter and to select properly its output circuit parameters for different induction heating applications. As stray inductances, related to the circuit layout, inevitablyappeared in the various parts of the inverter system, the effectof such inductances was also taken into consideration in theanalysis.It was found that by a proper choice of the series and parallelcompensating capacitors (C, and *Cp),* any desirable inverter

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