

## Efficient Design of Reversible Multiplexers with Low Quantum Cost

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### Abstract

Multiplexing is the generic term used to designate the operation of sending one or more analogue or digital signals over a common transmission line at dissimilar times or speeds and as such, the scheme we use to do just that is called a Multiplexer. In digital electronics, multiplexers are similarly known as data selectors as they can “select” each input line, are made from individual Analogue Switches encased in a single IC package as conflicting to the “mechanical” type selectors such as standard conservative switches and relays. In today era, reversibility has become essential part of digital world to make digital circuits more efficient. In this paper, we have proposed a new method to reduce quantum cost and power for various multiplexers. The results are simulated in Xilinx by using VHDL language.

**Keywords:** FRG Gate , MFRG Gate , Multiplexer , Power Consumption , Quantum Cost.

### I. Introduction

Reversible logic performs all operations in an invertible manner that marks a promising new direction. As compared with traditional logic, all computations can be reverted (i.e. the inputs can be obtained from the outputs *and vice versa*) by using reversible logic. This reversibility plays significant role for emerging technologies that may replace or at least enhance the traditional computer chip efficiency. Power dissipation and heat generation is a serious problem for today’s computer chips. The non-ideal behavior of transistors and some other materials becomes primary cause for the power dissipation. A more fundamental reason for power dissipation arises from the observations made by Landauer in 1961. Landauer proved that using traditional (irreversible) logic gates always lead to energy dissipation. More precisely, exactly  $kT \log_2$  Joule of energy is dissipated for each “lost” bit of information during the irreversible operation (where  $k$  is the Boltzmann constant and  $T$  is the temperature). [1][9]

Quantum Computation and Quantum Information can be accomplished using Quantum mechanical systems and is the study of the information processing tasks. Quantum mechanics is a mathematical schema or set of rules for the construction of physical theories. Quantum computation directed us to think physically about computation, and this approach turns out many new and exciting capabilities for information processing and communication. [7]

Reversibility in computing signifies that no information about the computational states can ever be lost, so it can be recovered at any earlier stage by computing backwards or uncomputing the results. This is termed as logical reversibility. Reversible computing will also lead to improvement in power efficiency. Power efficiency will fundamentally affect the speed of circuits such as nanocircuits— and therefore the speed of most computing applications. [9]

#### 1.1 Quantum Cost

Quantum Cost of the circuit is considered by knowing the number of simple reversible gates (gates of which rate is previously identified) needed to realize the circuit.

#### 1.2 Garbage Output

The output of the reversible gate that is not used as a main output or as input to other gates is called the garbage output. In little the unexploited output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are required in the circuit to retain the reversibility concept. [9]

#### 1.3 Organization of the work

This section describes the organization of the paper. Section 1 includes the introduction of reversibility. Section 2 shows the work done by the various researchers in the field of reversibility.. Section 3 describes the concept of reversible logic gates . Section 4 includes the proposed work. Section

5 includes the conclusion and Section 6 includes result and discussions. References are shown next..

## II. Literature Survey

F. J. Chih et al [4] described that adders are fundamental building blocks and often constitute part of the critical path. In this paper, they proposed four high-speed ripple carry adder designs using the dynamic circuit techniques. The SPICE simulation shows that the proposed dynamic ripple carry adders are at least two times faster than the conventional static ripple carry adder. **T. Himanshu et al** [7] described that the reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. This work proposed a new  $4 \times 4$  reversible gate called "TSG" gate. The proposed gate was used to design efficient adder units.

From above literature survey, it has been concluded that reversibility is essential for new technologies in terms of power efficiency. This can be done if the quantum cost and garbage output value of the digital circuits should be reduced which can only be possible by using reversible logic gates.

## III. Reversible Logic Gates [7] [10]

### 3.1 Peres Gate (PG)

The  $3 \times 3$  (Peres, 1985) is designated as follows: Input vector  $I_v = (A, B, C)$  and output vector  $O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$ . Block diagram of Peres is showed in Fig. 1. Peres gate is the combination of Feynman gate and Toffoli gate and this can contrivance operations like AND EX-OR. In this projected design PG gate is used for performing AND operation. The quantum cost of Peres gate is 4.

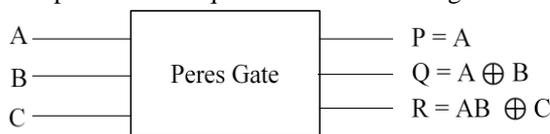


Figure 1: Peres gate

### 3.2 Fredkin Gate (FRG)

Input and output vectors for  $3 \times 3$  FRG (Fredkin and Toffoli, 1982) is well-defined as follows:  $I_v = (A, B, C)$  and  $O_v = (P = A, Q = \bar{A}B + AC, R = \bar{A}C + AB)$  FRG gate is showed in Fig. 2 and it is used in to hypothesis Multiplexers circuits. This gate is used in the planned designs for execution both AND and OR operation. This AND-OR output is attained at output R. The quantum cost of FRG gate is 5.

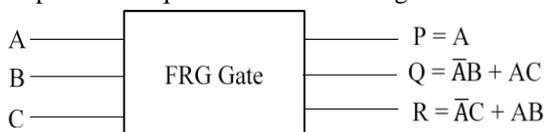


Figure 2: Fredkin gate

### 3.3 Modified Fredkin Gate (MFRG)

Input and output vectors for  $3 \times 3$  FRG (Fredkin and Toffoli, 1982) is well-defined as follows:  $I_v = (A, B, C)$  and  $O_v = (P = A, Q = \bar{A}B \oplus \bar{A}C, R = \bar{A}C \oplus AB)$  MFRG gate is showed in Fig. 3 and it is used in to hypothesis in Multiplexers circuits. This gate is used in the planned designs for execution both AND and OR operation. This AND-OR output is attained at output R. The quantum cost of MFRG gate is 4.

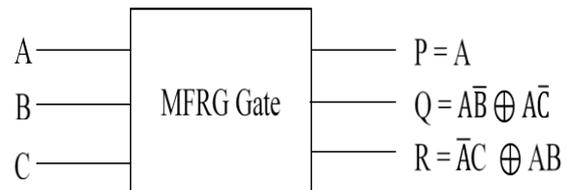


Figure 3: Modified Fredkin gate

### 3.4 MTSG Gate

Modified TSG (MTSG) gate is a  $4 \times 4$  reversible gate with following input and output vectors,  $I_v = (A, B, C, D)$  and  $O_v = (P = A, Q = A \oplus B, R = A \oplus B \oplus C$  and  $S = (A \oplus B).C \oplus (AB \oplus D))$ . This MTSG gate in Fig. 4 can be recycled to recognize a full adder by providing constant '0' at the input D. Quantum cost of changeable MTSG gate is 6 which is lower than 13 of TSG gate. This gate is used in the enterprise so as to produce the sum, carry and the spread output of the inputs.

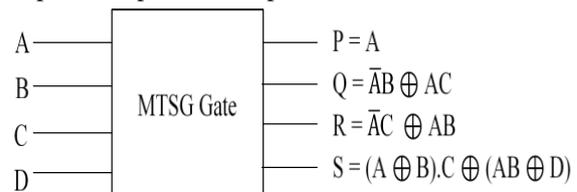


Figure 4: MTSG gate

### 3.5 MHNG Gate

MHNG gate is a  $4 \times 4$  reversible gate with following input and output vectors,  $I_v = (A, B, C, D)$  and  $O_v = (P = A, Q = D, R = A \oplus B \oplus C, S = (A \oplus B).C \oplus AB \oplus D)$ . The MHNG gate is shown in Fig. 5, where each output is annotated with the corresponding logic expression. One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit.

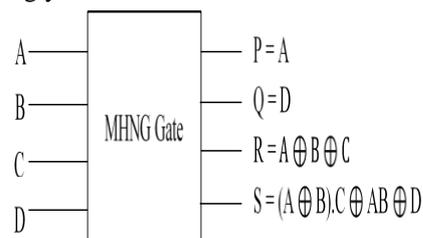


Figure 5: MHNG Gate

#### IV. Proposed Work

##### 4.1 2:1 Multiplexer

Fig. 6 shows the proposed architecture for 2:1 MUX using MFRG gate.

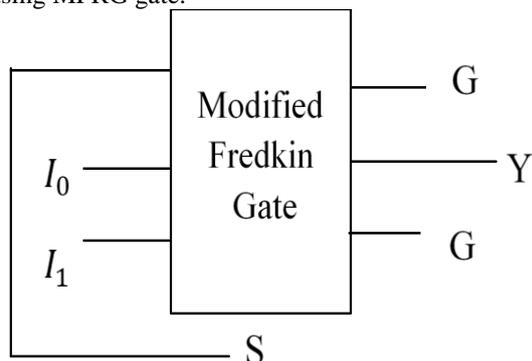


Figure 6: 2:1 MUX using MFRG gate

##### 4.2 4:1 Multiplexer

Fig. 7 shows the proposed architecture for 4:1 MUX using MFRG gates.

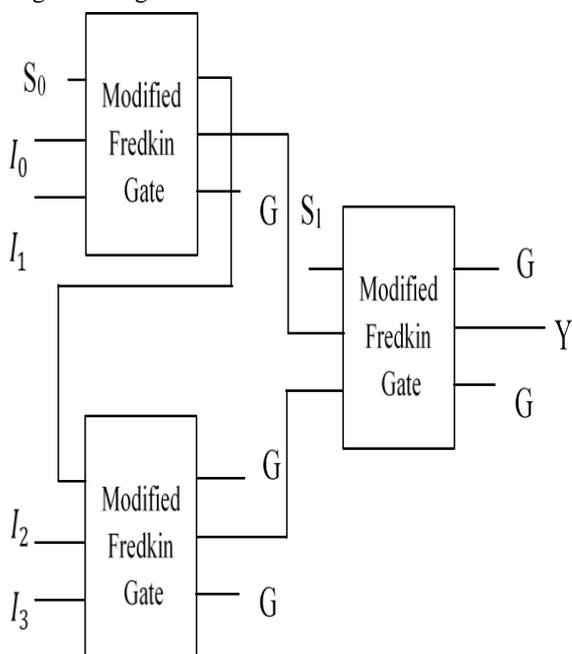


Figure 7: 4:1 MUX using MFRG gates

##### 4.3 8:1 Multiplexer

Fig. 8 shows the proposed architecture for 8:1 MUX using MFRG gate.

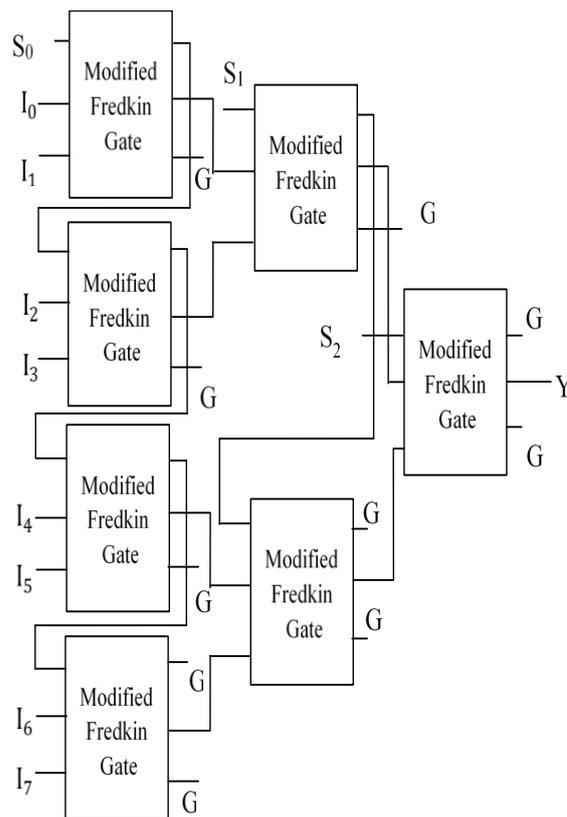


Figure 8: 8:1 MUX using MFRG gates

##### 4.4 16:1 Multiplexer:

Fig. 9 shows the proposed architecture for 16:1 MUX using MFRG gate.

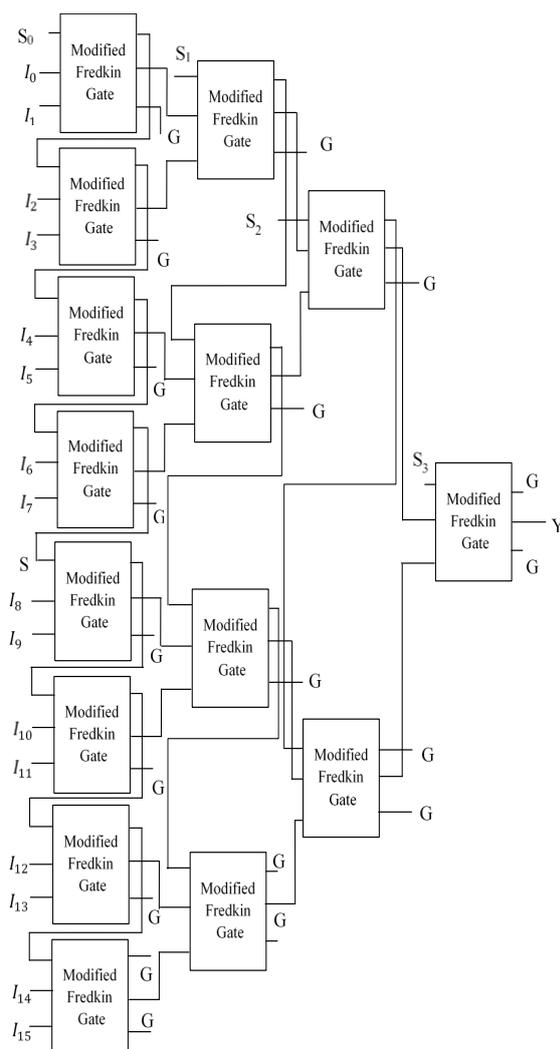


Figure 9: 16:1 MUX using MFRG gates

### V. Results and Discussions

Table 1: Comparison of proposed work with existing work

		Quantum Cost
<b>2:1 MUX</b>	Using FRG Gates	5
	Using MFRG Gates	4
<b>4:1 MUX</b>	Using FRG Gates	15
	Using MFRG Gates	12
<b>8:1 MUX</b>	Using FRG Gates	35
	Using MFRG Gates	28
<b>16:1 MUX</b>	Using FRG Gates	75
	Using MFRG Gates	60

The proposed reversible multiplexers are more efficient than the existing circuits presented in [10]. Evaluation of proposed circuit can be comprehended easily with the help of the comparative results in Table 1. Therefore, the proposed multiplexers are better than the existing circuits in terms of complexity. One of the other major constrains in

designing a reversible logic circuit is less quantum cost.

### VI. Conclusion

In this paper, we presented reversible multiplexers using MFRG gates. Table 1 demonstrates that the proposed reversible multiplexers are better than the existing designs in terms of hardware complexity and quantum cost. Our proposed reversible multiplexers can be applied to the design of complex systems in nanotechnology.

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