

Reduction of Static Power with Minimized Ground Bounce Noise Using Sleep Signal Slew Rate Modulation In 45nm Technology

M. Naga Pramod Reddy*, P. Madhu Kumar**

* Department of Electronics and Communications, Sree Vidyanikethan Engineering College, Tirupati,

** Department of Electronics and Communications, Sree Vidyanikethan Engineering College, Tirupati,

Abstract

In MTCMOS Integrated Circuit design there exists a significant trade-off between static power consumption and technology scaling. In Modern circuits increase in power dissipation is significant due to combination of higher clock speeds, greater functional integration and smaller process geometries resulting in dominant static power consumption component. This is a big challenge for the circuit designer. However, the designers do have few methods like sleep transistor approach, sleepy stack approach to reduce this static power consumption. However all of these methods do have their own drawbacks. In order to achieve lower static power consumptions one has to sacrifice area and circuit performance metrics. In this paper we propose a new enhancement to available static power reduction techniques by modulating the sleep signal slew rate. We have designed the basic CMOS circuits in MTCMOS to achieve significant reduction in Static power consumption. For Sleep signal slew rate modulation we have proposed a modulator called triple phase sleep signal slew rate modulator. By using this Triple Phase Sleep signal modulator(TPS) we can control the noise at ground distribution network (ground bounce noise) produced during sleep to active state transition. By using TPS we can decrease the reactivation time to a recognizable extent, along with reduced power (static and dynamic) dissipation.

Keywords: Power and Ground bouncing noise, reactivation time, sleep signal rise delay, static power reduction.

I. Introduction

CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this race in technology trends transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is in off state. Low threshold voltage also results in increasing sub-threshold leakage current as transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation has become a significant portion of total power consumption for current and future silicon technologies. Various techniques to reduce leakage power can be reviewed from reference no[1]. In present days these techniques are implemented using MTCMOS technology in which the entire circuit is divided into multiple

autonomous power/ground gating domains for effective reduction leakage power consumption[3],[4]. When an idle circuit is awoken, high currents flow through the sleep transistors. Significant voltage fluctuations occur on the power and ground distribution networks (power and ground bouncing noise). Reactivation noise has become an important reliability concern in modern Integrated

Circuits[5],[6]. We propose a new approach, thus providing a choice to VLSI designers by modulating the slew rate of sleep signal resulting in low-leakage power dissipations. By applying this sleep signal at the gates of power and ground gating transistors in general the sleep transistors the required reduction in power dissipation can be achieved at a cost of lowest ground bounce noise.

This paper is organized as follows: Static power reduction techniques are discussed in section 2. The necessity of sleep signal slew rate modulation followed by the previous sleep signal modulation techniques is presented in section 3. The new triple phase sleep signal slew rate modulator is presented in section 4. The performance parameters of previous techniques are summarized and compared with our proposed enhancement for static power reduction in section 5 followed by conclusion in section 6.

II. Static Power Reduction Techniques

1.1. Sleep Transistor Approach

The most well-known traditional approach is the sleep approach(Fig. 1)[1]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. By cutting off the power source, this technique can reduce leakage power effectively.

However, the technique results in destruction of state plus a floating output voltage in sleep mode. This method uses the aspect ratio of $W/L=3$ for NMOS and $W/L=6$ for PMOS in inverter delay chain and the additional sleep transistors.

1.2. Sleepy Stack Approach

In the sleepy stack structure the forced stack and the sleep transistor techniques are combined together. Hence the names sleepy stack[1]. Fig.10 shows a sleepy stack inverter. The sleepy stack inverter in Fig.2 uses the aspect ratio $W/L = 3$ for the pull up transistors and $W/L = 1.5$ for the pull down transistors. At the same time the conventional inverter with the same input capacitance uses the aspect ratio $W/L = 3$ for the pull up transistors and $W/L = 1.5$ for the pull down transistors. The sleep transistor and the stacked transistor in each network are made parallel. Here the width of the sleep transistors is reduced. Changing the width of the sleep transistors may provide additional tradeoffs between delay, power and area. The activity of the sleep transistors in sleepy stack is same as the activity of the sleep transistors in the sleep transistor technique. The sleep transistors are turned on during active mode and turned off during sleep mode. The sleepy stack structure can reduce the circuit delay in two ways. First, since the sleep transistors are always on during active mode so there is always a current flow through the circuit. That's why it gives a faster switching time than the forced stack structure. The high V_{th} transistors are used for the sleep transistor and the transistors parallel to the sleep transistor without incurring large delay increase. The delay time is increasing here but it gives low leakage. During sleep mode both the sleep transistors are turned off. But the sleepy stack structure maintains exact logic state. As high V_{th} transistor is used here so the leakage power is suppressed. The stacked transistors also suppressed the leakage power consumption. So sleepy stack structure achieves ultra low leakage power consumption during sleep mode while retaining the exact logic state. But the main drawback of this sleepy stack technique, however, is increasing area a lot.

1.3. Stacked Sleep Approach

This is another new leakage reduction technique. In this technique the sleep transistors are getting stacked. That's why we call it "Stacked sleep" approach. The stacked sleep approach for a chain of 4 inverters is shown in Fig. 3. This technique uses two stacked sleep transistor in Vdd and two stacked sleep transistor in ground. So, leakage reduction in this technique occurs in two ways. First, the stack effect of sleep transistors and second, the sleep transistor effect. It is well known that pmos transistors are not efficient at passing GND; similarly, it is well known that nmos transistors are not efficient at passing Vdd.

But this stacked sleep technique uses pmos transistor in GND and nmos transistor in Vdd for maintaining the exact logic state during sleep mode. This stacked sleep transistor uses aspect ratio $W/L=3$ for nmos transistor and $W/L=6$ for pmos transistor in the main inverter portion. For the stacked sleep transistor this technique uses aspect ratio $W/L=1$ for both the nmos and pmos transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use aspect ratio $W/L=1$.

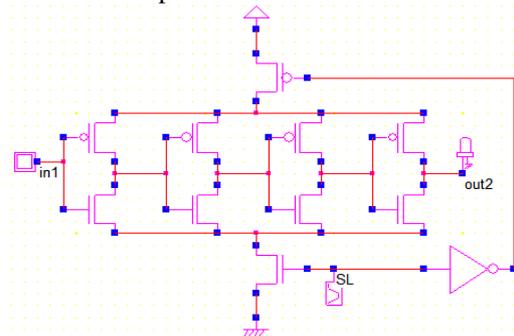


Fig -1: Sleep Transistor Approach

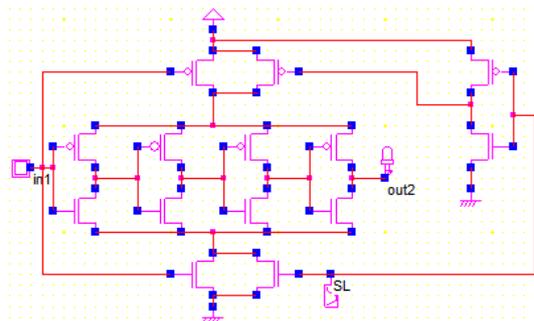


Fig -2: Sleepy Stack Approach

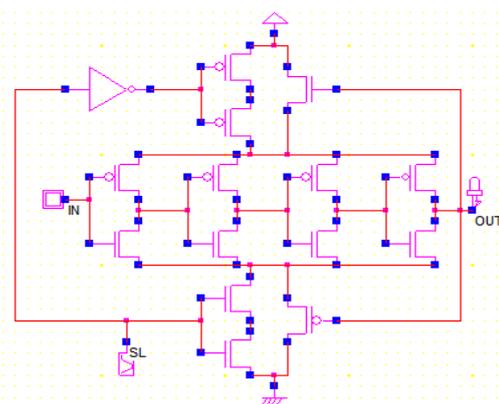


Fig -3: Stacked Sleep Approach

Now the proposed enhancement to all above three techniques is the modulated sleep signal, which is generated from single phase sleep signal slew rate modulator and triple phase sleep signal slew rate modulator that are discussed in section 3 and section 4. The stepwise V_{gs} MTCMOS circuit Sleep signal

modulator is just presented in this paper, and the simulation of 8-bit Brent-kung adder using this modulator is presented in this paper.

III. Previous Approaches of Sleep Signal Modulation

1.4. Necessity of Sleep Signal Modulation

Before going to explain about previous sleep signal slew rate modulation techniques let we know what is the necessity of these techniques. With the sleep signal having very small rise delay will introduce larger ground bounce noise in the power/ground distribution network. This noise is produced during the sleep to active state transition of the network. This is why because the awakening circuit block in MTCMOS circuit will produce a larger currents in very short span of time, which will pass from the sleep transistor. Because of this currents some noise will be generated at ground distribution network. This noise will propagate through the already active circuit block and shifts the output from correct levels or it may completely destroy the active circuit block. To avoid this phenomenon the design engineers has to eliminate the ground bounce noise or at least it has to be reduced to a harmless level.

As the rise delay of sleep signal increased from 60pSec to 100nSec the ground bounce noise is reduced to 0.466mV from 67.3mV. the decay of reduction in ground bounce noise with respect to sleep signal rise delay is plotted in Fig.4. The rise delay is the time interval for the sleep signal to rise from 10 to 990 mV.

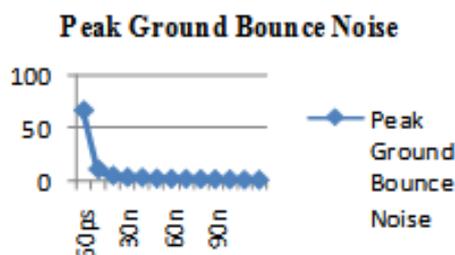


Fig -4: Peak ground bouncing noise produced by the ground-gated 8-bit adder with different sleep signal rise delays. The minimum realizable sleep signal rise delay is 60ps in this PTM 45-nm CMOS technology

1.5. Single Phase Sleep Signal Modulator

Sleep signal slew rate modulation techniques are evaluated with a ground gated 8-bit Brent-Kung adder as illustrated in Fig. 5. The sleep transistor is sized $2.5\mu\text{m}$ to achieve similar (within 4%) delay along the critical signal propagation path (in ACTIVE mode) of MTCMOS circuit as compared to the standard single low- $|V_{th}|$ circuit. Single-phase sleep signal slew rate modulation technique is presented in this section. Circuits are designed with the PTM 45-

nm multi-threshold voltage (multi- V_{th}) CMOS technology (high- $V_{th_nMOS} = +466\text{ mV}$, low- $V_{th_nMOS} = +220\text{ mV}$, high- $V_{th_pMOS} = -411\text{ mV}$, low- $V_{th_pMOS} = -220\text{ mV}$, and $V_{DD}=1\text{V}$) [10]. The ground bouncing noise phenomenon is evaluated with the parasitic impedance model of 40-pin dual in-line package[4].

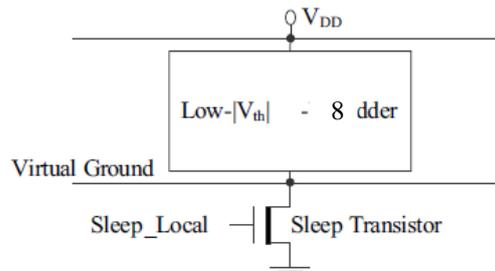


Fig -5: Ground-gated 8-bit Brent-Kung adder. High- $|V_{th}|$ sleep transistor is represented with a thick line in the channel area.

The rise delay is the time interval for the sleep signal to rise from 10 to 990 mV. Multiple noise waveforms are generated as the sleep signal gradually rises from 0 V to V_{DD} . When the voltage level of sleep signal is lower than the threshold voltage (V_{th_sleep}) of sleep transistor, the sleep transistor operates in weak inversion region. The virtual ground line (VGND) is discharged very slowly by the small leakage current produced by the high- $|V_{th}|$ sleep transistor as shown in Fig. 6. The noise induced on the ground distribution network is negligible for $V_{gs} < V_{th_sleep}$. After the sleep signal rises above the threshold voltage of sleep transistor, the VGND is discharged faster. Noise on the real ground is thereby increased. In SLEEP mode, VGND and all the internal nodes of low- $|V_{th}|$ circuit block are maintained at voltage levels close to V_{DD} . During a reactivation event, the internal nodes of the low- $|V_{th}|$ circuit block transition to the correct logic states stage by stage depending on the input. Some internal nodes follow the discharging VGND and transition toward 0V. Significant amount of switching and short-circuit currents are produced by the awakening low- $|V_{th}|$ logic block. Due to the high rate of change of the current produced by the sleep transistor (high di/dt), the ground bouncing noise is maximized. The switching and short-circuit currents through the low- $|V_{th}|$ circuit block gradually disappear as the VGND voltage subsides and the internal node voltages stabilize. The noise on real ground is therefore gradually dampened.

When the rise delay of sleep signal is relatively short (for example, 60ps), all the switching and short-circuit currents are produced during a relatively narrow time frame. Alternatively, when the rise delay of sleep signal is increased, the switching and short-

circuit currents are distributed to a longer time frame. The rate of change of instantaneous currents is thereby reduced and the ground bouncing noise is mitigated. As shown in Fig. 4, the peak ground bouncing noise produced by the ground-gated 8-bit adder is significantly reduced as the rise delay of sleep signal is increased from 60 ps to 100 ns. The sleep signal slew rate modulation technique is effective in suppressing the ground bouncing noise produce by an MTCMOS circuit. The Voltage waveforms on the virtual ground wire, real ground line are shown in Fig.6 when the ground-gated MTCMOS circuit transitions from SLEEP state to ACTIVE state.

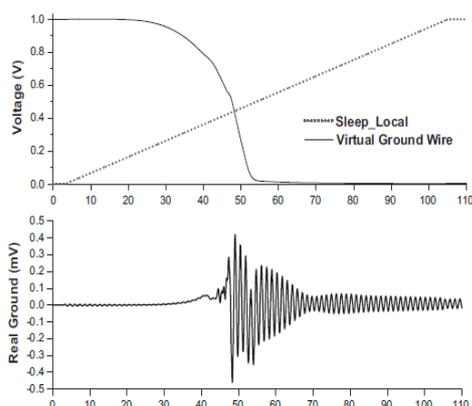


Fig -6: Voltage waveforms on the virtual ground wire, real ground line, when the ground-gated MTCMOS circuit transitions from SLEEP mode to ACTIVE mode

1.6. Stepwise Vgs MTCMOS Technique

Stepwise Vgs MTCMOS technique[11] is presented in this section. The schematic of this modulator is shown in Fig.7. A stepwise Vgs MTCMOS circuit is activated in two steps as follows. The sleep signal transitions from 0V to an intermediate voltage level VX (0 V < VX < VDD) during the first step of a reactivation event. The sleep transistor is weakly activated with a low gate voltage (VX). Although the voltage swing on the VGND is relatively high during the first wake up step, the amplitude of the first noise waveform is suppressed due to the weak conductivity of the sleep transistor. After the VGND is discharged to a sufficiently low voltage level, the sleep signal transitions from VX to VDD. The sleep transistor is strongly turned on. VGND is discharged to ~0 V following the full activation of the sleep transistor (Sleep_Local = VDD). The amplitude of the second noise waveform is also suppressed due to the lower voltage swing on the VGND during the second wake up step. A sleep signal modulator for stepwise Vgs MTCMOS circuit is shown in [11],Fig. 7. During the first wake up step, N2 is turned on. Pdiv and N2 raise Sleep_Local from 0 V to VX. The value of VX is determined by the

voltage divider that is composed of the diode-connected pMOS transistor Pdiv, diode-connected nMOS transistor Ndiv, and N1. During the second wake up step, N2 is cut off, while Pcharge is activated. Sleep_Local is raised from VX to VDD by Pcharge. The timing diagram of modulated sleep signal is shown in Fig. 8.

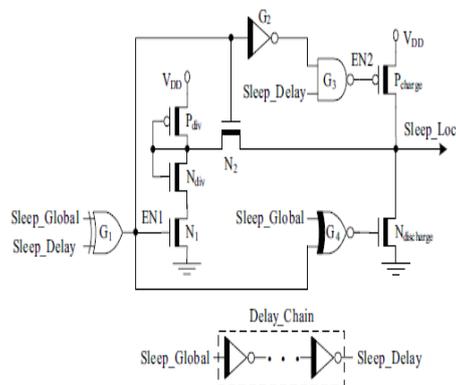


Fig -7: Schematic of the sleep signal modulator for stepwise Vgs MTCMOS circuit

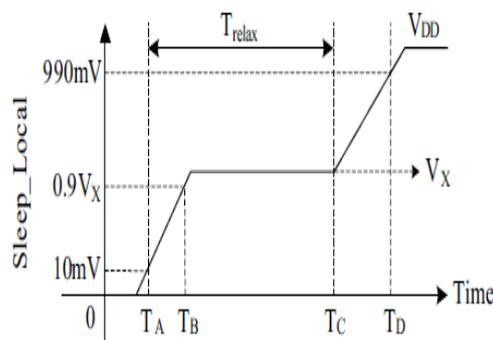


Fig -8: Timing diagram of the local sleep signal with the stepwise Vgs MTCMOS circuit

The methodology needed to choose an appropriate intermediate voltage VX is not provided. The influence of sleep signal slew rate on reactivation noise is not discussed. The optimum VX that minimizes the peak reactivation noise varies with the threshold voltage of sleep transistor. The effectiveness of stepwise Vgs in suppressing reactivation noise is therefore strongly affected by process variations.

IV. Triple Phase Sleep Signal Modulator

As discussed in Section 3.1, a slowly rising sleep signal is effective for suppressing the ground bounce noise in MTCMOS circuits. A slowly rising sleep signal however also significantly increases the reactivation time and energy consumption of MTCMOS circuits.

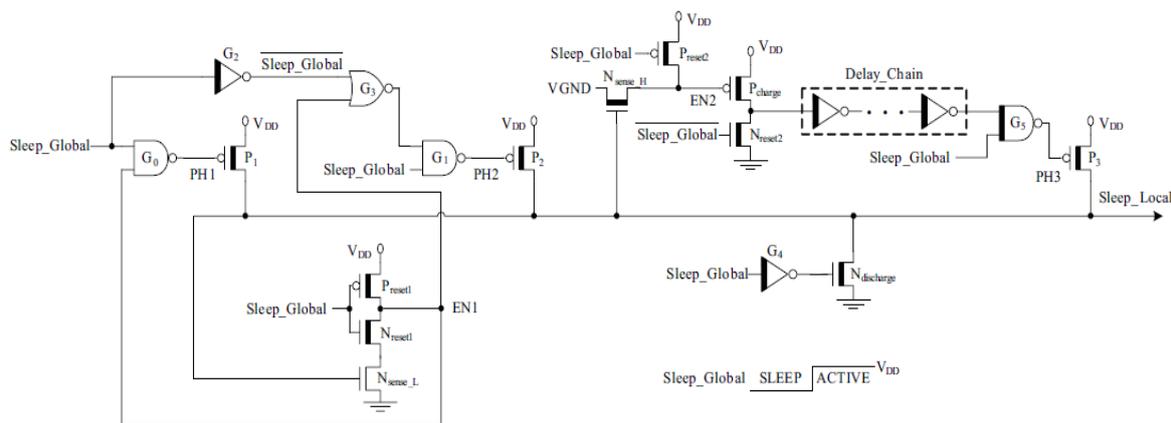


Fig -9: Schematic Of the Triple Phase Sleep Signal Slew Rate Modulator

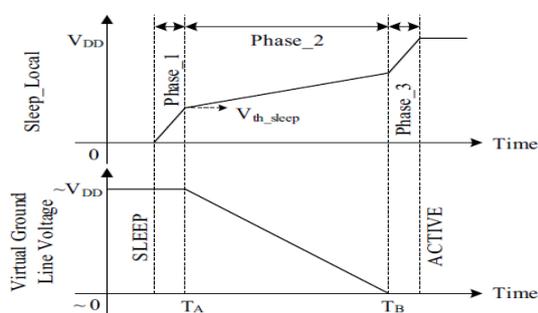


Fig -10: Illustration of TPS technique

The single-phase sleep signal slew rate modulation technique is therefore not suitable for fast and energy efficient power/ground gating in high-performance integrated circuits. An alternative triple-phase sleep signal slew rate modulation (TPS) technique [2],[8] is presented in this section to suppress the reactivation noise while accelerating the reactivation process in MTCMOS circuits. As discussed earlier the sleep transistor produces negligible noise when $V_{gs} < V_{th_sleep}$, so the sleep signal is preferred to rise faster until it reaches the threshold voltage of sleep transistor to decrease the reactivation time without producing significant noise. Reactivation noise is primarily produced after the sleep transistor is turned on. After reaching the threshold voltage of sleep transistor the sleep signal should be decelerated intentionally. This process will suppress the peak mode transition noise that is produced after the sleep transistor is fully activated. After the VGND voltage is reduced to a very low level close to 0 V (time point T_B as shown in Fig. 5), the mode transition noise diminishes to a negligibly low level. The rise of sleep signal should therefore be again accelerated to shorten the remaining duration of reactivation process. Due to the shorter periods of Phase_1 and Phase_3, the reactivation time and energy consumption of MTCMOS circuits are reduced with the TPS technique as compared with the single-phase sleep signal slew rate modulation

technique that is presented in Section 3.2. Before going to discuss about TPS there is an important parameter, that is Reactivation time(T_R) which is given below.

$$T_R = \text{Sleep Signal modulator delay} + \text{Reactivation Delay}$$

The triple phase sleep signal slew rate modulator shown in Fig.9 operates as follows. In sleep mode the sleep_global is maintained at 0V. The P1,P2,P3 transistors are in cut off mode. The P_reset1 is in active state which keeps EN1 at VDD. The N_discharge is in active state, which keeps the sleep_local at ~0V along the sleep mode. In sleep mode the PH1,PH2,PH3 are maintained at ~VDD. When reactivation starts the sleep_global starts to rise, and PH1 starts to decrease P1 starts to conducting, and sleep_local starts rising. When sleep_local reaches 0.22V(threshold voltage of N_{sense_L})[10],the EN1 starts to decrease to 0V,from this instant the PH1 starts rising, and P1 went into cut off state. When EN1 falling to 0V,the output of NOR gate starts to rise which in turn decrease the PH2,So P2 will get turned on. The P2 is designed(sized) weaker when compared to P1.in Phase-2 when sleep_local rises to threshold voltage of N_{sense_H} , it'll turn on and EN2 is discharged into VGND. Then P_charge turned on After the delay of Delay_Chain and NAND gate(G5) the P3 transistor will turn on.P2 is also in active state to assist the P3 in Phase-3.

During a deactivation event, Sleep_Global transitions from VDD to "0." PH1, PH2, and PH3 transition to high after the delay of G0, G1, and G5, respectively. P1, P2, and P3 are cut off. Alternatively, N_discharge is turned on after the delay of G4. Sleep_Local is discharged to ~0 V by $N_{discharge}$, thereby deactivating the MTCMOS circuit. Since P1, P2, and P3 are disabled before $N_{discharge}$ is turned on, no short-circuit current is produced by P1, P2, and P3 in this new digital sleep signal modulator.

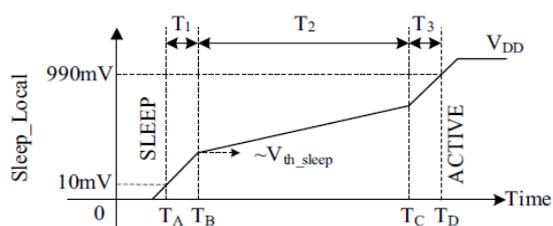


Fig -11: Timing Diagram of the local sleep signal with the TPS MTCMOS circuit.

With the triple-phase sleep signal slew rate modulator that is shown in Fig.9, the rising speed of sleep signal is adjusted by monitoring the voltage level of Sleep_Local and VGND. The transitions between the three phases of reactivation occur automatically. No additional control signals or voltage bias sources are required.

V. Simulation Results

The simulation results of 8-bit Brent-Kung adder using sleep signal generated from single phase sleep signal slew rate modulator, Stepwise Vgs MTCMOS technique and Triple phase sleep signal slew rate modulator technique is tabulated below.

Circuit Technique	Single Phase	Triple Phase	Stepwise Vgs
Peak Ground Bounce Noise (mV)	1.9mV	1.75mV	2.4mV
Reactivation Time (nS)	48.66 nS	11.08nS	15.92nS
Sleep Leakage Power (uW)	1.6uW	1.89uW	1.89uW

Table -1: Comparison of Sleep Signal Slew rate modulation techniques

The sleep signal modulated from above mentioned modulators is shown below.

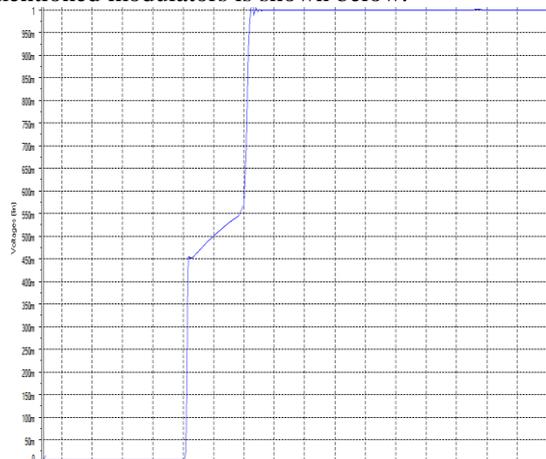


Fig -12: Triple Phase sleep signal

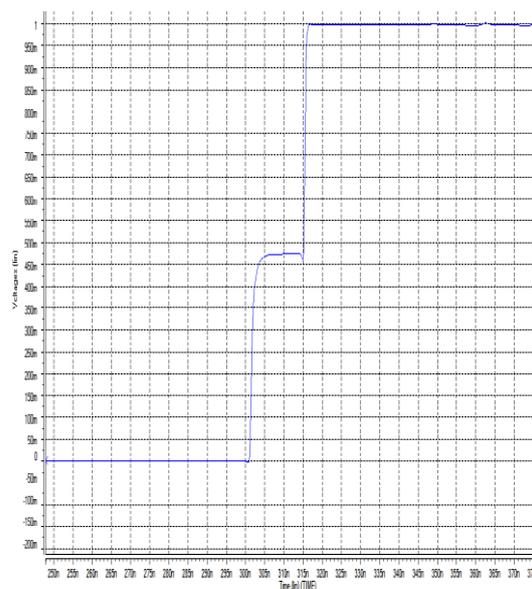


Fig -13: Sleep signal modulated by Stepwise Vgs MTCMOS technique

The comparison of static power reduction techniques with the added enhancement that is after applying the sleep signal modulated from the above mentioned three modulators with the static power reduction techniques with normal sleep signal i.e. which has 60pSec rise delay is tabulated below.

method	propagation Delay	Static Power	Dynamic Power	Bounce	Reactivation Time
base Case	2.574 nS	1.1072 uW	24.521 uW	3.9594 mV	not exist
Sleep Approach(general sleep)	0.82 nS	190.29 nW	95.68 uW	10.288 mV	not exist
Sleepy Stack(normal sleep)	0.451 nS	141.81 nW	197.56 uW	10.89 mV	not exist
Stacked Sleep(normal sleep)	1.862 nS	58.96 nW	182.7 uW	6.06 mV	not exist
base case(SPS)	0.79462 nS	51.131 nW	7.2029 uW	2.1 mV	54.348 nS
Sleep Approach(SPS)	0.8 nS	180.2 nW	15.36 uW	1.8 mV	55.23 nS
Sleepy Stack(SPS)	0.54 nS	104.45 nW	7.29 uW	1.41 mV	54.8469 nS
Stacked Sleep(SPS)	1.896 nS	61.6 nW	4.86 uW	0.32 mV	56.08 nS
base case(TPS)	0.0896 nS	1.0337 uW	16.095 uW	2.4 mV	9.01547 nS
Sleep Approach(TPS)	0.39345 nS	603.35 nW	15.73 uW	2.14 mV	12.73 nS
Sleepy Stack(TPS)	0.44 nS	226.99 nW	15.265 uW	1.61 mV	14.71 nS
Stacked Sleep(TPS)	1.899 nS	219.1 nW	13.36 uW	1.55 mV	15.5 nS

Table -2: Simulation results of static power reduction technique with add enhancement in 45nm technology

VI. CONCLUSION

Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient enhancement to the existing static power reduction techniques for reducing leakage power in VLSI design at very low ground bounce noise. Sleep signal slew rate modulation techniques are explored in this paper for reducing mode transition noise (ground bounce noise) in MTCMOS circuits. A triple-phase sleep signal slew rate modulation technique with a novel digital sleep signal generator is proposed. The triple phase sleep signal slew rate modulation technique reduces the overall reactivation time by 0.32 and 0.69 as compared to the single-phase and stepwise Vgs sleep signal slew rate modulation techniques, the sleep leakage power is increased by 1.18 and 1 as compared to the single-phase and stepwise Vgs sleep

signal slew rate modulation techniques respectively. By applying the sleep signal modulated from single phase sleep signal modulator the static power, dynamic power, propagation delay and bounce of static power reduction techniques has reduced when compared with the same techniques with normal sleep signal. By applying the sleep signal modulated from triple phase sleep signal modulator the static power, dynamic power has increased a little bit but propagation delay and bounce of static power reduction techniques has reduced when compared with the same techniques with normal sleep signal, and the circuit reactivation time has reduced by X3 when compared with single phase sleep signal modulation technique.

REFERENCES

- [1]. Md. Asif Jahangir Chowdhury, Md. Shahriar Rizwan, and M. S. Islam, "An Efficient VLSI Design Approach To Reduce Static power using Variable Body Biasing," in World Academy Of Science, Engineering and Technology 64 2012.
- [2]. H. Jiao and V. Kursun, "Reactivation Noise Suppression With Sleep Signal Slew Rate Modulation in MTCMOS Circuits," *IEEE Trans. VLSI Systems, Reg. Papers*, vol. 21, no. 3, pp. 533–545, Mar. 2013.
- [3]. B. H. Calhoun, F. A. Honoré, and A. P. Chandrakasan, "A leakage reduction methodology for distributed MTCMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 818–826, May 2004.
- [4]. H. Jiao and V. Kursun, "Ground-bouncing-noise-aware combinational MTCMOS circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 2053–2065, Aug. 2010.
- [5]. H. Jiao and V. Kursun, "Tri-mode operation for noise reduction and data preservation in low-leakage multi-threshold CMOS circuits," in *VLSI SoC: Forward-Looking Trends in IC and System Design*, J. L. Ayala, D. A. Atienza, and R. Reis, Eds. New York: Springer-Verlag, 2012, pp. 258–290.
- [6]. P. Heydari and M. Pedram, "Ground bounce in digital VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 2, pp. 180–185, Apr. 2003.
- [7]. "Understanding and Minimizing Ground Bounce" ,Fairchild Semiconductor Application Note June 1989 Revised February 2003.
- [8]. H. Jiao and V. Kursun, "Sleep signal slew rate modulation for mode transition noise suppression in ground gated integrated circuits," in *Proc.IEEE Int. SoC Conf., Sep. 2011*, pp. 365–370.
- [9]. M. Anis, S. Areibi, and M. Elmasry, "Design and optimization of multithreshold CMOS (MTCMOS) circuits," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 22, no. 10, pp. 1324–1242, Oct. 2003.
- [10]. PTM 45nm CMOS Technology[Online] Available: <http://ptm.asu.edu/latest.html>.
- [11]. S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, D. Heidel, and M. Immediato, "Minimizing inductive noise in system-on-a-chip with multiple power gating structures," in *Proc. IEEE Eur. Solid-State Circuit. Conf.*, Sep. 2003, pp. 635–638.