

## QPSK Modulator and Demodulator Using FPGA for SDR

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### ABSTRACT

A software-defined radio (SDR) allows for digital communication systems to simply accept more complicated coding and modulation technologies, which is enormously vital in meeting the ever-increasing demands of the wireless communication industry. An SDR has been constructed, using the Simulink tool, and implemented on the SPARTEN-3E Field Programmable Gate Array (FPGA) development kit. The modulation scheme used in the system is Quadrature Phase-Shift Keying (QPSK). In the first step to realize the whole modulation and demodulation schemes using MATLAB Simulink. The format of a VHDL program is built around the concept of BLOCKS which are the basic building units of a VHDL design. The results showed that the proposed method can greatly improve the developing efficiency, shorten developing period and reduce costs.

**Keywords** - Demodulator, FPGA, Modulator, QPSK, SDR VHDL

### I. INTRODUCTION

The objective of this paper is to design a QPSK modem using FPGA for SDR (Software Defined Radio). In this paper the modulator and demodulator is implemented on single FPGA kit. In which mainly concentrates on QPSK modulation techniques. In QPSK, two successive bits sequence are grouped together, this reduces the bit rate of a signaling rate ( $f_b$ ) and reduces the bandwidth of the channel.

Quadrature Phase Shift Keying (QPSK) modulation ordinary used modem chips or ASICS, to implement, but those chips usually do not have sufficient programming skill and its functionality cannot easily be changed or improved in the product development process. So those chips are not suitable the situation where the parameters changed frequently. The communication system based on FPGA is easy to implement the pipeline architecture and simple to upgrade. This is a very practical approach to implement the QPSK modulator and demodulator [1].

The FPGA implementation of  $\pi/4$  QPSK modulator and demodulator is presented complete modulator and demodulator units will be modeled using VHDL and functionality will be verified using modelsim simulation tools. The code will be synthesized onto Xilinx FPGA kit. The modulator consists of various communication modules like phase calculator, I-Q mapper, frequency synthesizer, clock generator and COS-LUT. The demodulator consists of modules COS-LUT, Negative SIN-LUT, digital multiplier integrate and dump circuit and baseband differential detector. These digital modules

will be implemented as different modules and used as components in top level entities [2].

### II. THE MODULATOR AND DEMODULATOR ARCHITECTURE

Principle of QPSK modulator— in quadrature phase shift keying (QPSK), two successive bits in the data sequence are grouped together this reduces the bit rate of a signaling rate ( $f_b$ ) and hence reduces the bandwidth of the channel. QPSK Modulator— the modulator converts the input bit stream into an electrical waveform suitable for transmission over the communication channel. Modulator is used to minimize the effect of channel noise and matching the frequency spread spectrum of transmitted signal.

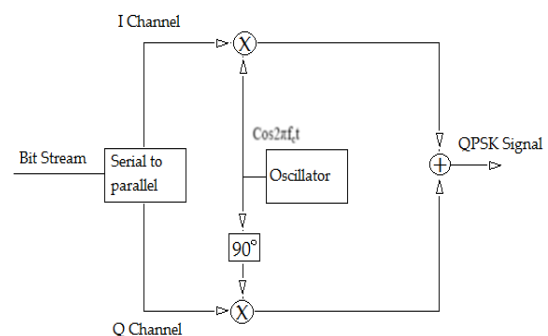


Fig (1): Block diagram of QPSK Modulator

The above fig (1) shows a block diagram of typical QPSK transmitter. The unipolar binary message stream has bit rate  $R_b$  and is first converted into a bipolar non-return-to-zero (NRZ) sequence using a unipolar to bipolar converter. The bit stream

$m(t)$  is then split into two bit streams  $m_1(t)$  and  $m_0(t)$  (in phase and quadrature streams), each having a bit rate of  $R_s=R_b/2$ . The bit stream  $m_1(t)$  is called the “even” stream and  $m_0(t)$  is called the “odd” stream. The two binary sequences are separately modulated by two carriers  $\phi_1(t)$  and  $\phi_2(t)$ , which are in quadrature. The two modulated signals, each of which can be considered to be a BPSK signal, are summed to produce a QPSK signal. The filter at the output of the modulator confines the power spectrum of the QPSK signal within the allocated band. This prevents spill-over of signal energy into adjacent channels and also removes out-of-band spurious signals generated during the modulation process. In most implementations, pulse shaping is done at baseband to provide proper RF filtering at the transmitter output.

The below fig (2) shows QPSK Modulation. In this fig  $m_1(t)$  and  $m_2(t)$  are message signal, Q-ch and I-ch are Q channel signals respectively (t) is modulated signal.

**QPSK Modulation signal:**

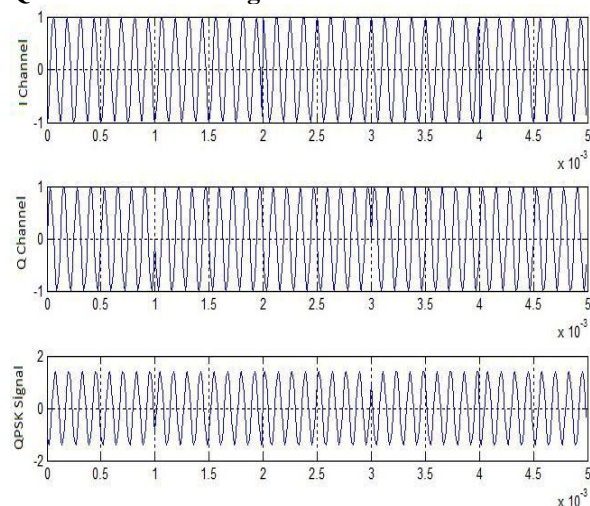


Fig (2): QPSK Modulation signal

**QPSK Demodulator:** The demodulation is the act of extracting the original information bearing signal from a modulated carrier wave. A demodulator is an electronic circuit or computer program in SDR that is used to recover the information content from the modulated carrier wave.

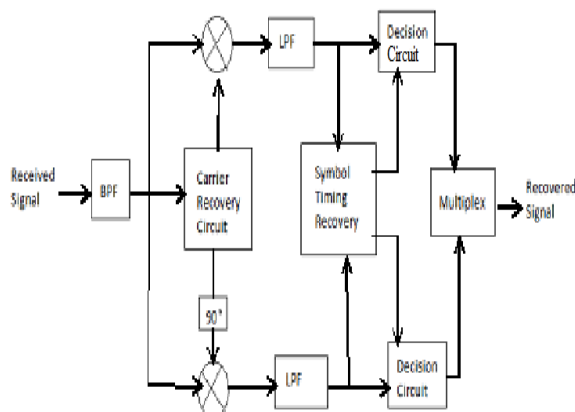


Fig (3) Block diagram of a QPSK Demodulator

The above fig shows a block diagram of a coherent QPSK demodulator. The frontend band pass filter removes the out-of-band noise and adjacent channel interference. The filtered output is split into two parts, and each part is coherently demodulated using the in-phase and quadrature carriers. The coherent carriers used for demodulation are recovered from the received signal using carrier recovery circuits. The outputs of the demodulators are passed through decision circuits which generate the in-phase and quadrature binary streams. The two components are then multiplexed to reproduce the original binary sequence.

**QPSK-Quadrature Phase Shift keying—** In QPSK two successive bits are combined this combination of two bits forms four distinct symbols. When symbol is change to next symbol the phase of the carrier changed by  $45^\circ$  ( $\pi/4$  radians). The table (1) shows symbol and their phase shifts. QPSK has double bandwidth efficiency of BPSK. In mapping of I and Q NRZ format is essential. The QPSK signal is represented mathematically in below equation (1) and I/Q are defined in equation (2, 3)

$$QPSK(t) = I(t)\cos(2\pi fct) - Q(t)\sin(\pi fct) \quad (1)$$

$$I = \sqrt{2E/T} \cos [(2i-1) \pi/4] \quad (2)$$

$$Q = \sqrt{2E/T} \sin [(2i-1) \pi/4] \quad (3)$$

**Table-1 Relation between the input symbols and the phase shifts**

Information Bits $M_i, M_q$	Phase Shifts $\pi$
11	$\pi/4$
01	$3\pi/4$
00	$-3\pi/4$
10	$-\pi/4$

Where T is symbol duration and is equal to twice bandwidth of bit rate period.  
 For  $i=1, 2, 3, 4$

The phase shifts  $\pi$  is related to input symbols mI and mQ according to the above table the in phase and in quadrature bit streams I and Q are separately modulated by two carriers and produce  $\pi/4$  QPSK waveforms given by:

$$QPSK(t) = I(t)\cos(2\pi fct) - Q(t)\sin(2\pi fct) \quad (1)$$

The vector I and Q carry one bit information

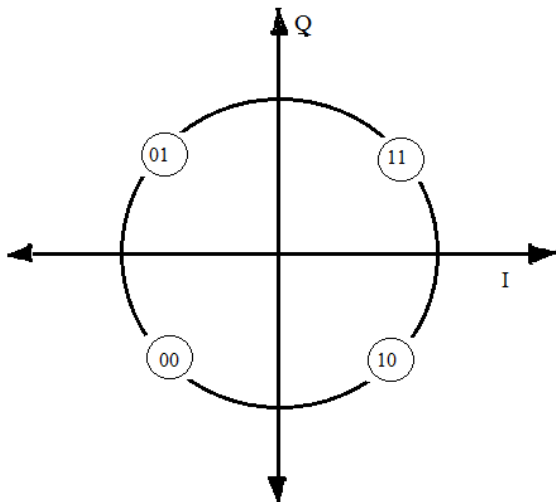


Fig (4): I-Q Mapper diagram

The above fig shows there are four symbols and the phase shifted in each symbol by  $\pi/4$  radians. Bit Error Rate— Although QPSK can be viewed as a quaternary modulation, it is easier to see it as two independently modulated quadrature carriers. With this interpretation, the even (or odd) bits are used to modulate the in-phase component of the carrier, while the odd (or even) bits are used to modulate the quadrature-phase component of the carrier. BPSK is used on both carriers and they can be independently demodulated.

As a result, the probability of bit-error for QPSK is the same as for BPSK:

$$P_b = Q(\sqrt{2E_b/N_0})$$

However, in order to achieve the same bit-error probability as BPSK, QPSK uses twice the power (since two bits are transmitted simultaneously).

The symbol error rate is given by:

$$P_s = 1 - (1 - P_b)^2$$

$$P_s = 2Q(\sqrt{E_s/N_0}) - Q^2(\sqrt{E_s/N_0})^2$$

$$P_s = 2Q(\sqrt{E_s/N_0}) - Q^2(\sqrt{E_s/N_0})^2$$

$$P_s = 2Q(\sqrt{E_s/N_0})$$

### III. DESIGN METHODOLOGIES

Generation of VHDL Codes for MATLAB-Simulink Models:

We have designed whole system using MATLAB Simulink. A MATLAB Simulation model is describing that an enable accurate performance of complete modulations and demodulation techniques. In next step to build the basic units in FPGA Spartan kit using VHDL coding. The whole problem is split down to smaller sub parts as below

- 1 Identify the basic building blocks of various communication techniques
- 2 Design the block using MATLAB Simulink with required specification
- 3 Developing an efficient mechanism using MUX
- 4 Converting different analog block to its digital equivalent block
- 5 Getting a digital equivalent output of an analog signal by sampling quantizing
- 6 Designing all the basic units in FPGA kits using VHDL coding

The different block have to combine and communicate to develop whole system.

Design flowchart is shown below—

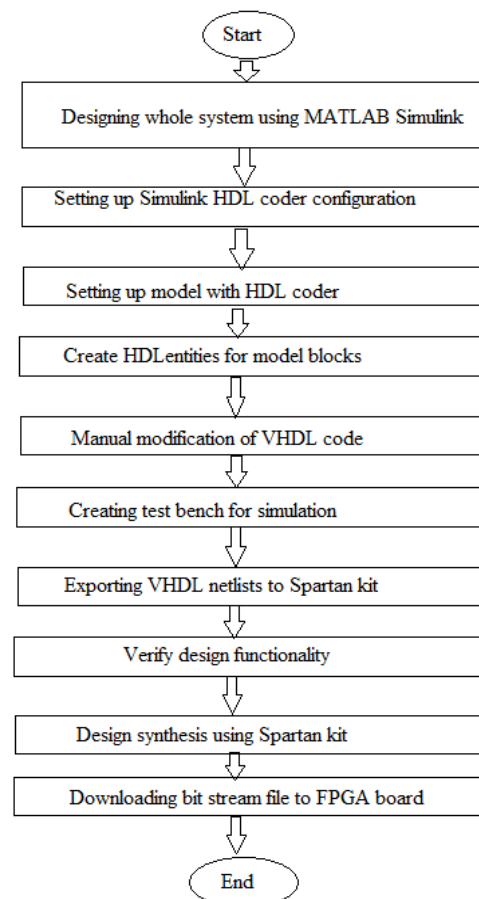


Fig (5) Design flow for MATLAB Simulink model using Spartan FPGA board.

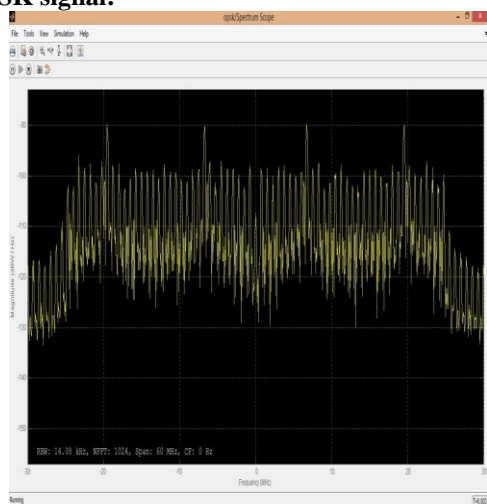
Basic building blocks—The basic building block consists of different low pass filter, High pass Filter, Integrator, multiplier, Adder, Inverter, pulse

wave generator, oscillator, sine wave generator, unipolar to bipolar converter, band pass filter, multiport switches with different control signal, transfer function =  $1/(S+1)$ , comparator, Butterworth filter ,phase shifter, message signal – different wave generator, control switches.

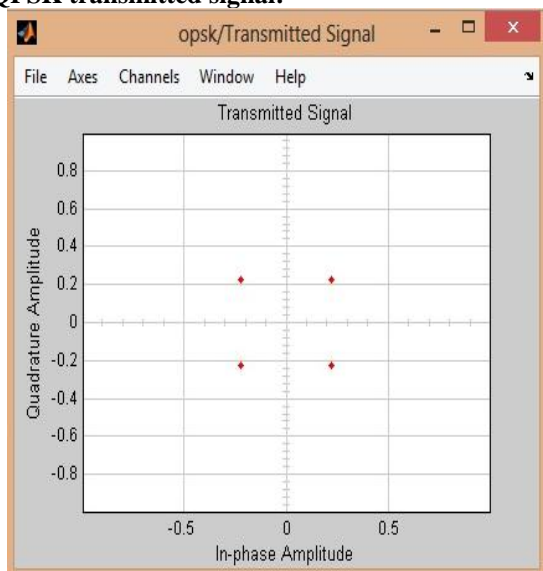
#### IV. RESULT ANALYSES

To ensure a high-quality product, diagrams and lettering MUST be either computer-drafted or drawn using India ink.

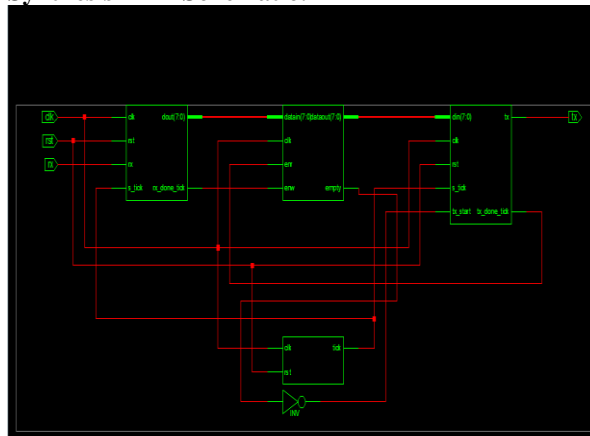
#### QPSK signal:



#### QPSK transmitted signal:



#### Synthesis RTL Schematic:



#### V. CONCLUSION

In this paper, we have presented a SDR System was successfully developed using Spartan FPGA kit. During the implementation stage, the operation of SDR was tested using MATLAB Simulink simulations, in order that the design is compiled.

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