

Design and Analysis of Comparator Using Different Logic Style of Full Adder

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ABSTRACT

In digital system the comparator is a very useful and basic arithmetic component. A compact, good cost benefit, high-performance ratio and LOW POWER comparator plays an important role in almost all hardware sorters. The basic function of a high-gain comparator is to determine whether an input voltage is higher or lower than a reference voltage—and to present that decision as one of two voltage levels, established by the output's limiting values. Comparators have a variety of uses, including: polarity identification, 1-bit analog-to-digital conversion, switch driving, square/triangular-wave generation, and pulse-edge generation. HERE a new design of comparator is described with the help of Full adder which are the basic building block of ALU and ALU is a basic functioning unit of the microprocessors and DSP. The objective of this paper is to provide small area, low power comparator for very large scale integration designers. in this paper a small power dissipation and less area over conventional 2 bit comparator is proposed and using this comparator a new style 16-bit comparator is proposed. Comparison between different designs is calculated by simulation that is performed at 0.12um technology in EDA Tool.

KEYWORDS: comparator, Low power VLSI, 90nm Technology and Micro-wind

I. INTRODUCTION

The Comparator is a very basic and useful arithmetic component of digital systems. There are several approaches to designing CMOS comparators, each with different operating speed, power consumption, and circuit complexity. One can implement the comparator by flattening the logic function directly [1-6]. Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements have been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area. One of the ways to reduce power is to explore new types of circuits in order to find better circuit techniques for energy savings. In this paper, we propose several design techniques for high performance and power-efficient CMOS comparators. Here we use Micro wind to draw the layout of the CMOS circuit. In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [7-12]. So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines

their relative magnitude. The outcome of comparison The outcome of comparison is specified by three binary variables that indicate whether $B > A$, $A = B$, $B < A$. Full adder based comparator is a 2-bit comparator consist of 2 full adders, 2 inverters at one of the input And 2 and gate at the output side. There are three outputs. One shows $A = B$ and another shows $A > B$ and $A < B$.

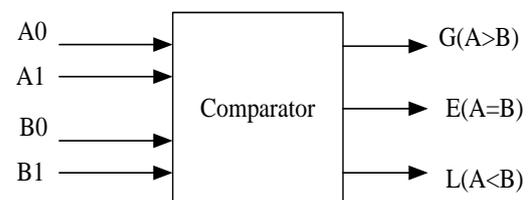


Figure 1: 2-bit comparator

Truth table of full adder based comparator is as shown below

A0	A1	B0	B1	A>B	A<B	A=B
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0

1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

II. RELATED RESEARCH WORKS

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires AND, OR gates. The basic logic diagram for full adder using its Boolean equations with basic gates can be represented as shown below.

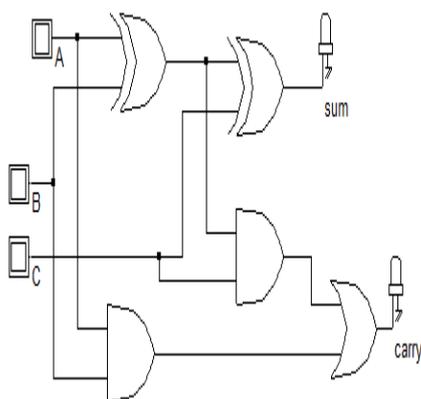


Fig.2 Logic diagram of basic full adder

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements have been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip. There by reducing the area and delay. There by reducing the area and delay. reducing the area and delay.

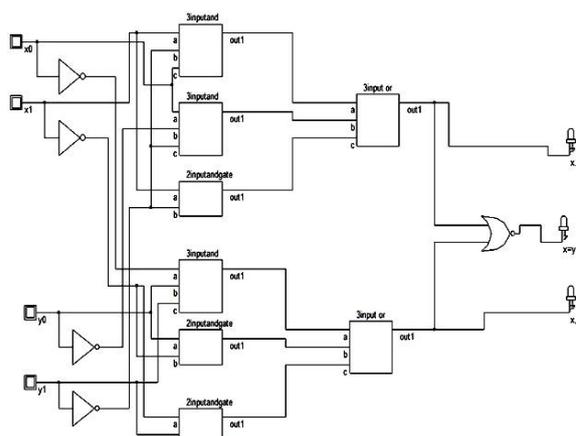


Fig.3. Logic diagram of basic full adder comparator

The layout design of the basic full adder based comparator is shown in fig.4. layout is the general concept that describes the geometrical representation of the circuits by the means of layers. Different logical layers is used by designers to generate the layout.

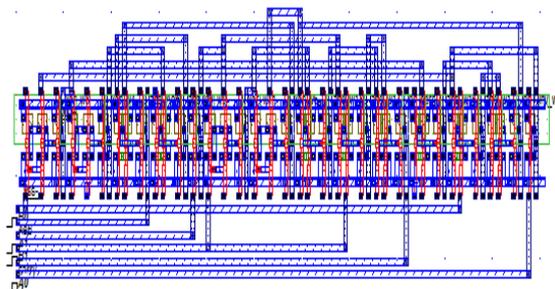


Fig.4. layout design of basic full adder based comparator

The logic diagram of hybrid full adder is as shown below .this logic style consist of two xor gate and one multiplexer.

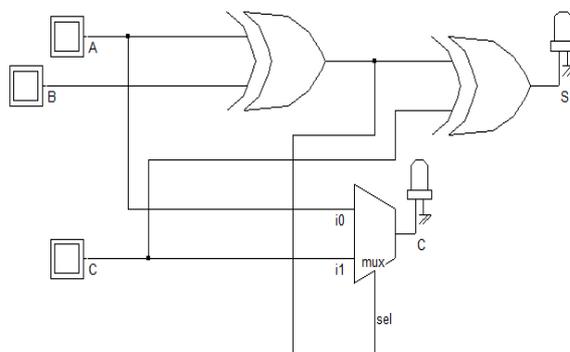


Fig.5. logic diagram of hybrid FULL ADDER

The comparator using hybrid full adder is shown in fig.6. the comparator consumes more power and area as compared to the basic full adder based

comparator. It consists of four xor gate, two multiplexer, two not gate and two AND gate. Comparator has four input (A1, A0, B1, B0) and three outputs (A=B, A>B, A<B).

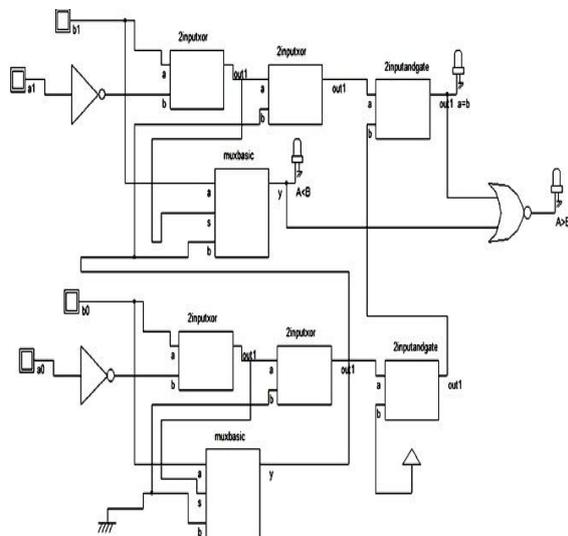


Fig.6.Logic diagram of basic full adder comparator

The layout design of the basic full adder based comparator is shown in fig.6.. layout is the general concept that describes the geometrical representation of the circuits by the means of layers. Different logical layers is used by designers to generate the layout.

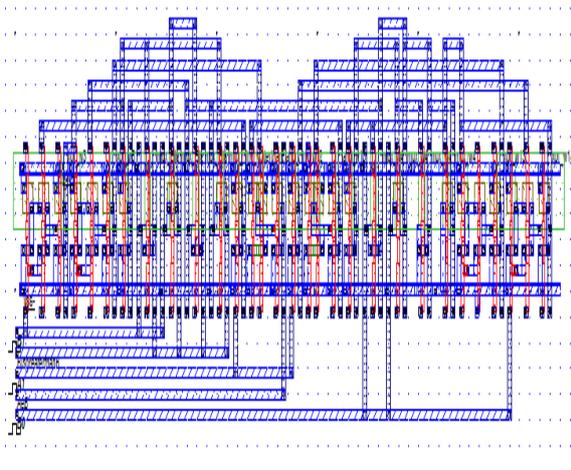
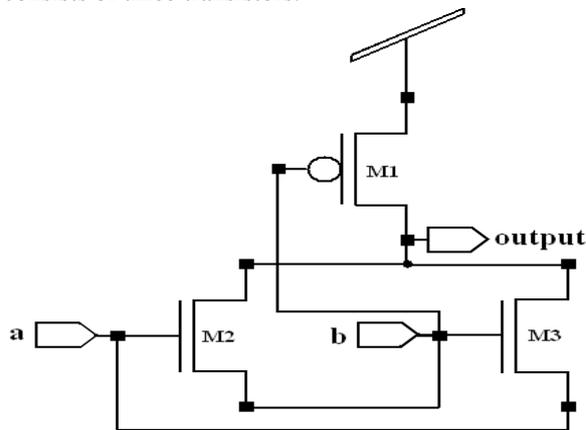


Fig.7.layout design of basic full adder based comparator

III. PROPOSED WORK

Proposed work of comparator is based on another logic style of full adder.this logic style of comparator provides less power consumption than other logic styles described in this paper. The implementation of new logic full adder based comparator is shown in fig.9.It consists of two full

adders, two inverters at one of the input and two AND gates at the output of the comparator and one ex-or gate at the output. It has four input (A1, B1, A0, B0) and three outputs(A=B, B>A,A>B).The full adder is designed by using the 3-t x-nor gate. It consists of three transistors.



3T X-NOR GATE

Fig.8.Logic diagram of 3t x-nor gate

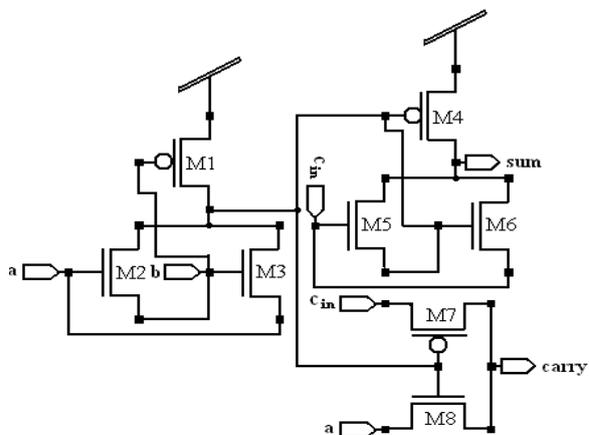


Fig.9.Logic diagram of 8stransistor full adder

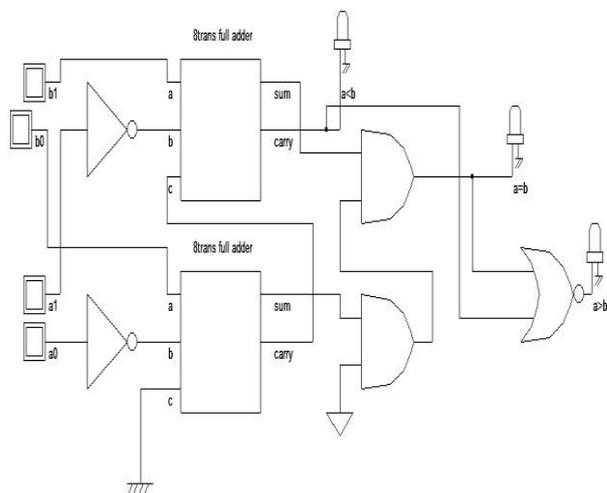


Fig.10.logic diagram of proposed full adder based comparator

This comparator consists of two 3 transistor full adders and two inverters and two and gates and the ex-or gate. The power consumption is decreases compared o the basic full adder and the hybrid full adderthe figure was shown above.

The layout design of comparator using another logic of full adder is shown in fig.10. layout is the general concept that describes the geometrical representation of the circuits by the means of layers and polygons. Different logical layers are used by designers to generate the layout. Different logical layers are used by the designers to generate the layout.

The layout for the proposed 2-bit comparator using 3-t x-or based full adder is shown below.

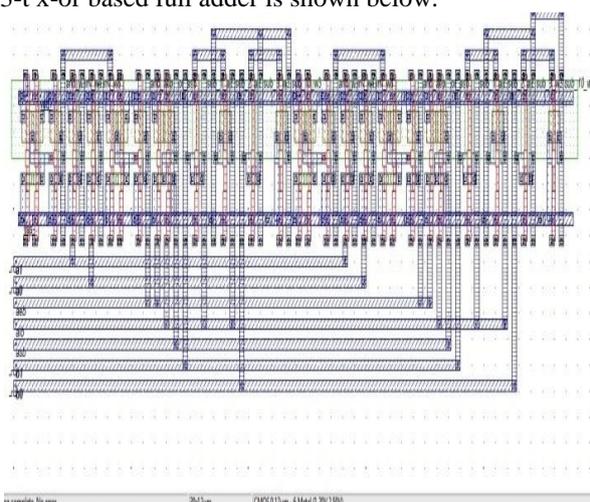
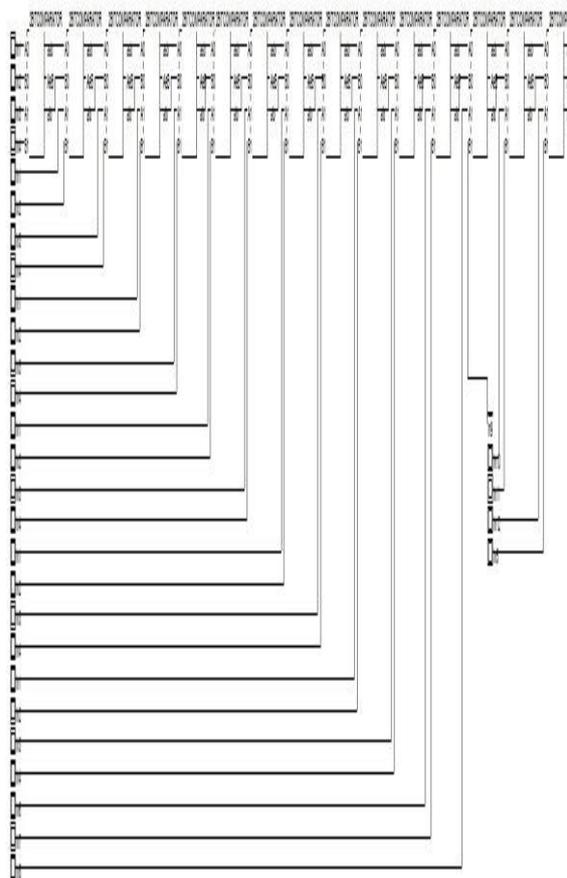


Fig.11. layout design of proposed full adder based comparator 16 bit comparator using 2- bit comparator:



The 16 bit comparator is designed based on he 2 bit comparator. It consists of 15 2-bit comparators. And it consists of 32 inputs and three outputs taken as (A<B,A=B,A>B).the figure was shown above.

IV. ANALYSIS AND COMPARISON

Analysis and comparison of different logic styles of comparator using various logic styles of full adder is shown in table.2. Simulations are obtained in Micro wind Tool. First step in obtaining the simulations is to compile the Verilog file in Micro wind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Micro wind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Micro wind. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature .the table is shown below. The future scope for this paper is designing of 16 bit comparator.

Table.2.Simulation results of various full adder based comparator

	Basic comparator	Hybrid comparator	Proposed comparator
Routed wires	25	36	24
Width	33.7	64.4	40.2
Height	9.8	9.4	9.2
Area	331.8	603.2	290.8
Power	42.289	919.0	0.818

V. CONCLUSION

This paper describes different logic styles of full adder for designing a comparator for low Power Consumption. Basic full adder based comparator Logic Style provides low power and area design as compared to other Logic Style. Hybrid comparator logic style provides high power consumption & area. The proposed comparator consumes less power as compared to other logic styles and the area consumption is less than basic full adder based, P. Heim, F. Kaese, E. Grenet, F. Heitger, P. Y. Burgi, S. Gyger and P. Nussbaum, "A 128X128 pixel 120 dB dynamic range vision-sensor chip for image contrast and orientation extraction," IEEE Journal Solid-State Circuits, vol. 38, pp. 2325-2333, 2003.

REFERENCES

- [1] H. Traff, "Naval approach to high speed CMOS current Comparator," Electron. Letter, vol. 28, no. 3, pp. 310- 312, Jan.1992.
- [2] A.T K. Tang and C. Toumazou, "High performance CMOS current comparator," Electron. Letter, vol. 30, pp. 5-6, 1994.
- [3] L. Ravezzi, D. Stoppa and G. F. Dalla Betta, "Simple High speed CMOS current comparator," Electron. Letter, vol.33, pp.1829-1830, 1997.
- [4] C. B. Kushwah, D. Soni and R. S. Gamad, "New design of CMOS Current comparator," Second International Conference on Emerging Trends in Engineering and Technology, ICETET, pp.125-129, June, 2009
- [5]. Current Comparator Design," Electron. Letter, vol. 44, no.3,pp.171-172, Jan. 2008.
- [6] Lu Chen, Bingxue Shi and Chun Lu, "A Robust High-Speed and Low-power CMOS Current Comparator Circuit," IEEE Asia-Pacific Conf. On Circuits and Systems, pp. 174-177, 2000.
- [7] S. Rahul, F. L. Richard and M. Carver, "A Low Power Wide Dynamic-Range Analog VLSI Cochlea," Analog Integral Circuits Signal Process, vol. 16, pp. 245– 274, 1998
- [8] P. F. Ruediden Brand, "Design of a comparator in a 0.25µm CMOS technology".
- [9] Niels van Bakel, Jo van comparator. By using the proposed architecture the power is reduced to 0.818microwatts and area is decreased than the other logic styles.
- [10] Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw-Hill third edition.
- [11] Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuit", Pearson Education Electronics and VLSI series, second edition.]