

Optimization and Performance Analysis of Bulk-Driven Differential Amplifier

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Abstract

In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. This paper presents a design of input stage of Operational Amplifier i.e cascode differential amplifier using a standard 65nm CMOS Technology. A comparison between gate-driven, bulk-driven and cascode bulk driven bulk-driven differential amplifier is described. The Results demonstrate that CMMR is 83.98 dB, 3-dB Bandwidth is 1.04 MHz. The circuit dissipate power of 28uW under single supply of 1.0V.

Keywords:- Common mode Rejection Ratio(CMMR), Low Voltage (LV), Low Power (LP)

I. INTRODUCTION

The reduction of minimum dimensions in CMOS technologies necessitates the downscaling of power supply voltage accordingly in integrated circuits (ICs). At the same time, increasing demands in portable and biomedical applications also require low-voltage and low-power analog and mixed signal ICs. With the development of these ICs, battery-powered electronic devices have become much smaller in size and are capable of operating much longer than ever before. In last few decades a great deal of attention has been paid to low-voltage (LV) low-power (LP) integrated circuits. Among many techniques used for the design of LV LP analog circuits, the Bulk-driven principle offers a promising route towards this design for many aspects mainly the simplicity and using the conventional MOS technology to implement these designs. This presented work focus on employing bulk driven technique in design of low voltage low power CMOS differential amplifier and to further optimize various circuit parameters for enhanced performance.

In addition, the low-voltage operation further complicates the designs of analog circuits due to limited signal swings. Conventional amplifiers require power supply voltages at least equal to the magnitude of the largest threshold voltages of the PMOS or the NMOS transistors plus necessary signal swing. Unfortunately, with the scaling of the power supply voltages, the reduction of the threshold voltage in the deep sub-micron CMOS processes over the years is not that aggressive, mostly because higher tends to provide better noise immunity. As a result, to design ultra-low voltage amplifiers with sufficient signal swings, novel circuit techniques are required. A number of low-voltage design techniques have been

developed without employing expensive low transistors, such as designs utilizing bulk-driven MOSFETs or floating-gate MOSFETs, sub-threshold design and level shifting techniques etc. Each of these methods has its advantage in specific applications.

1.1 Brief Discription of Bulk driven Approach

For a conventional gate-driven MOS transistor, we have to overcome the threshold voltage V_T to let it operate. As the feature size of modern CMOS processes scaling down, the maximum allowable power supply continuously decreases, but the threshold voltage does not scale down with the same rate.

The bulk-driven technique, which uses bulk terminal as signal input, is a promising method as it achieves enhanced performance without having to modify the existing structure of MOSFET. For a traditional MOSFET, it is mandatory to meet the requirement of $V_{GS} > V_{th}$ in order to make the MOSFET function in the triode or saturation region. In contrast, the bulk-driven technique allows even smaller voltage to be set at the input terminal but still generate saturation voltage at the output

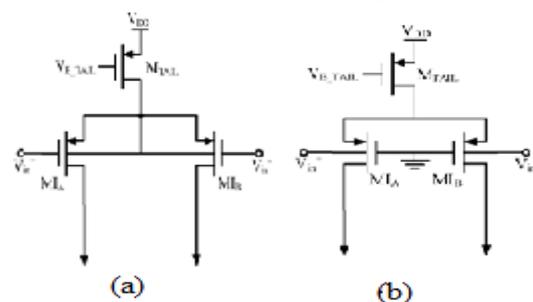


Figure 1.1: (a) Simple Gate-Driven (b) Bulk-Driven

Differential Pair

When applying this technique in the circuit design, satisfactory performance especially in the low-voltage and low-power applications can be achieved.

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A Differential amplifier is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages.

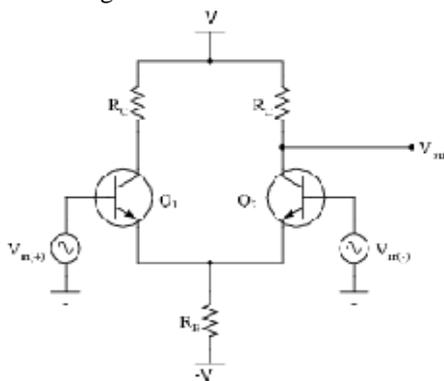


Figure 1.2 Basic Differential Pair

Many electronic devices use differential amplifiers internally. The output of an ideal differential amplifier is given by:

$$V_{out} = A_d (V_{in}^+ - V_{in}^-)$$

Where V_{in}^+ and V_{in}^- are the input voltages and A_d is the differential gain. The gain is not quite equal for the two inputs. This means, for instance, that if V_{in}^+ and V_{in}^- are equal, the output will not be zero, as it would be in the ideal case. A more realistic expression for the output of a differential amplifier thus includes a second term.

$$V_{out} = A_d (V_{in}^+ - V_{in}^-) + A_c (V_{in}^+ + V_{in}^-) / 2$$

A_c is called the common-mode gain of the amplifier.

As differential amplifiers are often used when it is desired to null out noise or bias-voltages that appear at both inputs, a low common-mode gain is usually considered good.

The common-mode rejection ratio, usually defined as the ratio between differential-mode gain and common-mode gain, indicates the ability of the amplifier to accurately cancel voltages that are common to both inputs.

In a perfectly symmetrical differential amplifier, A_c is zero and the CMRR is infinite. Note that a differential amplifier is a more general form of amplifier than one with a single input; by grounding one input of a differential amplifier, a single-ended amplifier results. An operational amplifier, or op-amp, is a differential amplifier with very high differential-mode gain, very high input impedances, and a low output impedance. Some kinds of differential amplifier usually include several simpler differential amplifiers. For example, an instrumentation amplifier, a fully differential amplifier, an instrument amplifier, or an isolation amplifier are often built from several op-amps.

The word “cascode” was originated from the phrase “cascade to cathode”. This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance. As the output impedance increases gain increases and power consumption decreases.

II. PROPOSED WORK

In bulk-driven technique, if the gate terminal is biased properly to turn on the MOSFET The negative signal can be applied between the bulk and the source junctions of the MOSFET so the source and body reverse biased and the current flow to ground through body.

In gate driven differential pair the input signals $In1$ and $In2$ are given at the gate terminals of the NMOS_3 and NMOS_4 and the Bulk of these is connected to negative voltage.

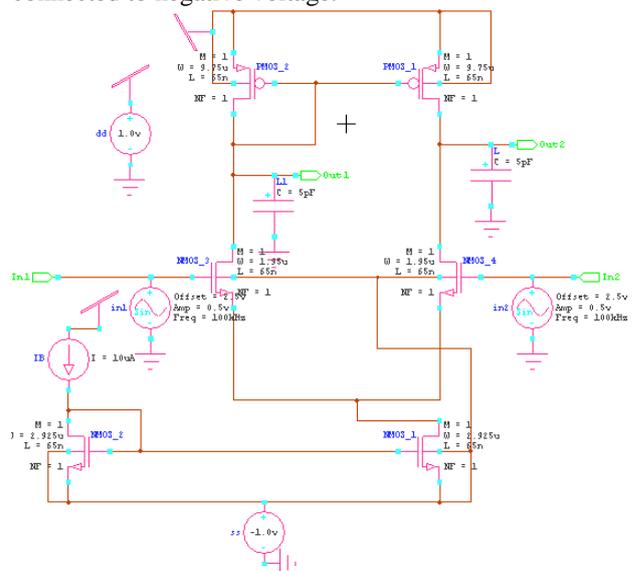


Figure 2.1: Gate driven Differential Amplifier

From the input signal the transistor gets the sufficient voltage to turn ON. PMOS_2 and PMOS_4 at as load. Here, we are not using the

resistor because they require large area on the chip during fabrication. Only PMOS transistor are taken because they are good passer of 1's. The current mirror is used for sinking the circuit. In This presented design Simple current mirror is selected. In current mirror same current flows in the two arms. Voltage source Vdd supply the voltage. In this circuit, let I current flows , then in NMOS_3 current is I1 and there is increase in the current suppose ΔI. On the other hand, the current flowing in NMOS_4 is I2 there is decrease in the current by ΔI. The main principle is that

$$I = I_1 + I_2$$

$$I = (I_1 + \Delta I) = (I_2 - \Delta I)$$

These circuits are much less sensitive to noise and interference as the difference of the signal is sensed, it will have no interference component.

In bulk-driven technique, if the gate terminal is biased properly to turn on the MOSFET The negative signal can be applied between the bulk and the source junctions of the MOSFET so the source and body reverse biased and the current flow to ground through body.

The operation of the bulk-driven MOSFET is similar to a JFET. Once the inversion layer beneath the gate of the transistor is formed by sufficient gate-to-source biasing voltage here 700mV, the channel current can be modulated by varying the bulk-to-source junction potential. This operation eliminates the threshold limitation of the gate-driven MOSFETs where the bulk-to-source junction can be either negative, zero, or slightly positive biased while still acting as the high impedance node. The gates of the transistor NMOS_3 and NMOS_4 are biased by small voltage 700mV to ensure that both the devices operating in the saturation region.

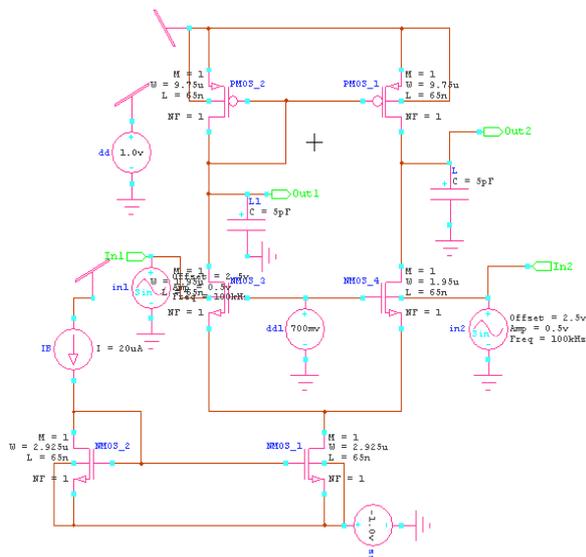


Figure 2.2: Bulk Driven Differential Amplifier

The dynamic range of the amplifier is increased since there is no threshold voltage associated with the bulk terminal, which allows a low-voltage operation. The gain increases.

The main problem associated with the bulk-driven technique is that the bulk Transconductance, is substantially smaller than the gate transconductance. This insufficient transconductance will affect the performance of the amplifier, such as unity gain bandwidth (UGBW), open loop gain, input referred noise, etc

The main advantage of this type of circuit is that the output impedance is more than the above circuits and the output voltage range is also increased as compared to the other architectures. It Control the frequency behaviour

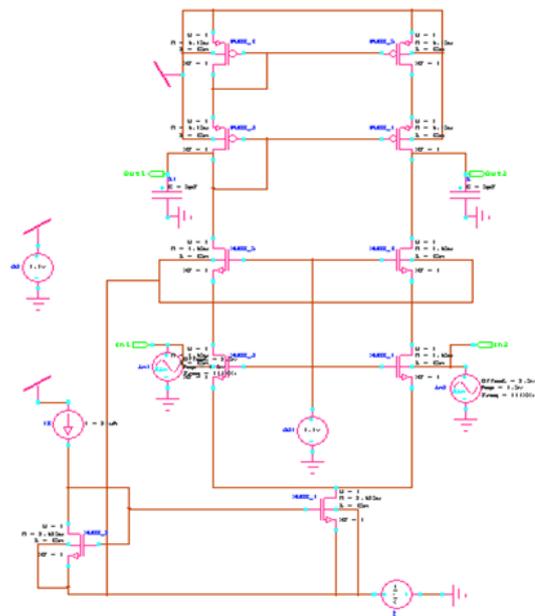


Figure 2.3: Cascode Bulk Driven Differential Amplifier

It gives more gain by increasing the output resistance of a stage and have a good noise performance.

As the output gain is the product of transconductance (gm) and resistance of output stage.

$$A_v = g_m * r_o$$

As the output resistance increases the overall gain of the of the circuit increases. The Common mode rejection ratio also increases and the power consumption of the circuit decreases.

III. SIMULATION AND RESULTS COMPARISON

Cascode Bulk driven differential amplifier is presented which is the input stage of the op amp and simulated using T-spice , 0.65µm technology. All the simulations are with MOSFETs of same length and varying width input voltage (VIN).

Technique	Technology (nm)	3-dB Bandwith (MHz)	Differential Gain (dB)	Common mode Gain (dB)	CMMR	Power Consumption (µW)
Gate-Driven	180	0.6036	37.37	-35.08	72.37	151.3072
Gate-Driven	65	2.44	20.90	-23.14	44.04	80.51383
Bulk-Driven	65	7.03	20.88	-37.96	58.84	173.6512
Cascode Bulk Driven	65	1.04	28.65	-55.33	83.98	28.54598
Rf [12]	35	-	-	-	65	130

Table1: Comparison between different techniques of Designing Differential Amplifier

Parameter	Simple current mirror	Wilson current mirror	Improved Wilson current mirror	Cascode current mirror	Improved Cascode Current Mirror
Differential Gain(dB)	28.65	34.60	34.77	34.87	19.07
Common mode gain(dB)	-55.33	-78.77	-77.44	-78.35	-63.66
CMMR	83.98	113.37	112.11	113.22	82.73
Power consumption(µW)	28.54599	20.15470	21.41823	21.39926	20.00006
3-dB Bandwidth	1.04	40.43	0.146	0.151	0.701

Table 2: Comparison between differential amplifier using different current mirrors

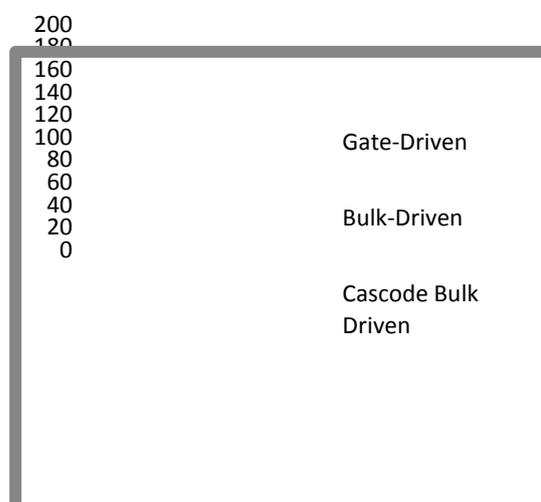


Figure 3.1 Comparison chart of parameters using Different Techniques of Design.

IV. CONCLUSION & FUTURE WORK

4.1 Conclusion

In this presented work, the design of Differential Amplifier and simulated cascode bulk driven differential amplifier in 65nm CMOS Technology. Simulation results showed increased Common mode rejection ratio (CMMR) with lower power consumption. Designed Differential Amplifier has also better Differential and Common mode gain. Different techniques of the Differential Amplifier are studied keeping in view the low power consumption requirements. The gate driven technique and bulk driven technique firstly chosen to reduce the power consumption. With gate driven technique , the dynamic range is low because of threshold associated with gate. Bulk driven have limitation of transconductance and hence power consumption is not as low as in gate but other paramters improved. Cascode bulk driven provide better gain ,CMMR and very low power Consumption in Comparison to other two.

4.2 Future Scope

With the development of ICs, battery-powered electronic devices have become much smaller in size and are capable of operating much longer than ever before. So Devices that consume less power are required. This Differential Amplifier can be used as the input stage for designing the Operational Amplifier with improved UGBW and open loop gain , as well as enhancement in other Op-Amp performance parameters.

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