RESEARCH ARTICLE OPEN ACCESS

8 Bit RISC Processor Using Verilog HDL

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Abstract
RISC is a design philosophy to reduce the complexity of instruction set that in turn reduces the amount of space, cycle time, cost and other parameters taken into account during the implementation of the design. The advent of FPGA has enabled the complex logical systems to be implemented on FPGA. The intent of this paper is to design and implement 8 bit RISC processor using FPGA Spartan 3E tool. This processor design depends upon design specification, analysis and simulation. It takes into consideration very simple instruction set. The momentous components include Control unit, ALU, shift registers and accumulator register.
Keyword: RISC, control unit, processor.

I. Introduction

Now days, Computers are mainstream in quotidian activities. RISC Processor is a CPU design strategy that uses simplified instructions for higher performance with faster execution of instruction. It also reduces the delay in execution. It uses general instructions rather than specialized instructions. They are less costly to design, test and manufacture. This has helped in implementation of RISC in technological field. Its range of application includes signal processing, convolution application, supercomputers such as K computers and wider base for smart phones.

In this work, an 8 bit RISC processor is presented with higher performance and efficiency being the main aim. This processor comprises of Control unit, general purpose registers, Arithmetic and logical unit, shift registers. Control unit follows instruction cycle of 3 stages fetch, decode and execute cycle. According to the instruction to the fetch stage, control unit generate signal to decode the instruction. The architecture supports 16 instructions for arithmetic, logical, shifting and rotational operations.

The whole paper is divided into the following sections. Section I describes the architecture of the processor. Section II explains the various modules of the processor. Result has been presented in the section III.

II. Architecture

The architecture of 8 bit RISC processor has been shown in the figure 1. It comprises of Control unit, general purpose register, ALU, Barrel shifter, universal shift register and accumulator. The control unit consists of two registers i.e instruction register and instruction decoder. Instruction and data are fetched sequentially in order to reduce the latency in the machine cycle. Pipeline structure has been incorporated that further utilizes three execution cycle fetch, decode and execute. This pipeline structure helps in enhancing the speed of operation.

In fetch cycle, instruction and relevant data are inferred from the memory while in decode cycle, instruction and data drawn from the memory are bifurcated to activate component and data path for execution and in the execution cycle instruction is executed, data is manipulated and result is stored in the accumulator.

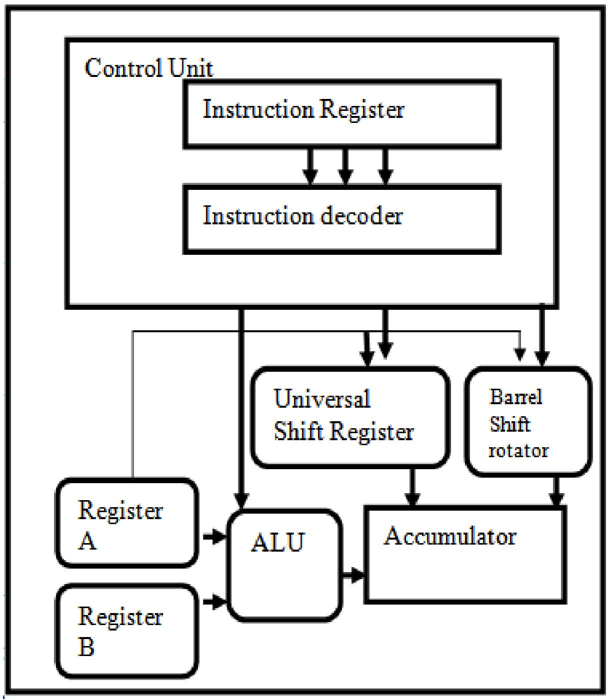


Figure 1.Architecture of 8 bit RISC processor

The control unit accept the opcode and generate the signal that triggers the components and data path to work accordingly and perform the desired function. The control unit has two instruction decoders. These two decoders decode the instruction bits and direct the signal to either into ALU, universal shift register or barrel shift rotator. The operands are received from register A or register B. Upon receiving the operands from registers and the decoded instruction bits arithmetic and logical unit perform arithmetic and logical functions. Universal shift register and barrel shift rotator receives the input from register A and depending upon the decoded information perform the desired operation of either shifting or rotation and the result is stored in the accumulator register.

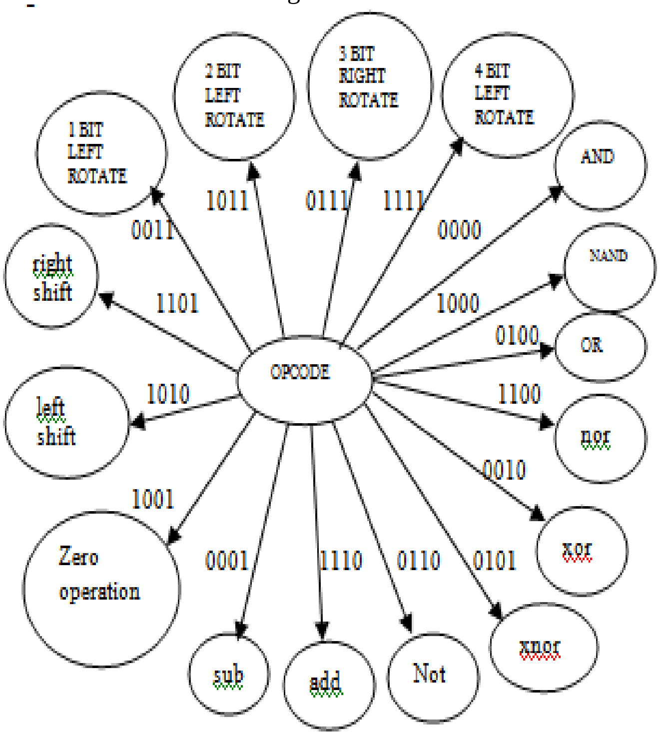


Figure 2.State diagram

III. Modules in the design of 8 bit RISC Processor

Modules are the building blocks of a Processor. This segment deals with the modules of 8 bit RISC processor. Control Unit, ALU, general purpose register, universal shift register, barrel shift rotator and accumulator are main modules of the processor.

1. Control Unit :

The control unit is based on state diagram as depicted in the figure 2. The state machine performs the functions of arithmetic, logical, shifting and rotating functions. If bit instruction is 0100 then OR operation is performed as soon as next instruction is received then appropriate operation is performed. The control unit consists of two decoders. The first decoder performs arithmetic and logical function and the second decoder performs shifting and rotating operations. The top block of control unit is shown in the figure 3,

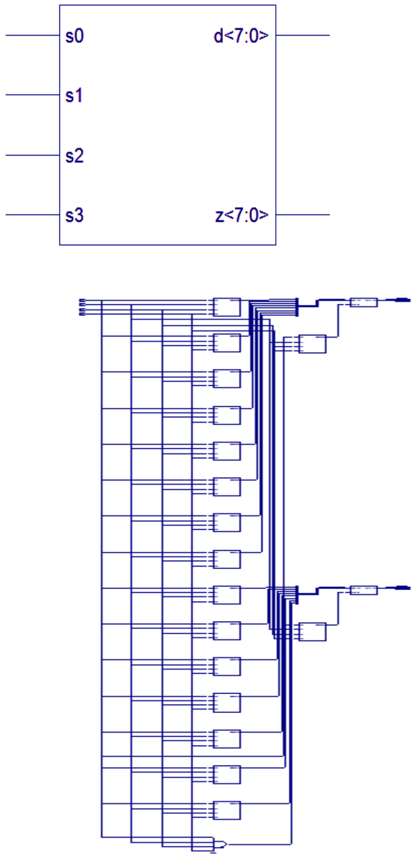


Figure 3.Control Unit top block

2. ALU

Arithmetic and logical unit is a digital circuit that performs arithmetic and logical operations. The proposed design performs seven logical functions and two arithmetic functions. The logical operations to be executed are AND, NAND, OR, NOR, XOR, XNOR and NOT while two logical operations are performed Addition and Subtraction. ALU will receive instruction bits from control unit and will execute the desired operation. For example, if input to control unit is 0000, the decoded bits will be 10000000 and after receiving the instruction bits from the decoder AND operation is performed by ALU according to the operands from register A and register B. The top block is shown in the figure 4.

Select lines				Decoder Output								Functions Performed
s0	s1	s2	s3	d0	d1	d2	d3	d4	d5	d6	d7	Operations
0	0	0	0	1	0	0	0	0	0	0	0	AND
1	0	0	0	0	1	0	0	0	0	0	0	NAND
0	1	0	0	0	0	1	0	0	0	0	0	OR
1	1	0	0	0	0	0	1	0	0	0	0	NOR
0	0	1	0	0	0	0	0	1	0	0	0	XOR
0	1	0	1	0	0	0	0	0	1	0	0	XNOR
0	1	1	0	0	0	0	0	0	0	1	0	Subtraction
1	1	1	0	0	0	0	0	0	0	0	1	Addition
s0	s1	s2	s3	Zo0	Zo1	Zo2	Zo3	Zo4	Zo5	Zo6	Zo7	
0	0	0	1	1	0	0	0	0	0	0	0	Not

Table 1. Operation of ALU

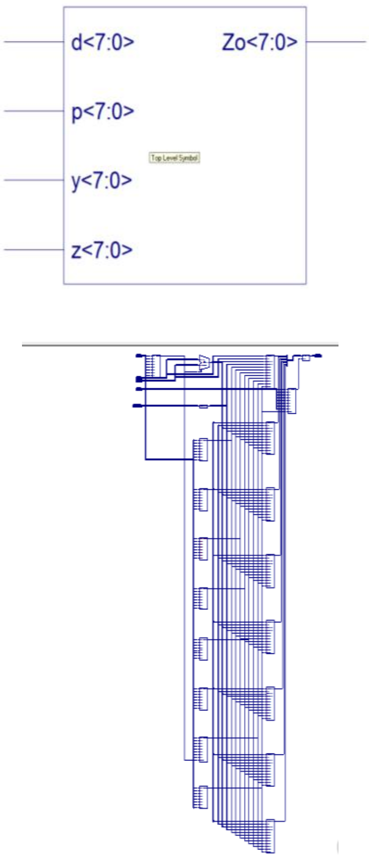


Figure 4. ALU Top Block

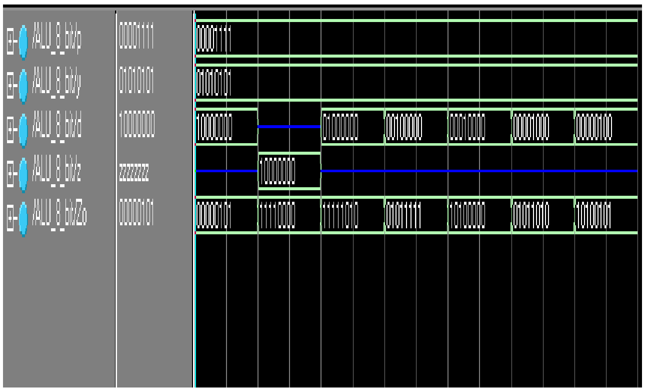


Figure 5. ALU Simulation Result

3. Barrel Shifter:

Barrel shifter is shown in the figure 6. It is a digital circuit that shifts the number of bits by specified times. It will receive the decoded intruction bits from the second intruction decoder inside the control unit and performs the desired operation depending upon operand from register A and select lines.

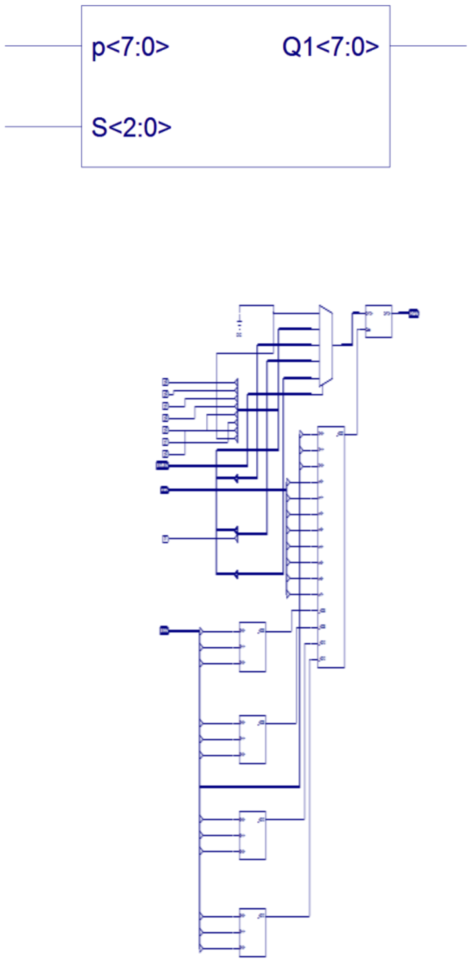


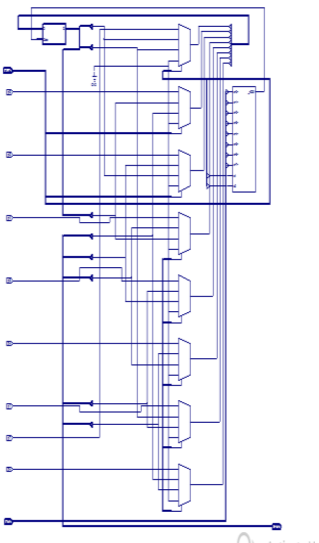
Figure 6. Barrel shifter Top block

Select lines			Decoder output								Function performed
S0	S1	S2	Zo0	Zo1	Zo2	Zo3	Zo4	Zo5	Zo6	Zo7	Operations
0	0	0	0	1	0	0	0	0	0	0	Zero opration
0	0	1	0	0	0	0	1	0	0	0	1 bit left rotate
0	1	0	0	0	0	0	0	1	0	0	2 bit left rotate
0	1	1	0	0	0	0	0	0	1	0	3 bit right rotate
1	0	0	0	0	0	0	0	0	0	1	4 bit left rotate

Table 2. Operation of Barrel shifter

4. Universal Shift Register

The achitecture is shown in the figure 7. This architecture performs four main functions as follows loading the value, left shift and right shift and no change. If s4 and s5 both are low while z is equal to 01000000 the value is loaded. If s4 is low and s5 is high with decoded output z as 00100000 left shift operation is performed.



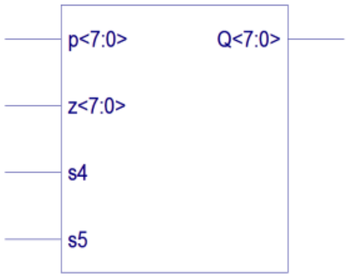


Figure 7. Universal Shift register Top block

Select lines		Decoder output								Functions performed
s4	s5	Zo0	Zo1	Zo2	Zo3	Zo4	Zo5	Zo6	Zo7	Operations
0	0	0	1	0	0	0	0	0	0	Load
0	1	0	0	1	0	0	0	0	0	Left shift
1	0	0	0	0	1	0	0	0	0	Right shift
1	1	0	0	0	0	1	0	0	0	Zero operation

Table 3. Operation of Universal shift register

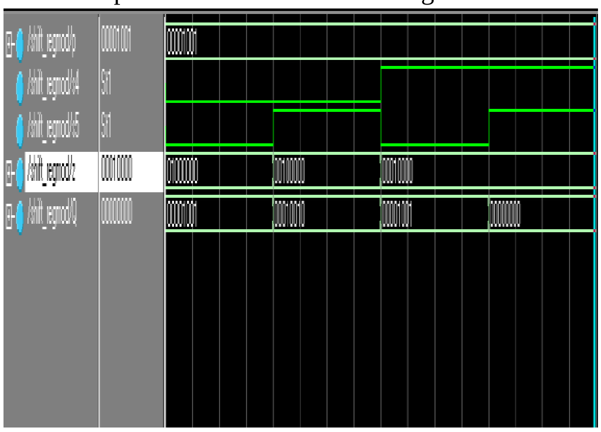


Figure 8.Universal shift register simulation result

5. General Purpose Register

General purpose register stores the 8 bit data. There are total 8 D flip flops. Two general purpose registers are A and B. If reset is high then register is clear, on the other hand if reset is low, rd is taken to be high and clock is high data is stored in the register. It is shown in the figure 9.

Input				Output
Clk	reset	**rd**	**A7 A6 A5 A4 A3 A2 A1 A0**	**P7 P6 P5 P4 P3 P2 P1 P0**
1	1	**x**	**X X X X X X X X**	**0 0 0 0 0 0 0 0**
1	0	**1**	**0 0 0 0 1 1 0 0**	**0 0 0 0 1 1 0 0**

Table 3.Operation of General purpose register

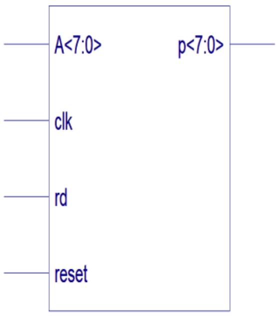


Figure 9.General purpose register Top Block

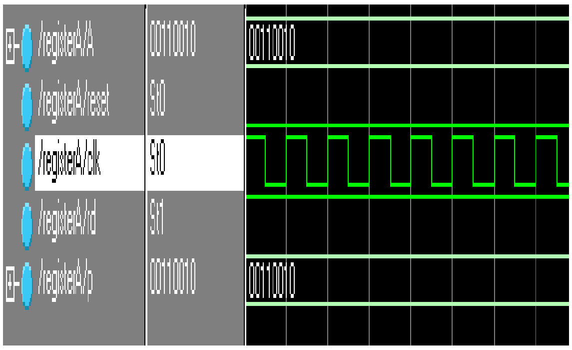


Figure 10.General purpose register Simulation result

6. Accumulator Register:

Accumulator register top block is shown in the figure 11.The result from ALU or universal shift register or barrel rotator is stored in the accumulator register. If reset is set to high then accumulator register is cleared otherwise 8 bit result is stored in the accumulator register.

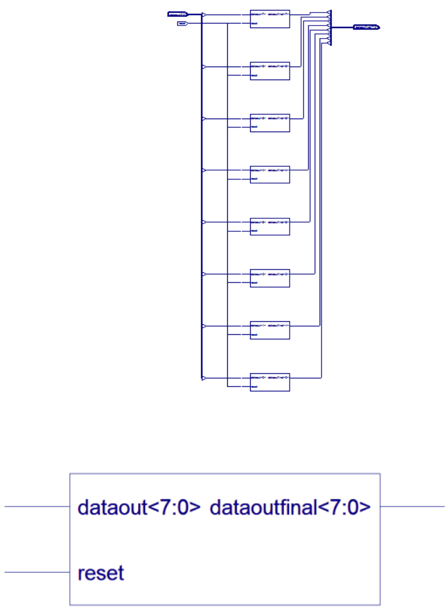


Figure 11.Accumulator register top block

Figure 12.Accumulator simulation result

IV. RESULT

The performance of 8 bit RISC processor has been scrutinized using Xilinx Spartan 3E technology. The design meets the requirement of high speed, extremely low cost and consumer oriented design.

The overall design has been shown in the figure. The data is received from two 8 bit registers A and B. Signal READ(rd) is a memory interface signal. This signal adumbrates the memory location to be read and data to be put into the data bus.

The synchronization is done utilizing clk signal. Design of processor has been accomplished using two control signals namely rd and reset. If reset is high, processor will not perform any operation and continue to remain in idle state. If reset is low and rd is high data is loaded into register. Depending upon the opcode from control unit the processor performs the operation.

This 8 bit RISC processor works on one clock cycle. clk is the external clock signal and triggers the input and result in the output. rd triggers the state of registers A and B. s0 to s3 specifies the opcode to enable the operation. If opcode is 0100 then OR operation is performed.

V. CONCLUSION

An 8 bit RISC processor with 16 instruction set has been designed. Every instruction has been executed in one clock cycle with 3 stage pipelining. Verification has been endeavored by exhaustive simulation. The processor can be used for mathematical computation in portable calculators as well as in gaming tool kit.

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