

Glitch Reduction in Low- Power Low- Frequency Multiplier

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ABSTRACT

Multiplication is an essential arithmetic operation for common DSP applications, such as filtering and fast Fourier transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP systems. A straightforward approach is to design a full adder (FA) that consumes less power. Power reduction can also be achieved through structural modification. For example, rows of partial products can be ignored. In this project a 10 transistor full adder is designed for low power which is used in the implementation of different types of multipliers. All these multipliers are compared for different technologies. A power gating technique is used by placing an MTCMOS cell is used at fine grain level so as to minimize the leakage power.

Keywords – Multiplier, Glitch, Power gates, Half adder and Transmission gates

I. Introduction

The next generation of wireless network requires High-Speed and low- power Digital Signal Processing(DSP) System-on-Chip(SoC).Amongst the building blocks of a DSP system a Multiplier is an essential component that has a significant role in both Speed and Power performances of the entire system. Most digital signal processor (DSP) systems incorporate a multiplication unit to implement algorithms such as Convolution and Filtering. In many DSP algorithms, the Multiplier in the critical path and ultimately determines the performance of the algorithm. However, the demand for High-Performance portable systems incorporating multimedia capabilities has elevated the design for Low-Power to the forefront of design requirement in order to maintain reliability and provide longer hours of operation. Comparing with other functions, the longest delay in Multiplier corresponds to the adder, so it is necessary to design a faster one. Multipliers are on the critical path of many computational applications .Examples are Real-time Digital Signal Processing, Floating Point applications, or Computers. Designing Low-Power fast Multipliers has been a great theoretical and practical interest for computer scientists and engineers. Several algorithms and VLSI implementations have been proposed and practically used. The proposed High-Speed multiplication algorithm which postpones the carry-propagation to the last stage where two $2(n-1)$ -bit numbers are added using a fast carry-look-ahead adder (CLA). Depending on the application, one of the parameters like speed, power consumption, or area might be of great priority. Based on this

criterion, the designer may decide to design the Multiplier. It was decided to optimize the Multiplier for Low-Power operation, so here there is a compromise between speed and power, the power is chosen as the first priority. After power, the other priorities are Speed and Area, respectively. In the signal processing offered in modern audio applications, multipliers are certainly among the most power-hungry elaboration units. Three fundamental approaches have been proposed to abate glitch generation and propagation in array multipliers, namely:

- 1) Shortening full-adder chains.
- 2) Equalizing internal delays.
- 3) Aligning sum and carry signals.

In this project, we first propose a MTCMOS cell to minimize the leakage and total power consumption of a static CMOS circuit for a given performance. In a conventional design area overhead and power consumption will be more. So that in order to reduce the area overhead and power consumption of a particular CMOS circuit MTCMOS cell is used. Due to this area and total power decreases significantly.

II. Subsystem Design Components

2.1 Power gating

Power Gating is effective for reducing leakage power. Power gating is the technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall leakage power of the chip. This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required for operation once

again they are activated to "active mode". These two modes are switched at the appropriate time and in the suitable manner to maximize power performance while minimizing impact to performance. Thus goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode.

2.2. Types of Multipliers

Multipliers are categorized relative to their applications, architecture and the way the partial products are produced and summed up. Based on all these, a designer might find following types of multipliers.

2.2.1 Array Multiplier

Array Multiplier is an efficient layout of a combination multiplier. It accepts all bits simultaneously. The longest product calculation delay in it depends on the speed of the adders. An n-bit multiplier requires 'n (n-1)' full adders and 'n²' AND gates. In array multipliers, the counters and compressors are connected in a serial fashion for all bit slices of the Partial Product parallelogram. There are several possible array topologies including simple, double and higher order arrays.

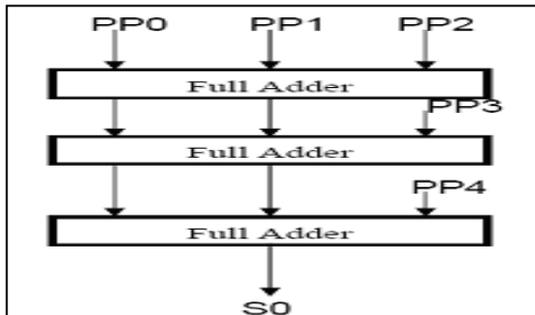


Fig 1: Array multiplier structure

2.2.2 Tree multipliers

In order to speed up the process of addition of partial products, tree based structure is used. In tree architecture, the compressors are connected for each bit slice in the PP parallelogram. Normally, they are used in parallel. Although the trees are faster than arrays, they both use the same number of compressors to reduce the partial products.

2.2.3 Serial multipliers

Bit serial arithmetic is a viable alternative in digital signal processing applications to traditional bit-parallel arithmetic. The major advantage of bit serial arithmetic is that it significantly reduces chip area. This is done in two ways; first it eliminates wide buses and simplifies wire routing. Secondly, small processing elements are used which make the chip smaller and require short wiring. Most of the bit serial multipliers are based on the shift and add

algorithm where several bit products are added in each time slot. Bit serial multipliers are classified as serial/parallel multiplier, Transposed serial/parallel multiplier and S/P multiplier-accumulator.

2.3 TRANSMISSION GATES

A CMOS transmission gate is created by connecting an nFET and pFET in Parallel. The nFET Mn is controlled by the signal s, while the pFET Mp is controlled by the complement s. When wired in this manner, the pair acts as a good electrical switch between the input and the output variables x and y respectively.

The operation of the switch can be understood by analyzing the two cases for s. if s=0, the nFET is OFF; since $\bar{s} = 1$, the pFET is also OFF, so that the TG acts as an open switch. In this case, there is no relationship between x and y. For the opposite case where s=1 and $\bar{s} = 0$, both FETS are on, and the TG provides a good conducting path between x and y. logically, this is identical to the switching of an nFET so that we may write

$$Y = x.s \text{ if } s=1 \dots\dots\dots (1)$$

This assumes that x is the input and y is the output. However, the TG is classified as a bi-directional switch. The TG symbol is based on this observation. It is created using two back-to-back arrows indicating that the data can flow in either direction. Control is achieved by s and \bar{s} ; the bubble indicates connection to the pFET gate.

Transmission gates are useful because they can transmit the entire voltage range [0,vDD] from left to right(or vice versa).This is due to the parallel connection of the transistors. Zero voltage levels are transmitted by the nFET, while the pFET is responsible for transmitting the power supply voltage VDD. The first paragraph under each heading or subheading should be flush left, and subsequent paragraphs should have a five-space indentation. A colon is inserted before an equation is presented, but there is no punctuation following the equation. All equations are numbered and referred to in the text solely by a number enclosed in a round bracket.

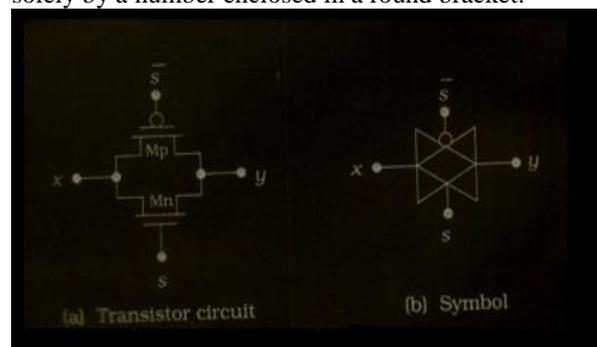


Fig 2: Transmission gate

III. DESIGN OF MULTIPLIER CIRCUIT STRUCTURES

3.1 CELL-1 STRUCTURE

The 4X4 bit Array Multiplier has two different cells which are named as cell-1 and cell-2. The implementation of cell-1 consists of conventional 36 transistor full adder as shown in figure 3.

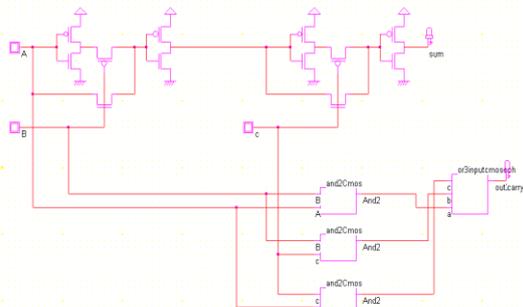


Fig 3: Schematic view of the designed cell-1 structure

3.2 CELL-2 STRUCTURE

The second type of cell named as cell-2 consists of 10-Transistor full adder cells and MTCMOS cells. The full adders used in cell-2 can be designed by using 10-Transistors and the design. The schematic view of the cell-2 structure is as shown in figure 4.

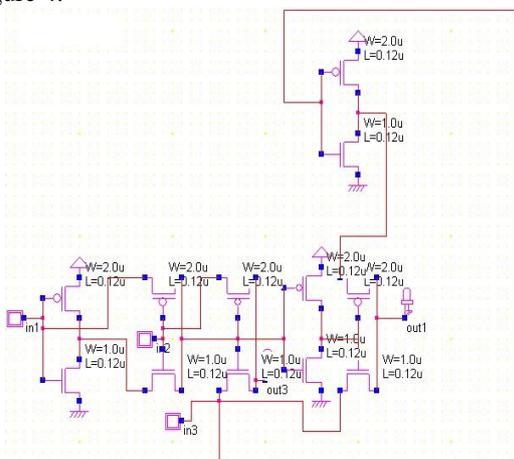


Fig 4: Schematic view of the designed cell-2 structure

IV. DESIGN OF 4X4 ARRAY MULTIPLIER BLOCK

We designed the 4x4 array multiplier using cell-1 and cell-2 structures.

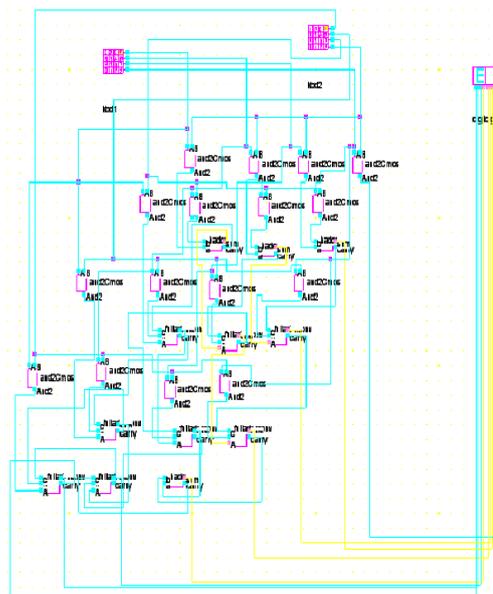


Fig 5: Schematic view of the designed 4X4 Array Multiplier

4.1 Simulated result and layouts

The simulated result of designed the 4x4 array multiplier using cell-1 and cell-2 structures is shown below.



Fig 6: Simulated result

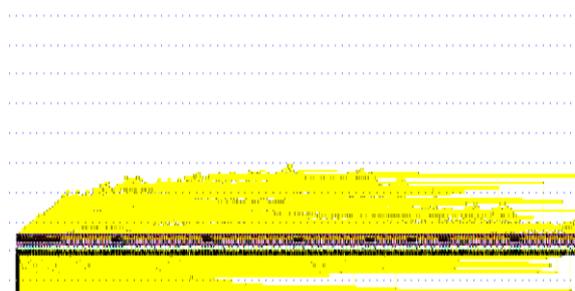


Fig 7: layout output

V. CONCLUSION

Power optimization can be done at different levels at the design, i.e at system level, algorithm level, architecture level, logic level, circuit level, etc. Here a 1-bit full adder is designed for low power and minimum area. This can be called as a high performance design as the number of transistors is reduced in the circuit which consumes less power. Here it is observed that a 65-70% of area overhead is reduced as well the power.

Different multipliers are constructed using this full adder for low power, which is an important block of the design as this is repeatedly used. To produce each and every partial product more than 50% of performance improvement is observed for every multiplier that is being constructed.

REFERENCES

- [1]. flavio carbognani, felix buergin, norbert felber, hubert kaeslin, member, ieee, and wolfgang fichtner, fellow, ieee "transmission gates combined with level-restoring cmos gates reduce glitches in low-power low-frequency multipliers" *IEEE transactions on very large scale integration (vlsi) systems*, vol. 16, no. 7, july 2008.
- [2]. john p. uyemura "cmos logic circuit design" springer international edition-2005 34
- [3]. john p. uyemura "chip design for submicron vlsi" thomson india edition-2007.
- [4]. neil h.e.weste, david harris, ayan banerjee "cmos vlsi design" third edition pearson education india edition-2006.
- [5]. douglas a. pucknell, kamran eshragian "basic vlsi design" prentice hall of india pvt ltd third edition-2005.
- [6]. M. Alioto and G. Palumbo, "Analysis and comparison on full adder block in Submicron technology," *IEEE Trans. Very Large Scale Integer. (VLSI) Syst.*, vol. 10, no. 6, pp. 806–823, Dec. 2002.
- [7]. J.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18- μ m full adder Performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integer. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.
- [8]. A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of Low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integer. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.