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Power Analysis of CMOS Combinational Logic Circuits Using Adiabatic Reduction Technique at 180nm Technology

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Abstract
In recent years the adiabatic techniques have been used to reduce power consumption in various high end processors. Various adiabatic logic circuits have been proposed based on the energy recovery principle. The term "adiabatic" is derived from a reversible thermodynamic process and it stands for a system where a transformation takes place in such a way that no gain or loss of heat or energy occurs. This paper discusses an energy efficient way of designing the combinational logic circuits using adiabatic technique to minimise the power consumption. A comparative analysis for power consumption between conventional CMOS designs of the AND, NAND, OR, Inverter Logic and their adiabatic designs has been performed at 180nm. A power saving of up to 33% in AND gate, 16% in NAND, 6% in NOR and 5% in Inverter respectively is observed at V_{DD}=1.8V, and T=27^0C.
Key Words: Adiabatic circuits, AND Logic, Combinational Circuits, Inverter, Low-Power, NAND Logic, OR Logic.

I. INTRODUCTION

In today's world Power reduction is one of the major concern in designing in VLSI using various methodologies because of two major reasons one is the long battery life requirement in digital equipment and in mobiles also and second is high power dissipation due to increase in number of transistors on a chip which results in problems in IC packaging and reliability [1].

Adiabatic logic uses AC power supply instead of constant DC supply and this is one of the main reasons in the reduction of power dissipation. The main idea in an adiabatic charging is that transitions are considered to be sufficiently slow so that all the nodes are charged or discharged at a constant current. In this way power dissipation is minimized by decreasing the peak current flow through the transistors.Use of adiabatic logic circuits with energy recovery scheme has received considerable attention in high performance low-power applications [2,3,4].

In this paper, the section II, discusses the review of previously reported work on power calculation in different combinational circuits. In section III, the designing and simulation of various combinational logic units like NAND, AND, OR and INVERTER has been performed and power consumption analysis is performed using adiabatic reduction techniques. Finally the conclusion has been discussed in section IV.

II. A REVIEW OF RELATED WORK

Various adiabatic power reduction techniques, e.g., Complementary Pass Transistor Logic, Two phase clocked adiabatic static CMOS logic, Two phase adiabatic dynamic CMOS logic, Adiabatic dynamic CMOS logic NOR, Quasi-static energy recovery logic NOR gate techniques etc. has been proposed by the researchers. A brief description of some of these techniques is as.

i. High Performance Sequential Circuits with Adiabatic Complementary Pass-Transistor Logic

The sequential circuits are implemented using Pure NMOS Transistors and the 4-Bit Shift Register is realized with Complementary Pass Transistor Logic and after implementation the Adiabatic D & JK flip-flop designs are proposed [5].
The analysis is performed on Cadence design tools. The power saving analysis is shown in Table1.

Table 1: Power saving of different Sequential Circuits [5]

Schematic Diagram	Power Saving	Power Saving
Flip Flop	CPAL Logic	2N-2N2P Logic
D	81%	88%
JK	13% to 68%	69% to 91%

ii. Analysis of Adiabatic Logic NOR Gate for Power Reduction

A NOR gate design is discussed using adiabatic reduction technique using five techniques namely Two phase clocked adiabatic static CMOS logic, Two phase adiabatic dynamic CMOS logic, Adiabatic dynamic CMOS logic NOR, Quasi-static energy recovery logic NOR gate techniques is studied [6]. According to the analysis done the 2PASCL NOR logic gives lowest dissipation power at frequency 10 to

1000MHZ. The simulations are performed using Tanner Tool Version 13 on 0.18µm. A constant output load capacitance of 1pf is used for power and delay measurement. CMOS technology and transient analysis is done at 1.8v supply voltage which is shown in Table2.

Table 2: Transient Simulation Results [6]

Input A	Input B	2PASCL	2PADCL	ADCL	QUASSI
0	0	Weak 0	Weak 1	Strong 1	Strong 1
0	1	Strong 0	Strong 0	Strong 0	Strong 0
1	0	Strong 0	Strong 0	Strong 0	Strong 0
1	1	Strong 0	Strong 0	Strong 0	Strong 0

III. SIMULATION OF ADIABATIC LOGIC CIRCUITS: AND, OR, NAND, & INVERTER

In this section the study and implementation of combinational logic units using adiabatic logic and conventional CMOS techniques at transistor level is carried out along with the Power analysis. The following parameters are taken in to account while designing.

Table 3: Width (W) and Length (L) for NMOS and PMOS

Technology	**180nm**
W(NMOS)	2µm
L(NMOS)	18µm
W(PMOS)	2 µm
L(PMOS)	18 µm

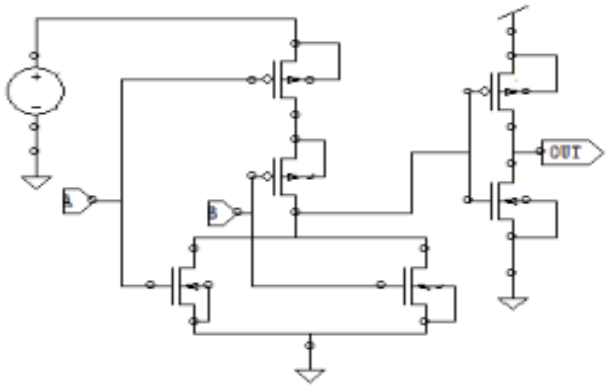

Figure 1: Schematic of Adiabatic NAND Gate

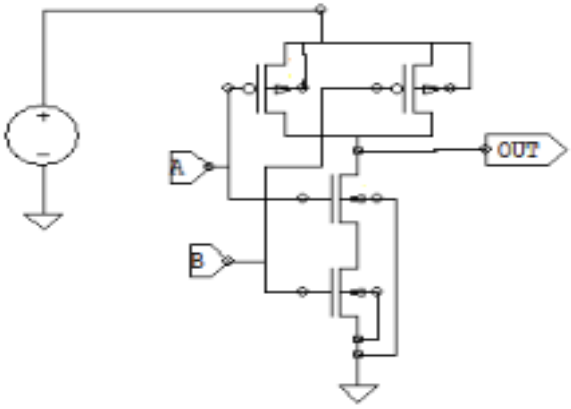

Figure 2: Schematic of Adiabatic OR Gate

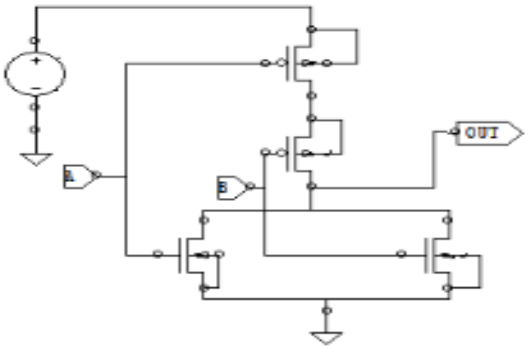

Figure 3: Schematic of Adiabatic AND Gate

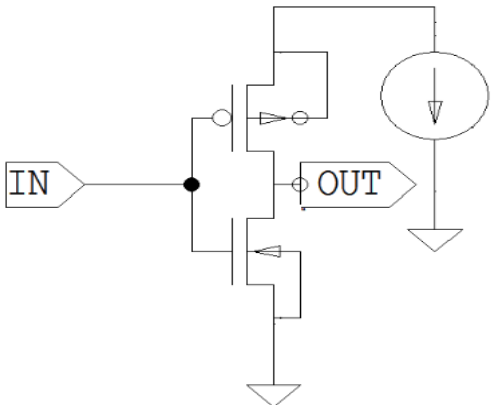

Figure 4: Schematic of Adiabatic Inverter Circuit

The power consumed for conventional CMOS circuits and with Adiabatic power reduction technique for NAND, AND, OR gate and Inverter is calculated on 180nm technology with 1.8 Volt supply. The graphical representation of power consumption in different Combinational Circuits is shown in Figure 5 along with the percentage of power reduction of the combinational logic units Figure 6.

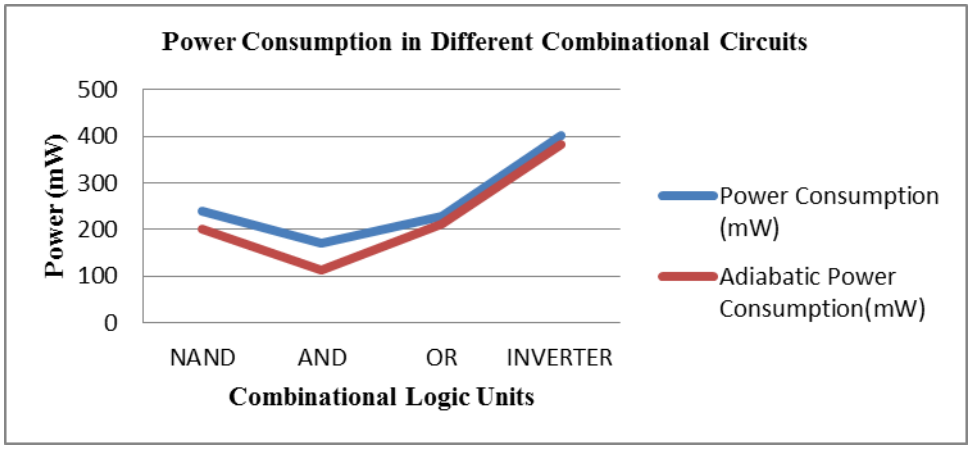

Figure 5: Analysis of power consumption of Different Combinational Circuits

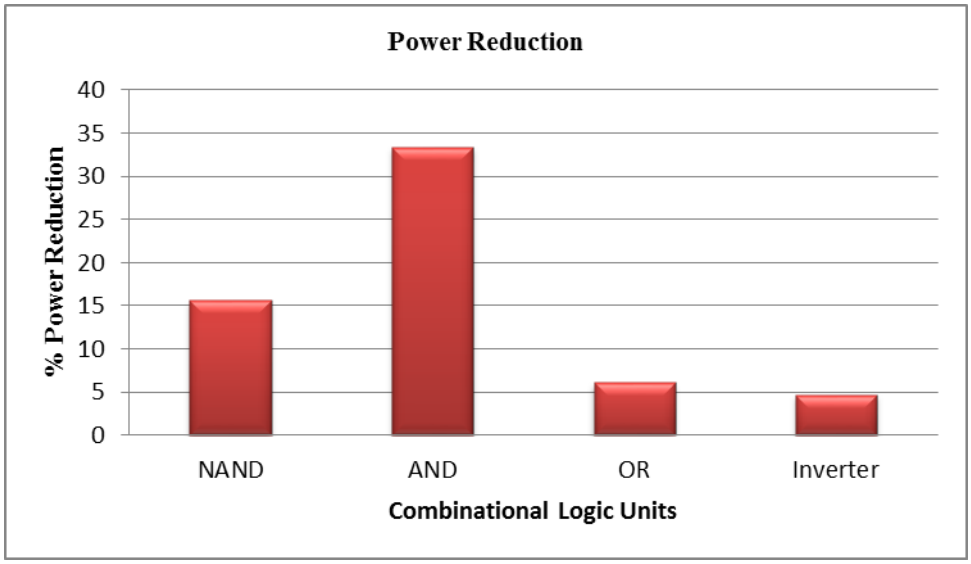

Figure 6: Analysis of % of power consumption of Different Combinational Logic units

IV. CONCLUSIONS

In this analysis, it is investigated that the AND gate has the highest level of power reduction of 33.4% whereas Inverter with lowest level of power reduction of 4.72% at adiabatic logic level. A power reduction of 15.6% and 6.1% is seen at NAND and OR logic units. All the parameters are computed on Cadence Virtuoso Tool at 180 nm Technology at 1.8V supply voltage. This reduction technique can be used in applications such as Memory Designing, in high performance low power circuits and various high end processors.

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